


# THE DATASHEET OF FPGA

# APEX 20KC

## Programmable Logic Device

February 2004 ver. 2.2 Data Sheet

## Features...

- Programmable logic device (PLD) manufactured using a 0.15-µm all-layer copper-metal fabrication process
  - 25 to 35% faster design performance than APEX™ 20KE devices
  - Pin-compatible with APEX 20KE devices
  - High-performance, low-power copper interconnect
  - MultiCore™ architecture integrating look-up table (LUT) logic and embedded memory
  - LUT logic used for register-intensive functions
  - Embedded system blocks (ESBs) used to implement memory functions, including first-in first-out (FIFO) buffers, dual-port RAM, and content-addressable memory (CAM)
- High-density architecture
  - 200,000 to 1 million typical gates (see Table 1)
  - Up to 38,400 logic elements (LEs)
  - Up to 327,680 RAM bits that can be used without reducing available logic

*Table 1. APEX 20KC Device Features* *Note (1)*

| Feature | EP20K200C | EP20K400C | EP20K600C | EP20K1000C |
|---|---|---|---|---|
| Maximum system gates | 526,000 | 1,052,000 | 1,537,000 | 1,772,000 |
| Typical gates | 200,000 | 400,000 | 600,000 | 1,000,000 |
| LEs | 8,320 | 16,640 | 24,320 | 38,400 |
| ESBs | 52 | 104 | 152 | 160 |
| Maximum RAM bits | 106,496 | 212,992 | 311,296 | 327,680 |
| PLLs *(2)* | 2 | 4 | 4 | 4 |
| Speed grades *(3)* | -7, -8, -9 | -7, -8, -9 | -7, -8, -9 | -7, -8, -9 |
| Maximum macrocells | 832 | 1,664 | 2,432 | 2,560 |
| Maximum user I/O pins | 376 | 488 | 588 | 708 |

*Notes to Table 1:*

(1) The embedded IEEE Std. 1149.1 Joint Test Action Group (JTAG) boundary-scan circuitry contributes up to 57,000 additional gates.
(2) PLL: phase-locked loop.
(3) The -7 speed grade provides the fastest performance.

## …and More Features

- Low-power operation design
  - 1.8-V supply voltage (see Table 2)
  - Copper interconnect reduces power consumption
  - MultiVolt™ I/O support for 1.8-V, 2.5-V, and 3.3-V interfaces
  - ESBs offering programmable power-saving mode
- Flexible clock management circuitry with up to four phase-locked loops (PLLs)
  - Built-in low-skew clock tree
  - Up to eight global clock signals
  - ClockLock™ feature reducing clock delay and skew
  - ClockBoost™ feature providing clock multiplication and division
  - ClockShift™ feature providing programmable clock phase and delay shifting
- Powerful I/O features
  - Compliant with peripheral component interconnect Special Interest Group (PCI SIG) ***PCI Local Bus Specification, Revision 2.2*** for 3.3-V operation at 33 or 66 MHz and 32 or 64 bits
  - Support for high-speed external memories, including DDR synchronous dynamic RAM (SDRAM) and ZBT static RAM (SRAM)
  - 16 input and 16 output LVDS channels at 840 megabits per second (Mbps)
  - Direct connection from I/O pins to local interconnect providing fast $t_{CO}$ and $t_{SU}$ times for complex logic
  - MultiVolt I/O support for 1.8-V, 2.5-V, and 3.3-V interfaces
  - Programmable clamp to $V_{CCIO}$
  - Individual tri-state output enable control for each pin
  - Programmable output slew-rate control to reduce switching noise
  - Support for advanced I/O standards, including low-voltage differential signaling (LVDS), LVPECL, PCI-X, AGP, CTT, SSTL-3 and SSTL-2, GTL+, and HSTL Class I
  - Supports hot-socketing operation
  - Pull-up on I/O pins before and during configuration

*Table 2. APEX 20KC Supply Voltages*

| Feature | Voltage |
|---|---|
| Internal supply voltage ($V_{CCINT}$) | 1.8 V |
| MultiVolt I/O interface voltage levels ($V_{CCIO}$) | 1.8 V, 2.5 V, 3.3 V, 5.0 V *(1)* |

***Note to Table 2:***
(1) APEX 20KC devices can be 5.0-V tolerant by using an external resistor.

- Advanced interconnect structure
  - Copper interconnect for high performance
  - Four-level hierarchical FastTrack® interconnect structure providing fast, predictable interconnect delays
  - Dedicated carry chain that implements arithmetic functions such as fast adders, counters, and comparators (automatically used by software tools and megafunctions)
  - Dedicated cascade chain that implements high-speed, high-fan-in logic functions (automatically used by software tools and megafunctions)
  - Interleaved local interconnect allows one LE to drive 29 other LEs through the fast local interconnect
- Advanced software support
  - Software design support and automatic place-and-route provided by the Altera® Quartus™ II development system for Windows-based PCs, Sun SPARCstations, and HP 9000 Series 700/800 workstations
  - Altera MegaCore® functions and Altera Megafunction Partners Program (AMPP℠) megafunctions optimized for APEX 20KC architecture available
  - NativeLink™ integration with popular synthesis, simulation, and timing analysis tools
  - Quartus II SignalTap® embedded logic analyzer simplifies in-system design evaluation by giving access to internal nodes during device operation
  - Supports popular revision-control software packages including PVCS, RCS, and SCCS

*Table 3. APEX 20KC QFP & BGA Package Options & I/O Count* *Notes (1), (2)*

| Device | 208-Pin PQFP | 240-Pin PQFP | 356-Pin BGA | 652-Pin BGA |
|---|---|---|---|---|
| EP20K200C | 136 | 168 | 271 | |
| EP20K400C | | | | 488 |
| EP20K600C | | | | 488 |
| EP20K1000C | | | | 488 |

*Table 4. APEX 20KC FineLine BGA Package Options & I/O Count Notes (1), (2)*

| Device | 484 Pin | 672 Pin | 1,020 Pin |
|---|---|---|---|
| EP20K200C | 376 | | |
| EP20K400C | | 488 (3) | |
| EP20K600C | | 508 (3) | 588 |
| EP20K1000C | | 508 (3) | 708 |

*Notes to Tables 3 and 4:*

(1) I/O counts include dedicated input and clock pins.
(2) APEX 20KC device package types include plastic quad flat pack (PQFP), 1.27-mm pitch ball-grid array (BGA), and 1.00-mm pitch FineLine BGA™ packages.
(3) This device uses a thermally enhanced package, which is taller than the regular package. Consult the *Altera Device Package Information Data Sheet* for detailed package size information.

*Table 5. APEX 20KC QFP & BGA Package Sizes*

| Feature | 208-Pin PQFP | 240-Pin PQFP | 356-Pin BGA | 652-Pin BGA |
|---|---|---|---|---|
| Pitch (mm) | 0.50 | 0.50 | 1.27 | 1.27 |
| Area ($mm^2$) | 924 | 1,218 | 1,225 | 2,025 |
| Length × Width (mm × mm) | 30.4 × 30.4 | 34.9 × 34.9 | 35.0 × 35.0 | 45.0 × 45.0 |

*Table 6. APEX 20KC FineLine BGA Package Sizes*

| Feature | 484 Pin | 672 Pin | 1,020 Pin |
|---|---|---|---|
| Pitch (mm) | 1.00 | 1.00 | 1.00 |
| Area ($mm^2$) | 529 | 729 | 1,089 |
| Length × Width (mm × mm) | 23 × 23 | 27 × 27 | 33 × 33 |

## General Description

Similar to APEX 20K and APEX 20KE devices, APEX 20KC devices offer the MultiCore architecture, which combines the strengths of LUT-based and product-term-based devices with an enhanced memory structure. LUT-based logic provides optimized performance and efficiency for data-path, register-intensive, mathematical, or digital signal processing (DSP) designs. Product-term-based logic is optimized for complex combinatorial paths, such as complex state machines. LUT- and product-term-based logic combined with memory functions and a wide variety of MegaCore and AMPP functions make the APEX 20KC architecture uniquely suited for SOPC designs. Applications historically requiring a combination of LUT-, product-term-, and memory-based devices can now be integrated into one APEX 20KC device.

APEX 20KC devices include additional features such as enhanced I/O standard support, CAM, additional global clocks, and enhanced ClockLock clock circuitry. Table 7 shows the features included in APEX 20KC devices.

*Table 7. APEX 20KC Device Features (Part 1 of 2)*

| Feature | APEX 20KC Devices |
|---|---|
| MultiCore system integration | Full support |
| Hot-socketing support | Full support |
| SignalTap logic analysis | Full support |
| 32-/64-bit, 33-MHz PCI | Full compliance |
| 32-/64-bit, 66-MHz PCI | Full compliance in -7 and -8 speed grades in selected devices |
| MultiVolt I/O | 1.8-V, 2.5-V, or 3.3-V $V_{CCIO}$<br>$V_{CCIO}$ selected bank by bank<br>5.0-V tolerant with use of external resistor |
| ClockLock support | Clock delay reduction<br>$m/(n \times v)$ clock multiplication<br>Drive ClockLock output off-chip<br>External clock feedback<br>ClockShift circuitry<br>LVDS support<br>Up to four PLLs<br>ClockShift clock phase adjustment |
| Dedicated clock and input pins | Eight |

*Table 7. APEX 20KC Device Features (Part 2 of 2)*

| Feature | APEX 20KC Devices |
|---|---|
| I/O standard support | 1.8-V, 2.5-V, 3.3-V, 5.0-V I/O<br>3.3-V PCI and PCI-X<br>3.3-V AGP<br>CTT<br>GTL+<br>LVCMOS<br>LVTTL<br>True-LVDS™ and LVPECL data pins (in EP20K400C and larger devices)<br>LVDS and LVPECL clock pins (in all devices)<br>LVDS and LVPECL data pins up to 156 Mbps (in EP20K200C devices)<br>HSTL Class I<br>PCI-X<br>SSTL-2 Class I and II<br>SSTL-3 Class I and II |
| Memory support | CAM<br>Dual-port RAM<br>FIFO<br>RAM<br>ROM |

All APEX 20KC devices are reconfigurable and are 100% tested prior to shipment. As a result, test vectors do not have to be generated for fault-coverage purposes. Instead, the designer can focus on simulation and design verification. In addition, the designer does not need to manage inventories of different application-specific integrated circuit (ASIC) designs; APEX 20KC devices can be configured on the board for the specific functionality required.

APEX 20KC devices are configured at system power-up with data stored in an Altera serial configuration device or provided by a system controller. Altera offers in-system programmability (ISP)-capable EPC16, EPC8, EPC4, EPC2, and EPC1 configuration devices and one-time programmable (OTP) EPC1 configuration devices, which configure APEX 20KC devices via a serial data stream. Moreover, APEX 20KC devices contain an optimized interface that permits microprocessors to configure APEX 20KC devices serially or in parallel, and synchronously or asynchronously. The interface also enables microprocessors to treat APEX 20KC devices as memory and configure the device by writing to a virtual memory location, making reconfiguration easy.

After an APEX 20KC device has been configured, it can be reconfigured in-circuit by resetting the device and loading new data. Real-time changes can be made during system operation, enabling innovative reconfigurable computing applications.

APEX 20KC devices are supported by the Altera Quartus II development system, a single, integrated package that offers HDL and schematic design entry, compilation and logic synthesis, full simulation and worst-case timing analysis, SignalTap logic analysis, and device configuration. The Quartus II software runs on Windows-based PCs, Sun SPARCstations, and HP 9000 Series 700/800 workstations.

The Quartus II software provides NativeLink interfaces to other industry-standard PC- and UNIX workstation-based EDA tools. For example, designers can invoke the Quartus II software from within third-party design tools. Further, the Quartus II software contains built-in optimized synthesis libraries; synthesis tools can use these libraries to optimize designs for APEX 20KC devices. For example, the Synopsys Design Compiler library, supplied with the Quartus II development system, includes DesignWare functions optimized for the APEX 20KC architecture.

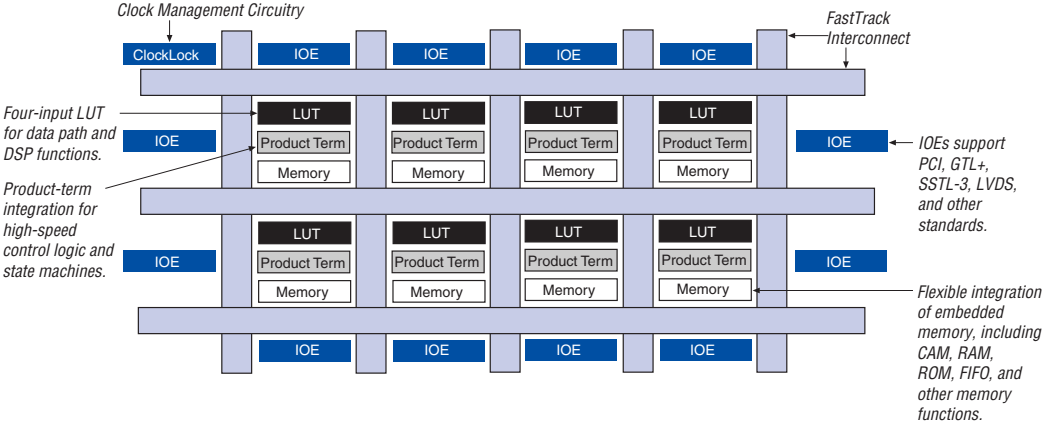
## Functional Description

APEX 20KC devices incorporate LUT-based logic, product-term-based logic, and memory into one device on an all-copper technology process. Signal interconnections within APEX 20KC devices (as well as to and from device pins) are provided by the FastTrack interconnect—a series of fast, continuous row and column channels that run the entire length and width of the device.

Each I/O pin is fed by an I/O element (IOE) located at the end of each row and column of the FastTrack interconnect. Each IOE contains a bidirectional I/O buffer and a register that can be used as either an input or output register to feed input, output, or bidirectional signals. When used with a dedicated clock pin, these registers provide exceptional performance. IOEs provide a variety of features, such as 3.3-V, 64-bit, 66-MHz PCI compliance; JTAG BST support; slew-rate control; and tri-state buffers. APEX 20KC devices offer enhanced I/O support, including support for 1.8-V I/O, 2.5-V I/O, LVCMOS, LVTTL, LVPECL, 3.3-V PCI, PCI-X, LVDS, GTL+, SSTL-2, SSTL-3, HSTL, CTT, and 3.3-V AGP I/O standards.

The ESB can implement a variety of memory functions, including CAM, RAM, dual-port RAM, ROM, and FIFO functions. Embedding the memory directly into the die improves performance and reduces die area compared to distributed-RAM implementations. Moreover, the abundance of cascadable ESBs allows APEX 20KC devices to implement multiple wide memory blocks for high-density designs. The ESB's high speed ensures it can implement small memory blocks without any speed penalty. Additionally, designers can use the ESBs to create as many different-sized memory blocks as the system requires. Figure 1 shows an overview of the APEX 20KC device.

***Figure 1. APEX 20KC Device Block Diagram***

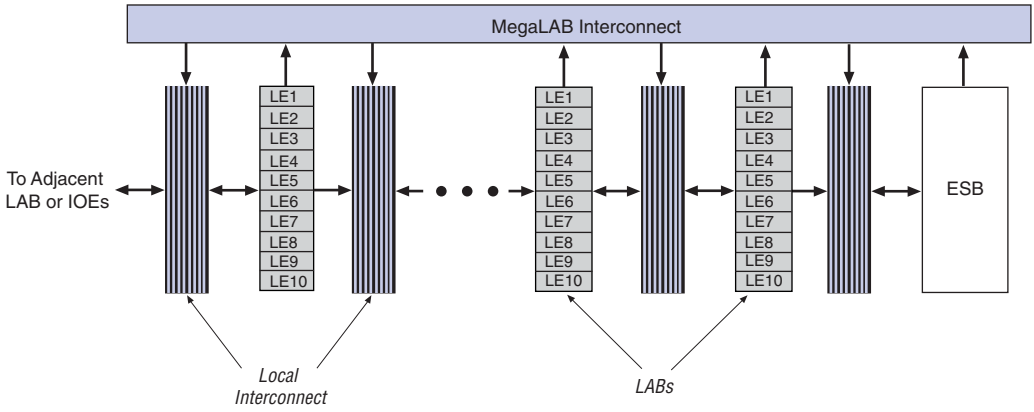



APEX 20KC devices provide four dedicated clock pins and four dedicated input pins that drive register control inputs. These signals ensure efficient distribution of high-speed, low-skew control signals, which use dedicated routing channels to provide short delays and low skews. Four of the dedicated inputs drive four global signals. These four global signals can also be driven by internal logic, providing an ideal solution for a clock divider or internally generated asynchronous clear signals with high fan-out. The dedicated clock pins featured on the APEX 20KC devices can also feed logic. The devices also feature ClockLock and ClockBoost clock management circuitry.

## MegaLAB Structure

APEX 20KC devices are constructed from a series of MegaLAB™ structures. Each MegaLAB structure contains 16 logic array blocks (LABs), one ESB, and a MegaLAB interconnect, which routes signals within the MegaLAB structure. In EP20K1000C devices, MegaLAB structures contain 24 LABs. Signals are routed between MegaLAB structures and I/O pins via the FastTrack interconnect. In addition, edge LABs can be driven by I/O pins through the local interconnect. Figure 2 shows the MegaLAB structure.

*Figure 2. MegaLAB Structure*

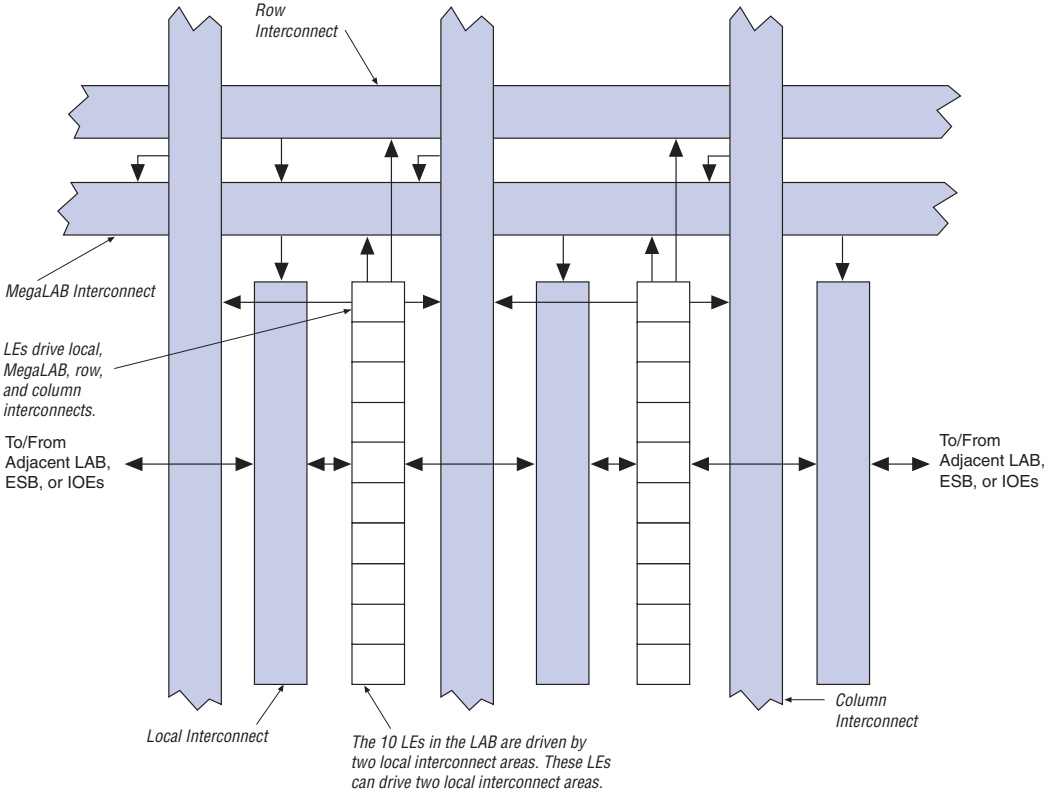



## Logic Array Block

Each LAB consists of 10 LEs, the LEs' associated carry and cascade chains, LAB control signals, and the local interconnect. The local interconnect transfers signals between LEs in the same or adjacent LABs, IOEs, or ESBs. The Quartus II Compiler places associated logic within an LAB or adjacent LABs, allowing the use of a fast local interconnect for high performance. Figure 3 shows the APEX 20KC LAB.

APEX 20KC devices use an interleaved LAB structure. This structure allows each LE to drive two local interconnect areas, minimizing the use of the MegaLAB and FastTrack interconnect and providing higher performance and flexibility. Each LE can drive 29 other LEs through the fast local interconnect.

*Figure 3. LAB Structure*



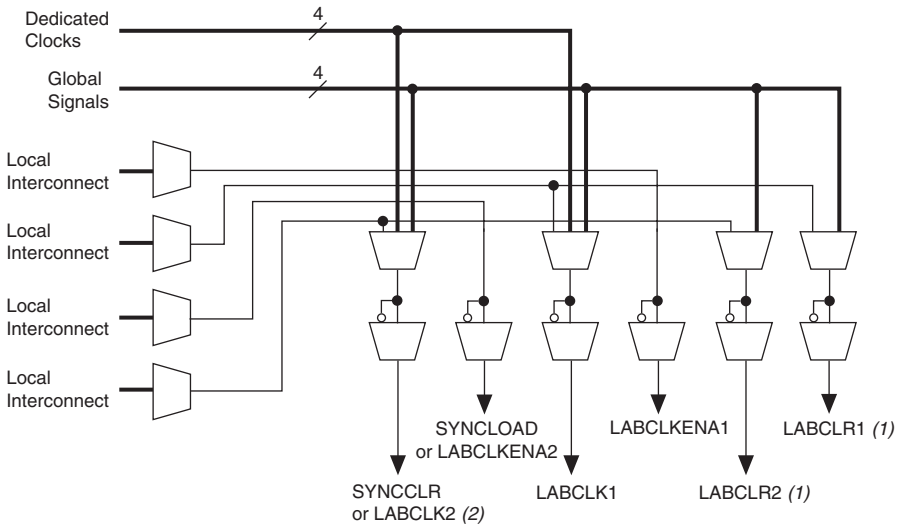

Each LAB contains dedicated logic for driving control signals to its LEs and ESBs. The control signals include clock, clock enable, asynchronous clear, asynchronous preset, asynchronous load, synchronous clear, and synchronous load signals. A maximum of six control signals can be used at a time. Although synchronous load and clear signals are generally used when implementing counters, they can also be used with other functions.

Each LAB can use two clocks and two clock enable signals. Each LAB's clock and clock enable signals are linked (e.g., any LE in a particular LAB using `CLK1` will also use `CLKENA1`). LEs with the same clock but different clock enable signals either use both clock signals in one LAB or are placed into separate LABs.

If both the rising and falling edges of a clock are used in a LAB, both LAB-wide clock signals are used.

The LAB-wide control signals can be generated from the LAB local interconnect, global signals, and dedicated clock pins. The inherent low skew of the FastTrack interconnect enables it to be used for clock distribution. Figure 4 shows the LAB control signal generation circuit.

*Figure 4. LAB Control Signal Generation*




*Notes to Figure 4:*

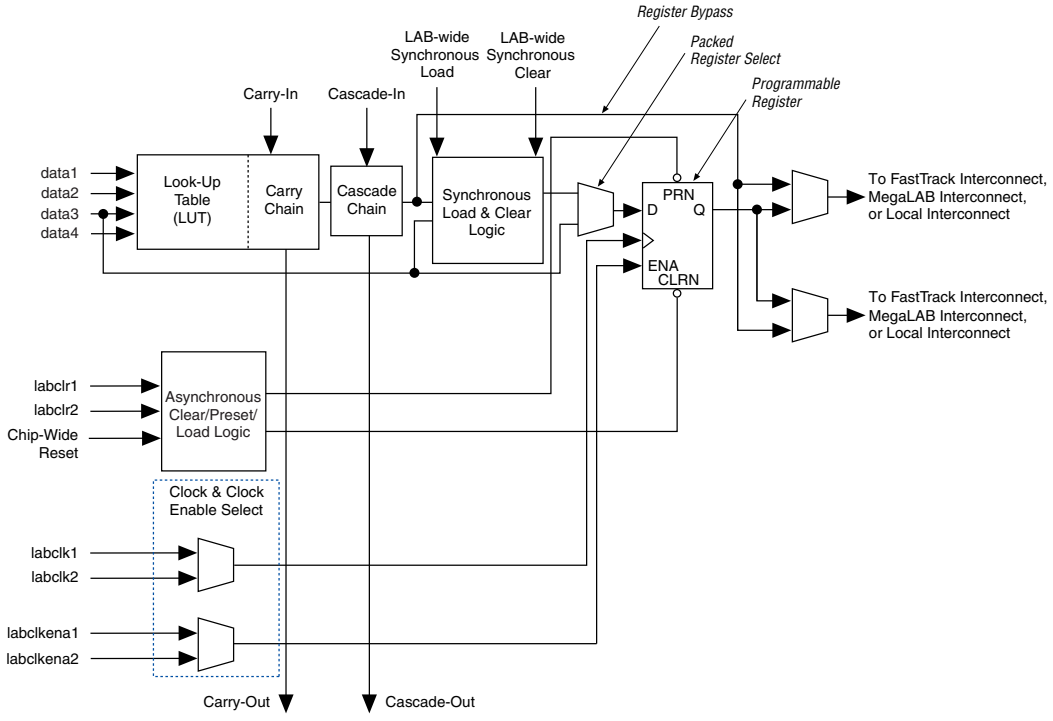
(1) The LABCLR1 and LABCLR2 signals also control asynchronous load and asynchronous preset for LEs within the LAB.

(2) The SYNCCLR signal can be generated by the local interconnect or global signals.

## Logic Element

The LE, the smallest unit of logic in the APEX 20KC architecture, is compact and provides efficient logic usage. Each LE contains a four-input LUT, which is a function generator that can quickly implement any function of four variables. In addition, each LE contains a programmable register and carry and cascade chains. Each LE drives the local interconnect, MegaLAB interconnect, and FastTrack interconnect routing structures. See Figure 5.

*Figure 5. APEX 20KC Logic Element*




Each LE's programmable register can be configured for D, T, JK, or SR operation. The register's clock and clear control signals can be driven by global signals, general-purpose I/O pins, or any internal logic. For combinatorial functions, the register is bypassed and the output of the LUT drives the outputs of the LE.

Each LE has two outputs that drive the local, MegaLAB, or FastTrack interconnect routing structure. Each output can be driven independently by the LUT's or register's output. For example, the LUT can drive one output while the register drives the other output. This feature, called register packing, improves device utilization because the register and the LUT can be used for unrelated functions. The LE can also drive out registered and unregistered versions of the LUT output.

The APEX 20KC architecture provides two types of dedicated high-speed data paths that connect adjacent LEs without using local interconnect paths: carry chains and cascade chains. A carry chain supports high-speed arithmetic functions such as counters and adders, while a cascade chain implements wide-input functions such as equality comparators with minimum delay. Carry and cascade chains connect LEs 1 through 10 in an LAB and all LABs in the same MegaLAB structure.

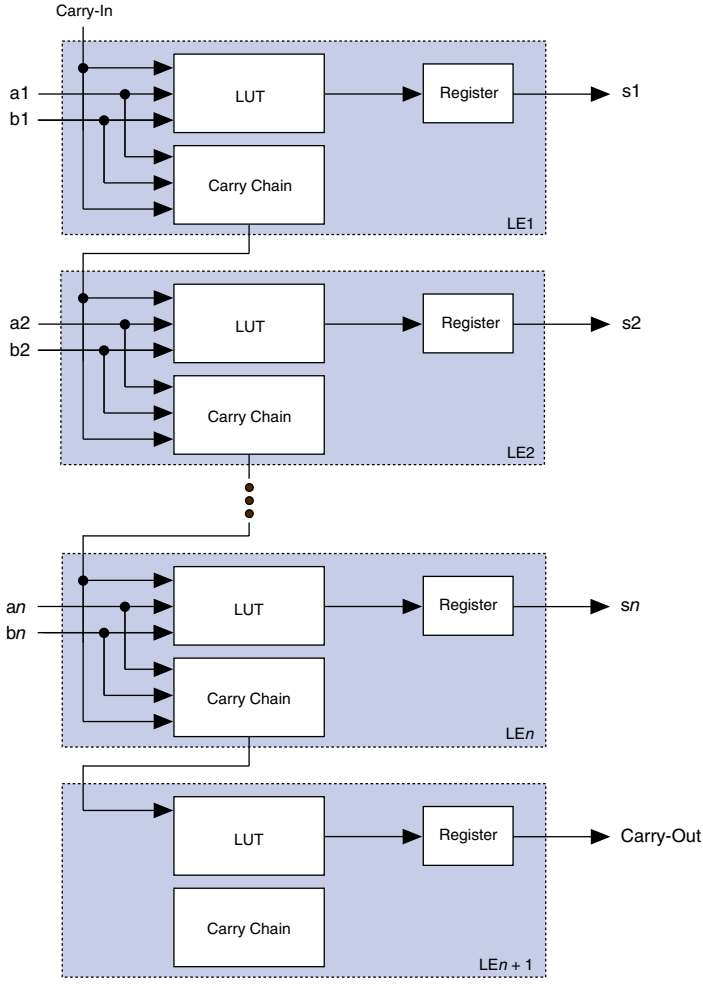
### *Carry Chain*

The carry chain provides a very fast carry-forward function between LEs. The carry-in signal from a lower-order bit drives forward into the higher-order bit via the carry chain, and feeds into both the LUT and the next portion of the carry chain. This feature allows the APEX 20KC architecture to implement high-speed counters, adders, and comparators of arbitrary width. Carry chain logic can be created automatically by the Quartus II Compiler during design processing, or manually by the designer during design entry. Parameterized functions such as DesignWare functions from Synopsys and library of parameterized modules (LPM) functions automatically take advantage of carry chains for the appropriate functions.

The Quartus II Compiler creates carry chains longer than ten LEs by automatically linking LABs together. For enhanced fitting, a long carry chain skips alternate LABs in a MegaLAB structure. A carry chain longer than one LAB skips either from an even-numbered LAB to the next even-numbered LAB, or from an odd-numbered LAB to the next odd-numbered LAB. For example, the last LE of the first LAB in the upper-left MegaLAB structure carries to the first LE of the third LAB in the MegaLAB structure.

Figure 6 shows how an *n*-bit full adder can be implemented in *n* + 1 LEs with the carry chain. One portion of the LUT generates the sum of two bits using the input signals and the carry-in signal; the sum is routed to the output of the LE. The register can be bypassed for simple adders or used for accumulator functions. Another portion of the LUT and the carry chain logic generates the carry-out signal, which is routed directly to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it is driven onto the local, MegaLAB, or FastTrack interconnect routing structures.

*Figure 6. APEX 20KC Carry Chain*

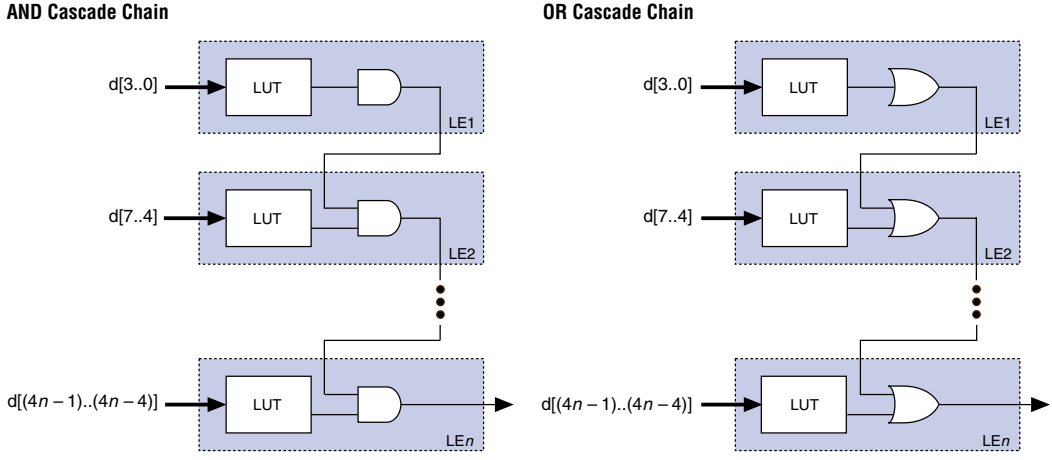


### *Cascade Chain*

With the cascade chain, the APEX 20KC architecture can implement functions with a very wide fan-in. Adjacent LUTs can compute portions of a function in parallel; the cascade chain serially connects the intermediate values. The cascade chain can use a logical AND or logical OR (via De Morgan's inversion) to connect the outputs of adjacent LEs. Each additional LE provides four more inputs to the effective width of a function, with a short cascade delay. Cascade chain logic can be created automatically by the Quartus II Compiler during design processing, or manually by the designer during design entry.

Cascade chains longer than ten LEs are implemented automatically by linking LABs together. For enhanced fitting, a long cascade chain skips alternate LABs in a MegaLAB structure. A cascade chain longer than one LAB skips either from an even-numbered LAB to the next even-numbered LAB, or from an odd-numbered LAB to the next odd-numbered LAB. For example, the last LE of the first LAB in the upper-left MegaLAB structure carries to the first LE of the third LAB in the MegaLAB structure. Figure 7 shows how the cascade function can connect adjacent LEs to form functions with a wide fan-in.

***Figure 7. APEX 20KC Cascade Chain***



### *LE Operating Modes*

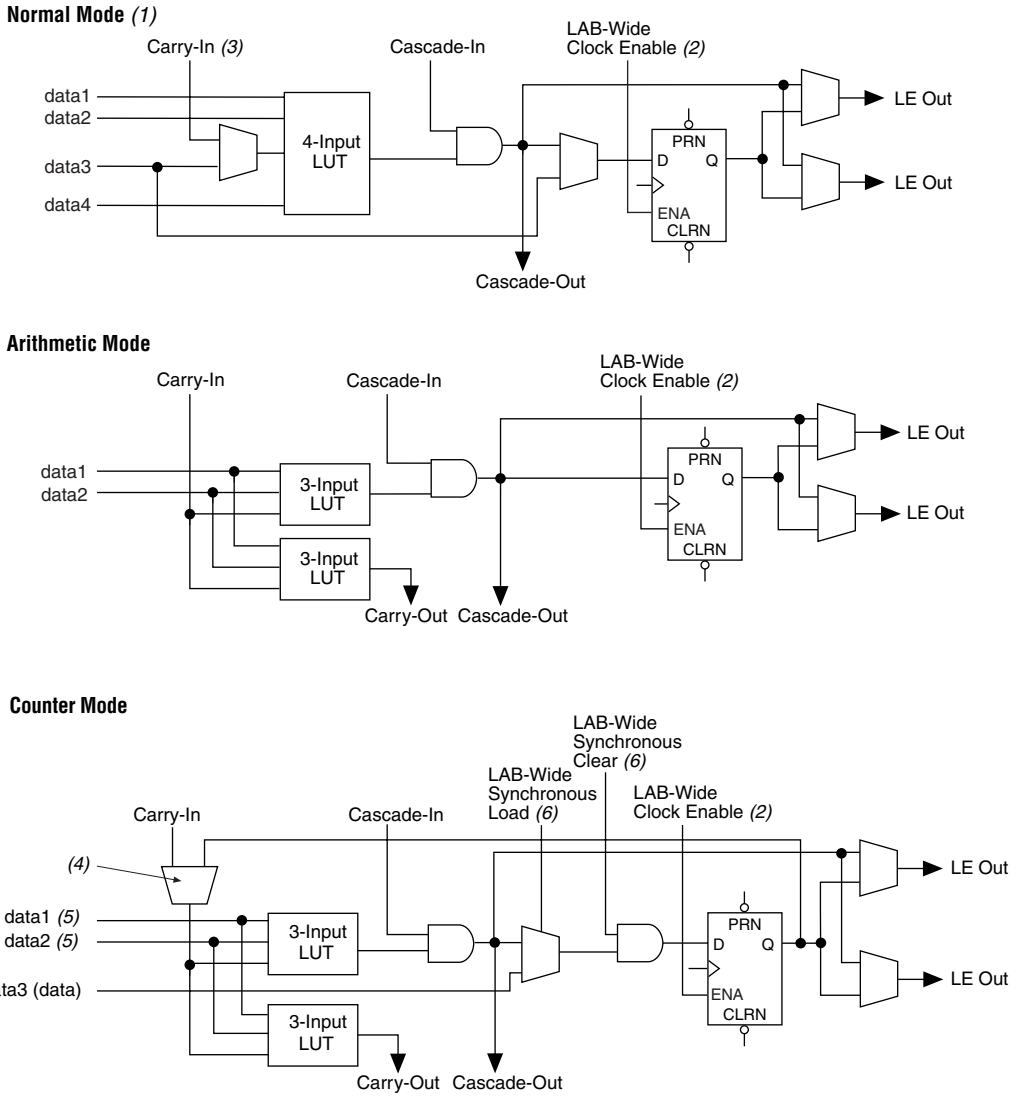
The APEX 20KC LE can operate in one of the following three modes:

- Normal mode
- Arithmetic mode
- Counter mode

Each mode uses LE resources differently. In each mode, seven available inputs to the LE—the four data inputs from the LAB local interconnect, the feedback from the programmable register, and the carry-in and cascade-in from the previous LE—are directed to different destinations to implement the desired logic function. LAB-wide signals provide clock, asynchronous clear, asynchronous preset, asynchronous load, synchronous clear, synchronous load, and clock enable control for the register. These LAB-wide signals are available in all LE modes.

The Quartus II software, in conjunction with parameterized functions such as LPM and DesignWare functions, automatically chooses the appropriate mode for common functions such as counters, adders, and multipliers. If required, the designer can also create special-purpose functions that specify which LE operating mode to use for optimal performance. Figure 8 shows the LE operating modes.

*Figure 8. APEX 20KC LE Operating Modes*




*Notes to Figure 8:*

(1) LEs in normal mode support register packing.
(2) There are two LAB-wide clock enables per LAB.
(3) When using the carry-in in normal mode, the packed register feature is unavailable.
(4) A register feedback multiplexer is available on LE1 of each LAB.
(5) The DATA1 and DATA2 input signals can supply counter enable, up or down control, or register feedback signals for LEs other than the second LE in an LAB.
(6) The LAB-wide synchronous clear and LAB wide synchronous load affect all registers in an LAB.

### Normal Mode

The normal mode is suitable for general logic applications, combinatorial functions, or wide decoding functions that can take advantage of a cascade chain. In normal mode, four data inputs from the LAB local interconnect and the carry-in are inputs to a four-input LUT. The Quartus II Compiler automatically selects the carry-in or the DATA3 signal as one of the inputs to the LUT. The LUT output can be combined with the cascade-in signal to form a cascade chain through the cascade-out signal. LEs in normal mode support packed registers.

### Arithmetic Mode

The arithmetic mode is ideal for implementing adders, accumulators, and comparators. An LE in arithmetic mode uses two 3-input LUTs. One LUT computes a three-input function; the other generates a carry output. As shown in Figure 8, the first LUT uses the carry-in signal and two data inputs from the LAB local interconnect to generate a combinatorial or registered output. For example, when implementing an adder, this output is the sum of three signals: DATA1, DATA2, and carry-in. The second LUT uses the same three signals to generate a carry-out signal, thereby creating a carry chain. The arithmetic mode also supports simultaneous use of the cascade chain. LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output.

The Quartus II software implements parameterized functions that use the arithmetic mode automatically where appropriate; the designer does not need to specify how the carry chain will be used.

### Counter Mode

The counter mode offers clock enable, counter enable, synchronous up/down control, synchronous clear, and synchronous load options. The counter enable and synchronous up/down control signals are generated from the data inputs of the LAB local interconnect. The synchronous clear and synchronous load options are LAB-wide signals that affect all registers in the LAB. Consequently, if any of the LEs in an LAB use the counter mode, other LEs in that LAB must be used as part of the same counter or be used for a combinatorial function. The Quartus II software automatically places any registers that are not used by the counter into other LABs.

The counter mode uses two 3-input LUTs: one generates the counter data, and the other generates the fast carry bit. A 2-to-1 multiplexer provides synchronous loading, and another AND gate provides synchronous clearing. If the cascade function is used by an LE in counter mode, the synchronous clear or load overrides any signal carried on the cascade chain. The synchronous clear overrides the synchronous load. LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output.

### *Clear & Preset Logic Control*

Logic for the register's clear and preset signals is controlled by LAB-wide signals. The LE directly supports an asynchronous clear function. The Quartus II Compiler can use a NOT-gate push-back technique to emulate an asynchronous preset or to emulate simultaneous preset and clear or asynchronous load. However, this technique uses three additional LEs per register. All emulation is performed automatically when the design is compiled. Registers that emulate simultaneous preset and load will enter an unknown state upon power-up or when the chip-wide reset is asserted.

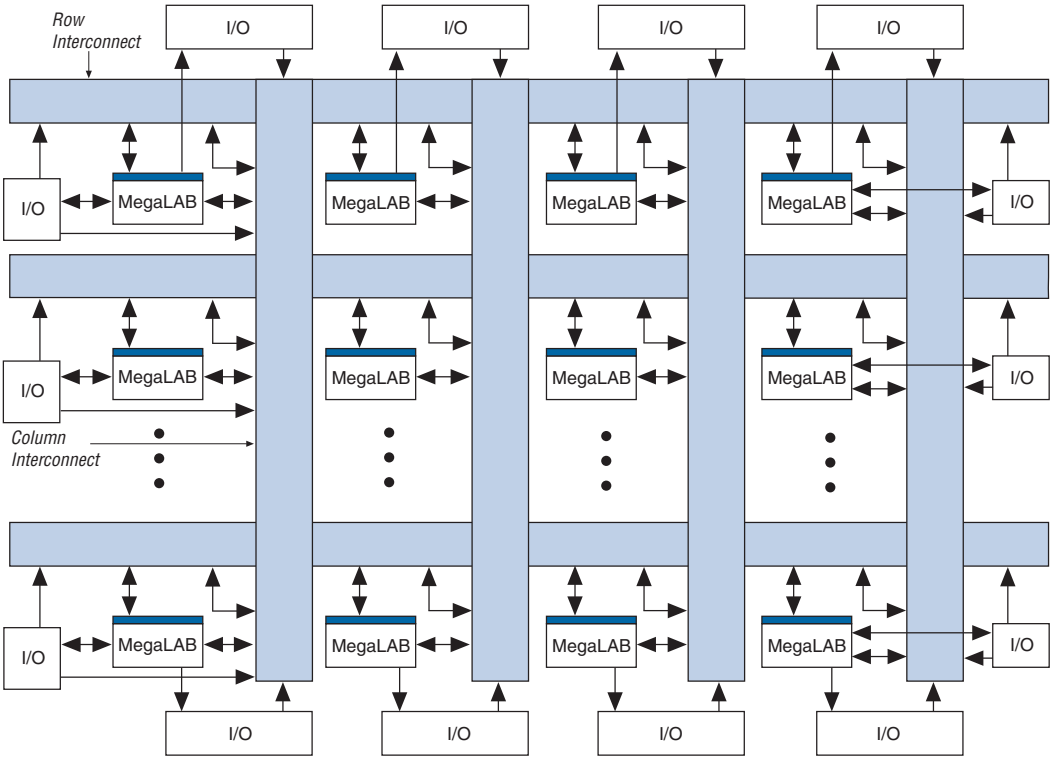
In addition to the two clear and preset modes, APEX 20KC devices provide a chip-wide reset pin (DEV_CLRn) that resets all registers in the device. Use of this pin is controlled through an option in the Quartus II software that is set before compilation. The chip-wide reset overrides all other control signals. Registers using an asynchronous preset are preset when the chip-wide reset is asserted; this effect results from the inversion technique used to implement the asynchronous preset.

## FastTrack Interconnect

In the APEX 20KC architecture, connections between LEs, ESBs, and I/O pins are provided by the FastTrack interconnect. The FastTrack interconnect is a series of continuous horizontal and vertical routing channels that traverse the device. This global routing structure provides predictable performance, even in complex designs. In contrast, the segmented routing in FPGAs requires switch matrices to connect a variable number of routing paths, increasing the delays between logic resources and reducing performance.

The FastTrack interconnect consists of row and column interconnect channels that span the entire device. The row interconnect routes signals throughout a row of MegaLAB structures; the column interconnect routes signals throughout a column of MegaLAB structures. When using the row and column interconnect, an LE, IOE, or ESB can drive any other LE, IOE, or ESB in a device. See Figure 9.

*Figure 9. APEX 20KC Interconnect Structure*




A row line can be driven directly by LEs, IOEs, or ESBs in that row. Further, a column line can drive a row line, allowing an LE, IOE, or ESB to drive elements in a different row via the column and row interconnect. The row interconnect drives the MegaLAB interconnect to drive LEs, IOEs, or ESBs in a particular MegaLAB structure.

A column line can be directly driven by LEs, IOEs, or ESBs in that column. A column line on a device's left or right edge can also be driven by row IOEs. The column line is used to route signals from one row to another. A column line can drive a row line; it can also drive the MegaLAB interconnect directly, allowing faster connections between rows.

Figure 10 shows how the FastTrack interconnect uses the local interconnect to drive LEs within MegaLAB structures.

*Figure 10. FastTrack Connection to Local Interconnect*

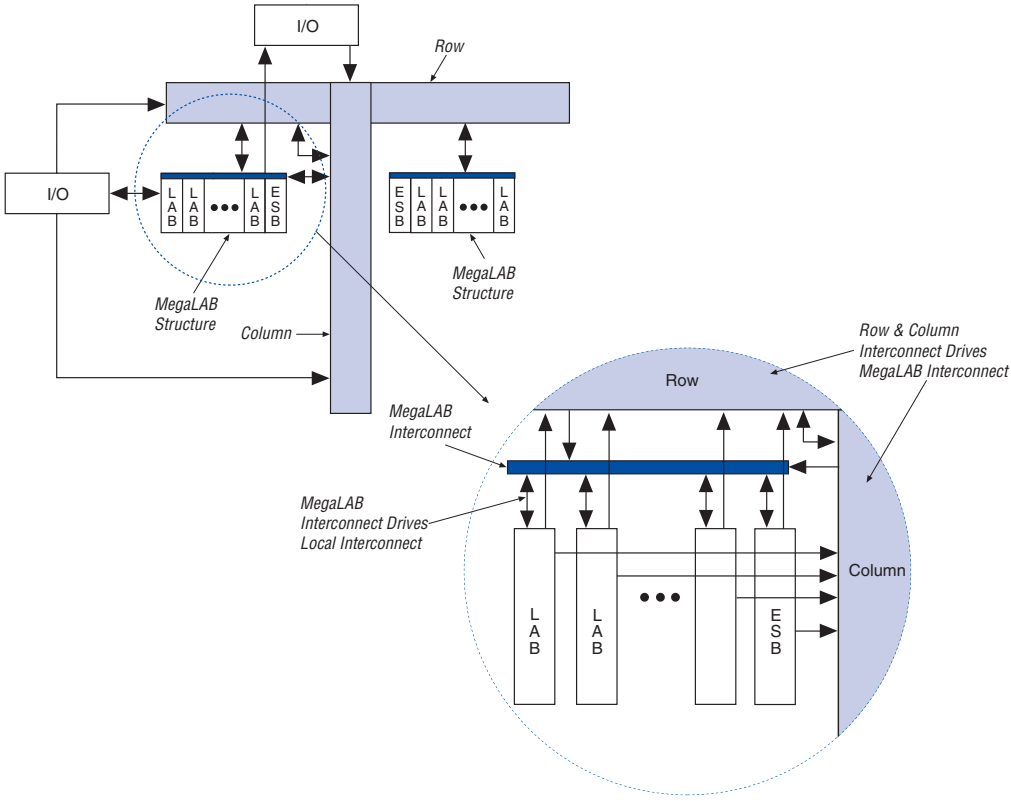
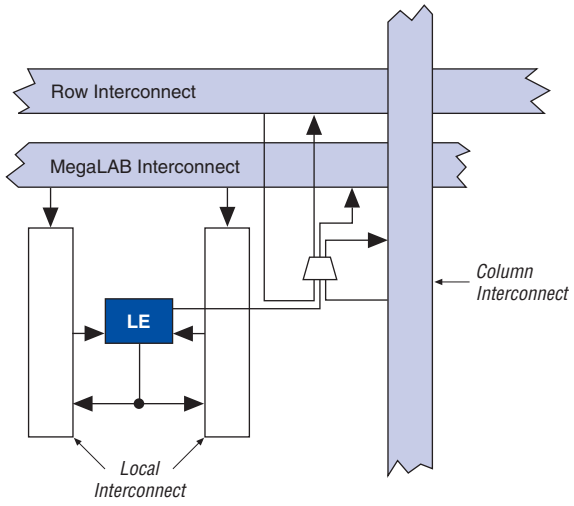


Figure 11 shows the intersection of a row and column interconnect, and how these forms of interconnects and LEs drive each other.

*Figure 11. Driving the FastTrack Interconnect*




APEX 20KC devices include an enhanced interconnect structure for faster routing of input signals with high fan-out. Column I/O pins can drive the FastRow™ interconnect, which routes signals directly into the local interconnect without having to drive through the MegaLAB interconnect. The FastRow lines traverse two MegaLAB structures. Also, these pins can drive the local interconnect directly for fast setup times. On EP20K400C and larger devices, the FastRow interconnect drives the two MegaLAB structures in the top left corner, the two MegaLAB structures in the two right corner, the two MegaLAB structures in the bottom left corner, and the two MegaLAB structures in the bottom right corner. On EP20K200C and smaller devices, FastRow interconnect drives the two MegaLAB structures on the top and the two MegaLAB structures on the bottom of the device. On all devices, the FastRow interconnect drives all local interconnect in the appropriate MegaLAB structures except the end local interconnect on the side of the MegaLAB opposite the ESB. Pins using the FastRow interconnect achieve a faster set-up time, as the signal does not need to use a MegaLAB interconnect line to reach the destination LE. Figure 12 shows the FastRow interconnect.

*Figure 12. APEX 20KC FastRow Interconnect*

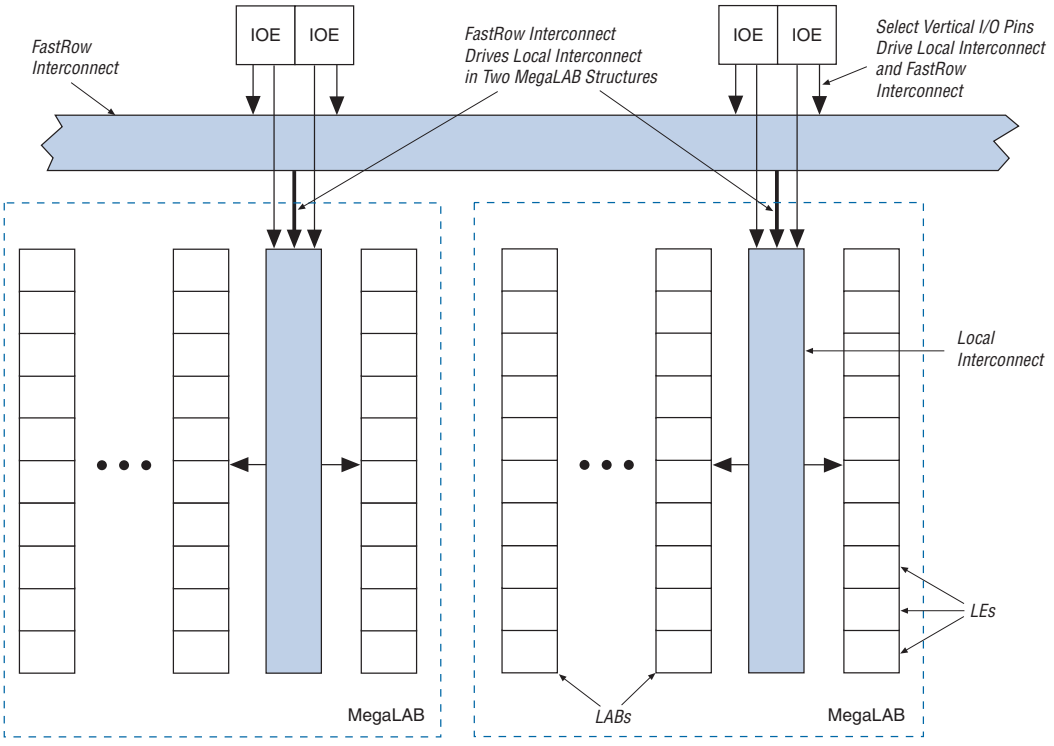



Table 8 summarizes how various elements of the APEX 20KC architecture drive each other.

*Table 8. APEX 20KC Routing Scheme*

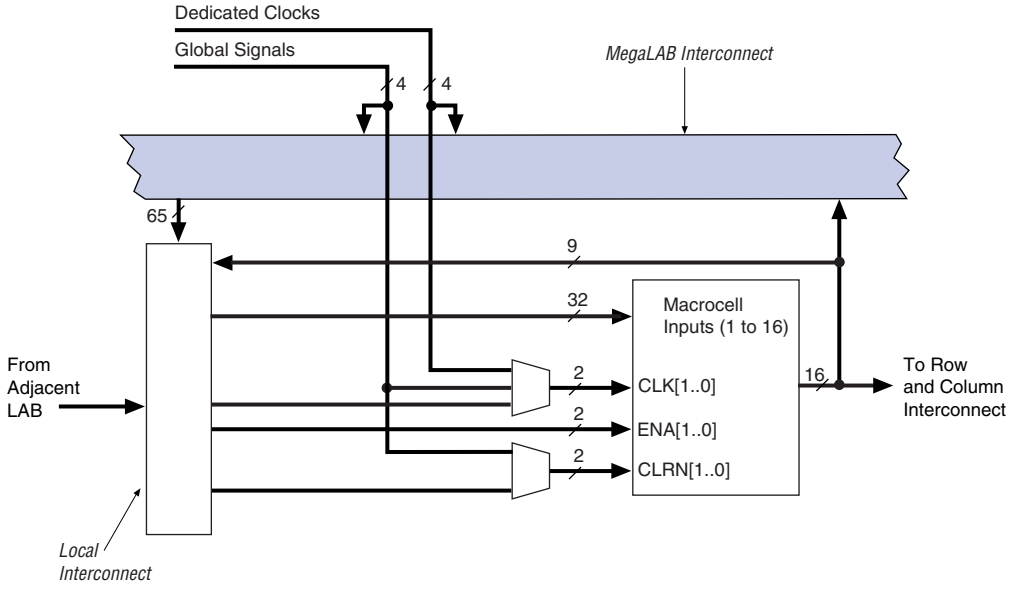
| Source | Destination | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | Row I/O Pin | Column I/O Pin | LE | ESB | Local Interconnect | MegaLAB Interconnect | Row FastTrack Interconnect | Column FastTrack Interconnect | FastRow Interconnect |
| Row I/O pin | | | | | ✓ | ✓ | ✓ | ✓ | |
| Column I/O pin | | | | | | | | ✓ | ✓ |
| LE | | | | | ✓ | ✓ | ✓ | ✓ | |
| ESB | | | | | ✓ | ✓ | ✓ | ✓ | |
| Local interconnect | ✓ | ✓ | ✓ | ✓ | | | | | |
| MegaLAB interconnect | | | | | ✓ | | | | |
| Row FastTrack interconnect | | | | | | ✓ | | ✓ | |
| Column FastTrack interconnect | | | | | | ✓ | ✓ | | |
| FastRow interconnect | | | | | ✓ | | | | |

## Product-Term Logic

The product-term portion of the MultiCore architecture is implemented with the ESB. The ESB can be configured to act as a block of macrocells on an ESB-by-ESB basis. Each ESB is fed by 32 inputs from the adjacent local interconnect; therefore, it can be driven by the MegaLAB interconnect or the adjacent LAB. Also, nine ESB macrocells feed back into the ESB through the local interconnect for higher performance. Dedicated clock pins, global signals, and additional inputs from the local interconnect drive the ESB control signals.

In product-term mode, each ESB contains 16 macrocells. Each macrocell consists of two product terms and a programmable register. Figure 13 shows the ESB in product-term mode.

*Figure 13. Product-Term Logic in ESB*

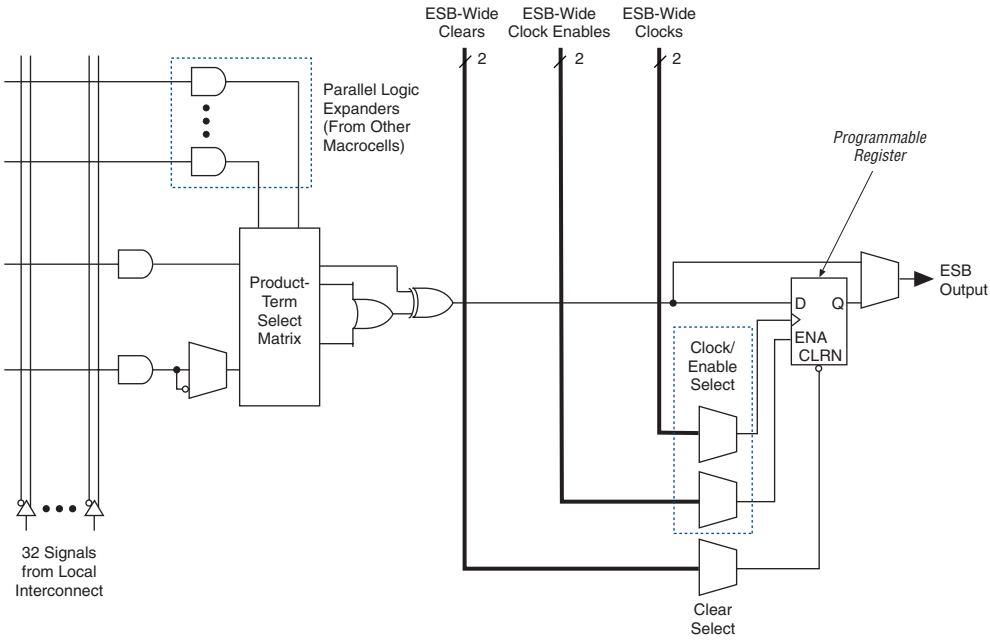



### *Macrocells*

APEX 20KC macrocells can be configured individually for either sequential or combinatorial logic operation. The macrocell consists of three functional blocks: the logic array, the product-term select matrix, and the programmable register.

Combinatorial logic is implemented in the product terms. The product-term select matrix allocates these product terms for use as either primary logic inputs (to the OR and XOR gates) to implement combinatorial functions, or as parallel expanders to be used to increase the logic available to another macrocell. One product term can be inverted; the Quartus II software uses this feature to perform De Morgan's inversion for more efficient implementation of wide OR functions. The Quartus II Compiler can use a NOT-gate push-back technique to emulate an asynchronous preset. Figure 14 shows the APEX 20KC macrocell.

*Figure 14. APEX 20KC Macrocell*



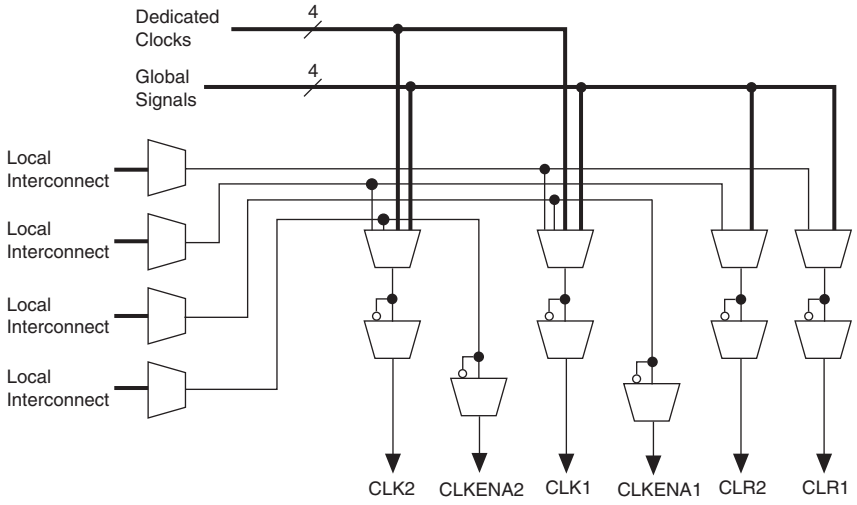

For registered functions, each macrocell register can be programmed individually to implement D, T, JK, or SR operation with programmable clock control. The register can be bypassed for combinatorial operation. During design entry, the designer specifies the desired register type; the Quartus II software then selects the most efficient register operation for each registered function to optimize resource utilization. The Quartus II software or other synthesis tools can also select the most efficient register operation automatically when synthesizing HDL designs.

Each programmable register can be clocked by one of two ESB-wide clocks. The ESB-wide clocks can be generated from device dedicated clock pins, global signals, or local interconnect. Each clock also has an associated clock enable, generated from the local interconnect. The clock and clock enable signals are related for a particular ESB; any macrocell using a clock also uses the associated clock enable.

If both the rising and falling edges of a clock are used in an ESB, both ESB-wide clock signals are used.

The programmable register also supports an asynchronous clear function. Within the ESB, two asynchronous clears are generated from global signals and the local interconnect. Each macrocell can either choose between the two asynchronous clear signals or choose to not be cleared. Either of the two clear signals can be inverted within the ESB. Figure 15 shows the ESB control logic when implementing product-terms.

*Figure 15. ESB Product-Term Mode Control Logic*

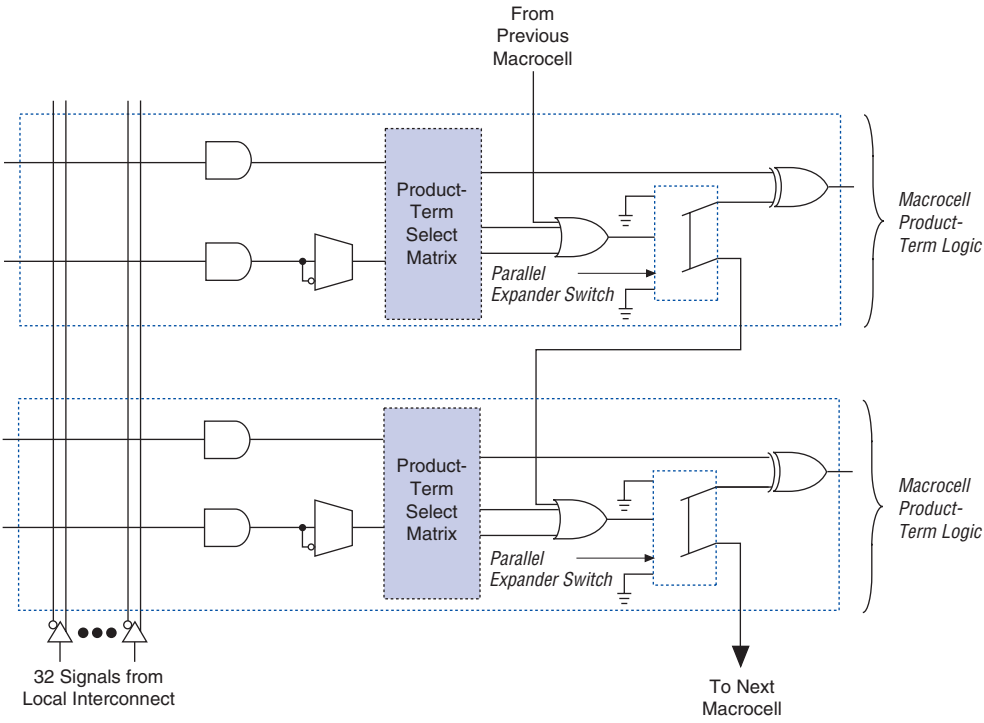



### *Parallel Expanders*

Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 32 product terms to feed the macrocell OR logic directly, with two product terms provided by the macrocell and 30 parallel expanders provided by the neighboring macrocells in the ESB.

The Quartus II Compiler can allocate up to 15 sets of up to two parallel expanders per set to the macrocells automatically. Each set of two parallel expanders incurs a small, incremental timing delay. Figure 16 shows the APEX 20KC parallel expanders.

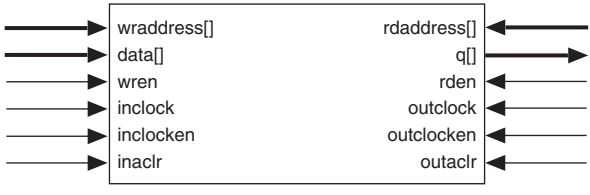
*Figure 16. APEX 20KC Parallel Expanders*




## Embedded System Block

The ESB can implement various types of memory blocks, including dual-port RAM, ROM, FIFO, and CAM blocks. The ESB includes input and output registers; the input registers synchronize writes, and the output registers can pipeline designs to improve system performance. The ESB offers a dual-port mode, which supports simultaneous reads and writes at two different clock frequencies. Figure 17 shows the ESB block diagram.

*Figure 17. ESB Block Diagram*



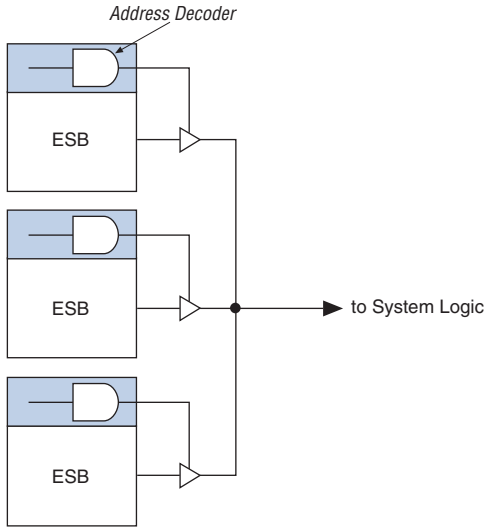
ESBs can implement synchronous RAM, which is easier to use than asynchronous RAM. A circuit using asynchronous RAM must generate the RAM write enable (WE) signal, while ensuring that its data and address signals meet setup and hold time specifications relative to the WE signal. In contrast, the ESB's synchronous RAM generates its own WE signal and is self-timed with respect to the global clock. Circuits using the ESB's self-timed RAM must only meet the setup and hold time specifications of the global clock.

ESB inputs are driven by the adjacent local interconnect, which in turn can be driven by the FastTrack or MegaLAB interconnect. Because the ESB can be driven by the local interconnect, an adjacent LE can drive it directly for fast memory access. ESB outputs drive the FastTrack and MegaLAB interconnects. In addition, ten ESB outputs, nine of which are unique output lines, drive the local interconnect for fast connection to adjacent LEs or for fast feedback product-term logic.

When implementing memory, each ESB can be configured in any of the following sizes: 128 × 16, 256 × 8, 512 × 4, 1,024 × 2, or 2,048 × 1. By combining multiple ESBs, the Quartus II software implements larger memory blocks automatically. For example, two 128 × 16 RAM blocks can be combined to form a 128 × 32 RAM block, and two 512 × 4 RAM blocks can be combined to form a 512 × 8 RAM block. Memory performance does not degrade for memory blocks up to 2,048 words deep. Each ESB can implement a 2,048-word-deep memory; the ESBs are used in parallel, eliminating the need for any external control logic and its associated delays.

To create a high-speed memory block that is more than 2,048 words deep, ESBs drive tri-state lines. Each tri-state line connects all ESBs in a column of MegaLAB structures, and drives the MegaLAB interconnect and row and column FastTrack interconnect throughout the column. Each ESB incorporates a programmable decoder to activate the tri-state driver appropriately. For instance, to implement 8,192-word-deep memory, four ESBs are used. Eleven address lines drive the ESB memory, and two more drive the tri-state decoder. Depending on which 2,048-word memory page is selected, the appropriate ESB driver is turned on, driving the output to the tri-state line. The Quartus II software automatically combines ESBs with tri-state lines to form deeper memory blocks. The internal tri-state control logic is designed to avoid internal contention and floating lines. See Figure 18.

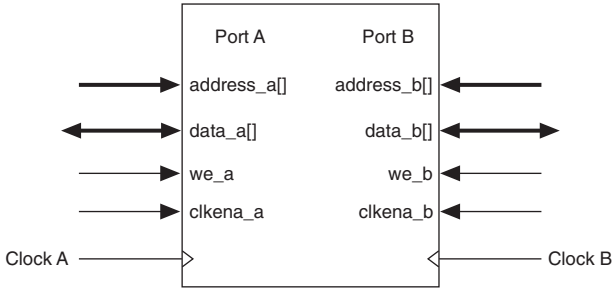
*Figure 18. Deep Memory Block Implemented with Multiple ESBs*




The ESB implements two forms of dual-port memory: read/write clock mode and input/output clock mode. The ESB can also be used for bidirectional, dual-port memory applications in which two ports read or write simultaneously. To implement this type of dual-port memory, two ESBs are used to support two simultaneous reads or writes.

The ESB can also use Altera megafunctions to implement dual-port RAM applications where both ports can read or write, as shown in Figure 19.

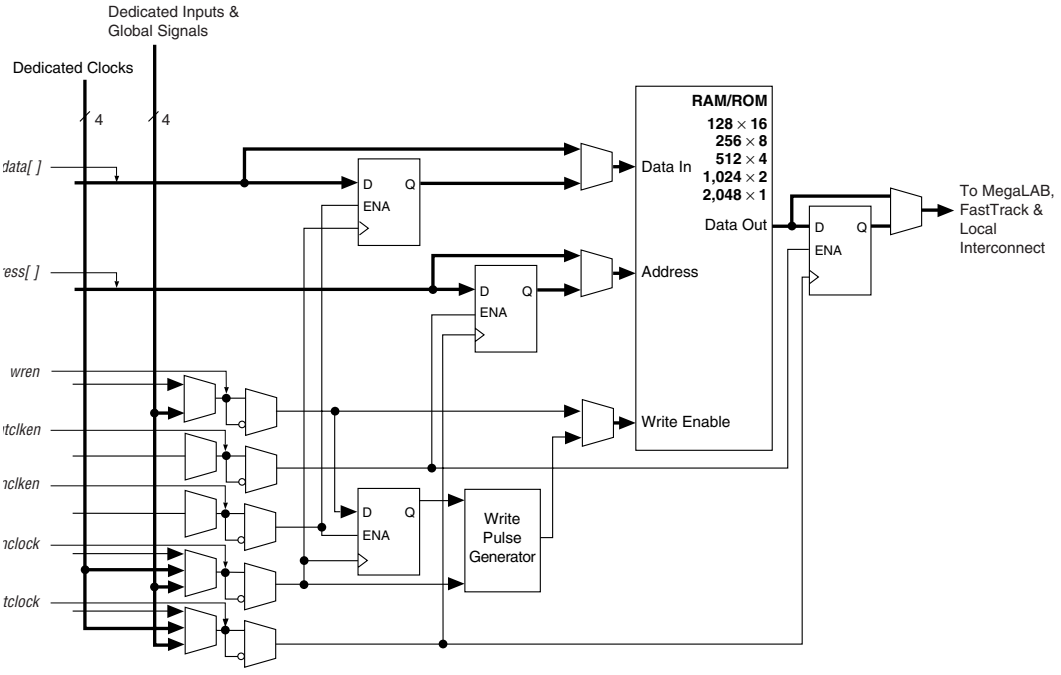
*Figure 19. APEX 20KC ESB Implementing Dual-Port RAM*



## Read/Write Clock Mode

The read/write clock mode contains two clocks. One clock controls all registers associated with writing: data input, WE, and write address. The other clock controls all registers associated with reading: read enable (RE), read address, and data output. The ESB also supports clock enable and asynchronous clear signals; these signals also control the read and write registers independently. Read/write clock mode is commonly used for applications where reads and writes occur at different system frequencies. Figure 20 shows the ESB in read/write clock mode.

***Figure 20. ESB in Read/Write Clock Mode*** *Note (1)*



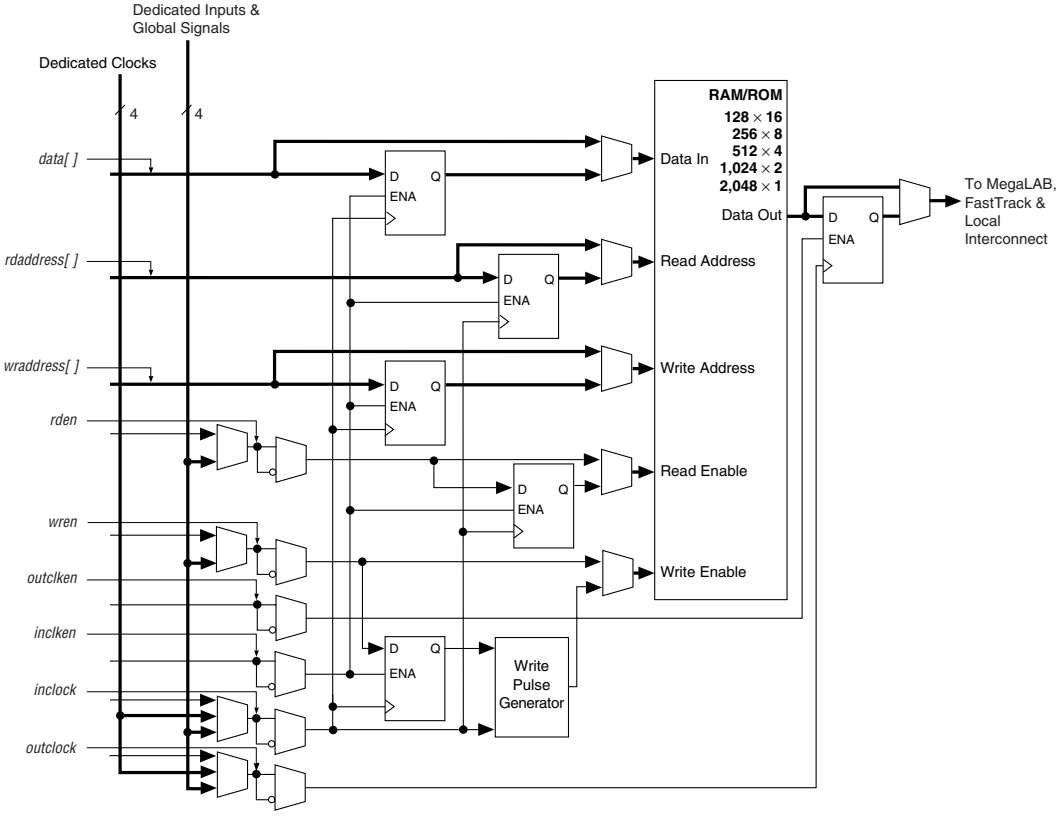

*Note to Figure 20:*

(1) All registers can be cleared asynchronously by ESB local interconnect signals, global signals, or the chip-wide reset.

## Input/Output Clock Mode

The input/output clock mode contains two clocks. One clock controls all registers for inputs into the ESB: data input, WE, RE, read address, and write address. The other clock controls the ESB data output registers. The ESB also supports clock enable and asynchronous clear signals; these signals also control the reading and writing of registers independently. Input/output clock mode is commonly used for applications where the reads and writes occur at the same system frequency, but require different clock enable signals for the input and output registers. Figure 21 shows the ESB in input/output clock mode.

***Figure 21. ESB in Input/Output Clock Mode*** *Note (1)*



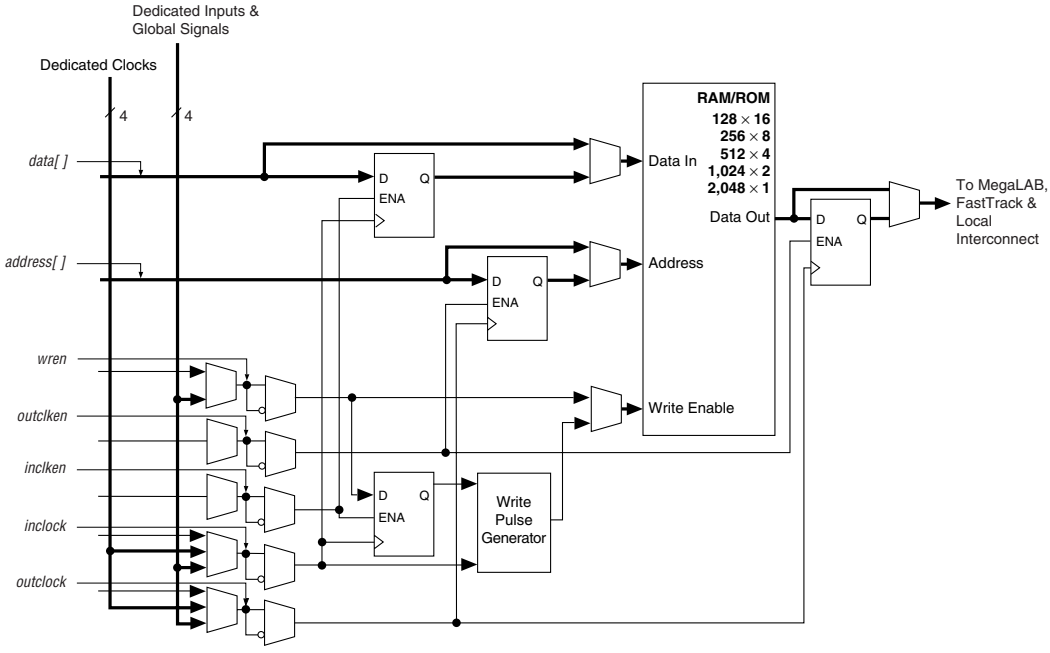

*Note to Figure 21:*

(1) All registers can be cleared asynchronously by ESB local interconnect signals, global signals, or the chip-wide reset.

## Single-Port Mode

The APEX 20KC ESB also supports a single-port mode, which is used when simultaneous reads and writes are not required. See Figure 22.

*Figure 22. ESB in Single-Port Mode* *Note (1)*




*Note to Figure 22:*

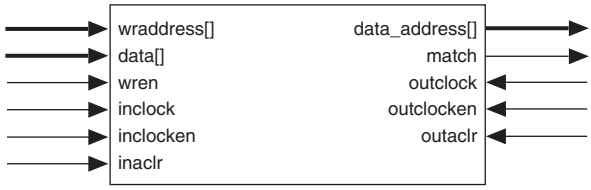
(1) All registers can be asynchronously cleared by ESB local interconnect signals, global signals, or the chip-wide reset.

## Content-Addressable Memory

In APEX 20KC devices, the ESB can implement CAM. CAM can be thought of as the inverse of RAM. When read, RAM outputs the data for a given address. Conversely, CAM outputs an address for a given data word. For example, if the data `FA12` is stored in address `14`, the CAM outputs `14` when `FA12` is driven into it.

CAM is used for high-speed search operations. When searching for data within a RAM block, the search is performed serially. Thus, finding a particular data word can take many cycles. CAM searches all addresses in parallel and outputs the address storing a particular word. When a match is found, a match flag is set high. Figure 23 shows the CAM block diagram.

*Figure 23. APEX 20KC CAM Block Diagram*




CAM can be used in any application requiring high-speed searches, such as networking, communications, data compression, and cache management.

The APEX 20KC on-chip CAM provides faster system performance than traditional discrete CAM. Integrating CAM and logic into the APEX 20KC device eliminates off-chip and on-chip delays, improving system performance.

When in CAM mode, the ESB implements 32-word, 32-bit CAM. Wider or deeper CAM can be implemented by combining multiple CAMs with some ancillary logic implemented in LEs. The Quartus II software combines ESBs and LEs automatically to create larger CAMs.

CAM supports writing "don't care" bits into words of the memory. The "don't care" bit can be used as a mask for CAM comparisons; any bit set to "don't care" has no effect on matches.

The output of the CAM can be encoded or unencoded. When encoded, the ESB outputs an encoded address of the data's location. For instance, if the data is located in address `12`, the ESB output is `12`. When unencoded, the ESB uses its 16 outputs to show the location of the data over two clock cycles. In this case, if the data is located in address `12`, the 12th output line goes high. When using unencoded outputs, two clock cycles are required to read the output because a 16-bit output bus is used to show the status of 32 words.

The encoded output is better suited for designs that ensure duplicate data is not written into the CAM. If duplicate data is written into two locations, the CAM's output will be incorrect. If the CAM may contain duplicate data, the unencoded output is a better solution; CAM with unencoded outputs can distinguish multiple data locations.

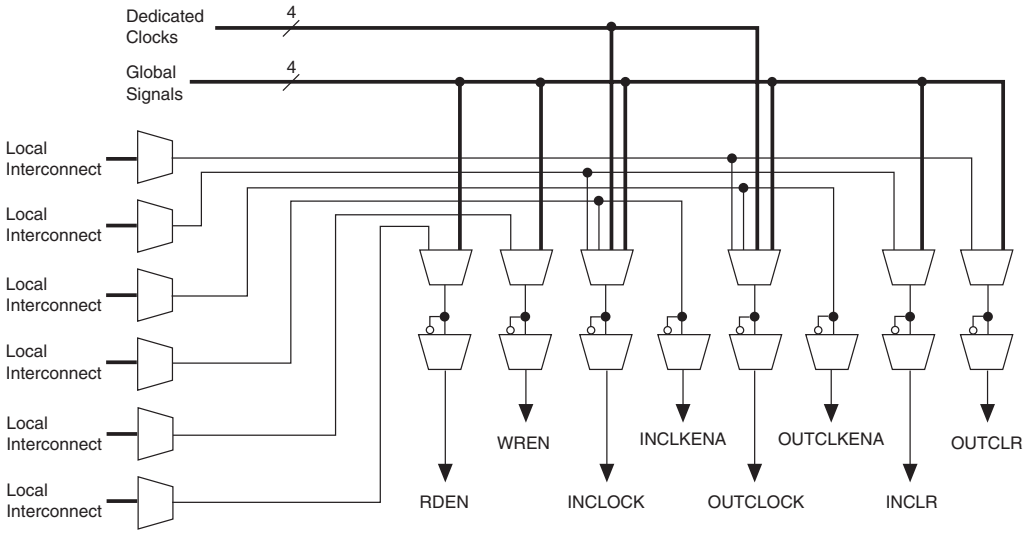
CAM can be pre-loaded with data during configuration, or it can be written during system operation. In most cases, two clock cycles are required to write each word into CAM. When "don't care" bits are used, a third clock cycle is required.

For more information on APEX 20KC devices and CAM, see *Application Note 119 (Implementing High-Speed Search Applications with APEX CAM).*

## Driving Signals to the ESB

ESBs provide flexible options for driving control signals. Different clocks can be used for the ESB inputs and outputs. Registers can be inserted independently on the data input, data output, read address, write address, WE, and RE signals. The global signals and the local interconnect can drive the WE and RE signals. The global signals, dedicated clock pins, and local interconnect can drive the ESB clock signals. Because the LEs drive the local interconnect, the LEs can control the WE and RE signals and the ESB clock, clock enable, and asynchronous clear signals. Figure 24 shows the ESB control signal generation logic.

*Figure 24. ESB Control Signal Generation*




An ESB is fed by the local interconnect, which is driven by adjacent LEs (for high-speed connection to the ESB) or the MegaLAB interconnect. The ESB can drive the local, MegaLAB, or FastTrack interconnect routing structure to drive LEs and IOEs in the same MegaLAB structure or anywhere in the device.

### Implementing Logic in ROM

In addition to implementing logic with product terms, the ESB can implement logic functions when it is programmed with a read-only pattern during configuration, creating a large LUT. With LUTs, combinatorial functions are implemented by looking up the results, rather than by computing them. This implementation of combinatorial functions can be faster than using algorithms implemented in general logic, a performance advantage that is further enhanced by the fast access times of ESBs. The large capacity of ESBs enables designers to implement complex functions in one logic level without the routing delays associated with linked LEs or distributed RAM blocks. Parameterized functions such as LPM functions can take advantage of the ESB automatically. Further, the Quartus II software can implement portions of a design with ESBs where appropriate.

### Programmable Speed/Power Control

APEX 20KC ESBs offer a high-speed mode that supports very fast operation on an ESB-by-ESB basis. When high speed is not required, this feature can be turned off to reduce the ESB's power dissipation by up to 50%. ESBs that run at low power incur a nominal timing delay adder. This Turbo Bit™ option is available for ESBs that implement product-term logic or memory functions. An ESB that is not used will be powered down so that it does not consume DC current.

Designers can program each ESB in the APEX 20KC device for either high-speed or low-power operation. As a result, speed-critical paths in the design can run at high speed, while the remaining paths operate at reduced power.

## I/O Structure

The APEX 20KC IOE contains a bidirectional I/O buffer and a register that can be used either as an input register for external data requiring fast setup times or as an output register for data requiring fast clock-to-output performance. IOEs can be used as input, output, or bidirectional pins.

APEX 20KC devices include an enhanced IOE, which drives the FastRow interconnect. The FastRow interconnect connects a column I/O pin directly to the LAB local interconnect within two MegaLAB structures. This feature provides fast setup times for pins that drive high fan-outs with complex logic, such as PCI designs. For fast bidirectional I/O timing, LE registers using local routing can improve setup times and OE timing. The APEX 20KC IOE also includes direct support for open-drain operation, giving faster clock-to-output for open-drain signals. Some programmable delays in the APEX 20KC IOE offer multiple levels of delay to fine-tune setup and hold time requirements. The Quartus II Compiler sets these delays by default to minimize setup time while providing a zero hold time.

The Quartus II Compiler uses the programmable inversion option to invert signals from the row and column interconnect automatically where appropriate. Because the APEX 20KC IOE offers one output enable per pin, the Quartus II Compiler can emulate open-drain operation efficiently.

The APEX 20KC IOE includes programmable delays that can be activated to ensure zero hold times, minimum clock-to-output times, input IOE register-to-core register transfers, or core-to-output IOE register transfers. A path in which a pin directly drives a register may require the delay to ensure zero hold time, whereas a path in which a pin drives a register through combinatorial logic may not require the delay.

Table 9 describes the APEX 20KC programmable delays and their logic options in the Quartus II software.

*Table 9. APEX 20KC Programmable Delay Chains*

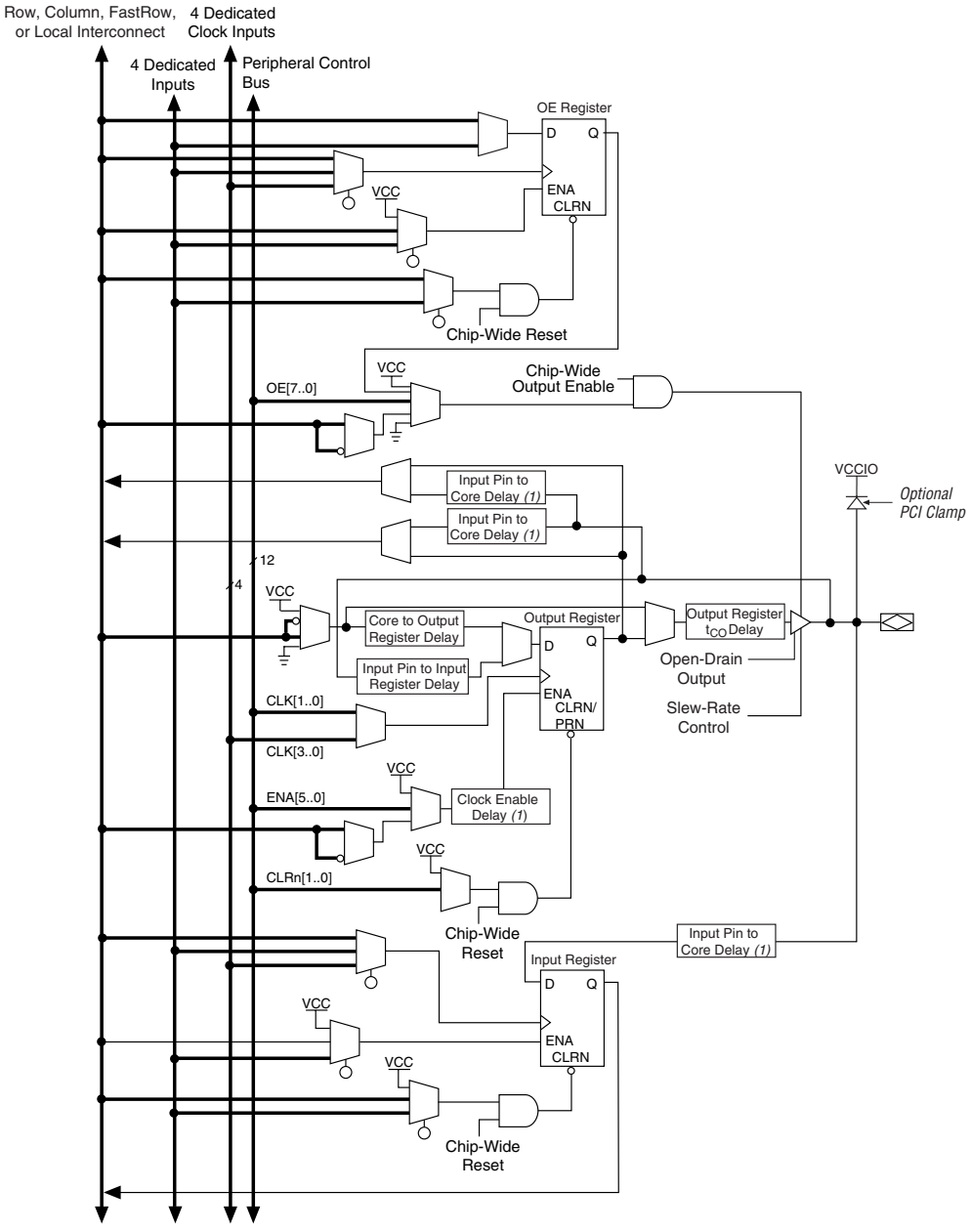
| Programmable Delay | Quartus II Logic Option |
|---|---|
| Input pin to core delay | Decrease input delay to internal cells |
| Input pin to input register delay | Decrease input delay to input registers |
| Core to output register delay | Decrease input delay to output register |
| Output register $t_{CO}$ delay | Increase delay to output pin |
| Clock enable delay | Increase clock enable delay |

The Quartus II Compiler can program these delays automatically to minimize setup time while providing a zero hold time.

The register in the APEX 20KC IOE can be programmed to power-up high or low after configuration is complete. If it is programmed to power-up low, an asynchronous clear can control the register. If it is programmed to power-up high, an asynchronous preset can control the register. This feature is useful for cases where the APEX 20KC device controls an active-low input or another device; it prevents inadvertent activation of the input upon power-up.

Figure 25 shows how fast bidirectional I/O pins are implemented in APEX 20KC devices. This feature is useful for cases where the APEX 20KC device controls an active-low input or another device; it prevents inadvertent activation of the input upon power-up.

***Figure 25. APEX 20KC Bidirectional I/O Registers*** *Notes (1), (2)*



*Notes to Figure 25:*
(1) This programmable delay has four settings: off and three levels of delay.
(2) The output enable and input registers are LE registers in the LAB adjacent to the bidirectional pin.

Each IOE drives a row, column, MegaLAB, or local interconnect when used as an input or bidirectional pin. A row IOE can drive a local, MegaLAB, row, and column interconnect; a column IOE can drive the column interconnect. Figure 26 shows how a row IOE connects to the interconnect.

***Figure 26. Row IOE Connection to the Interconnect***

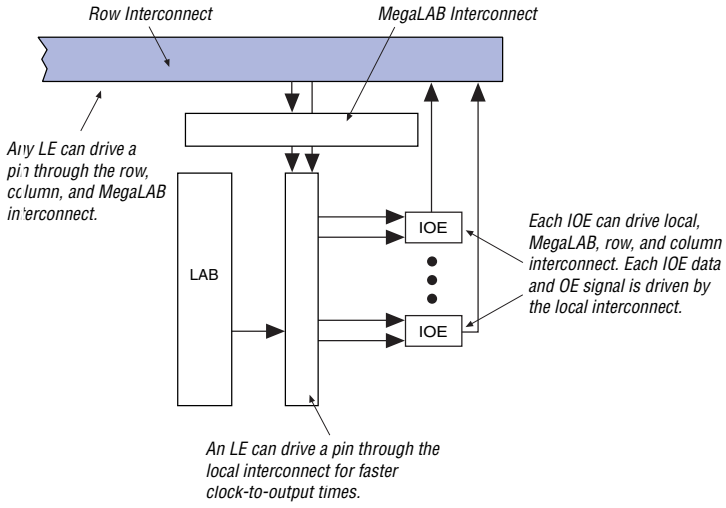
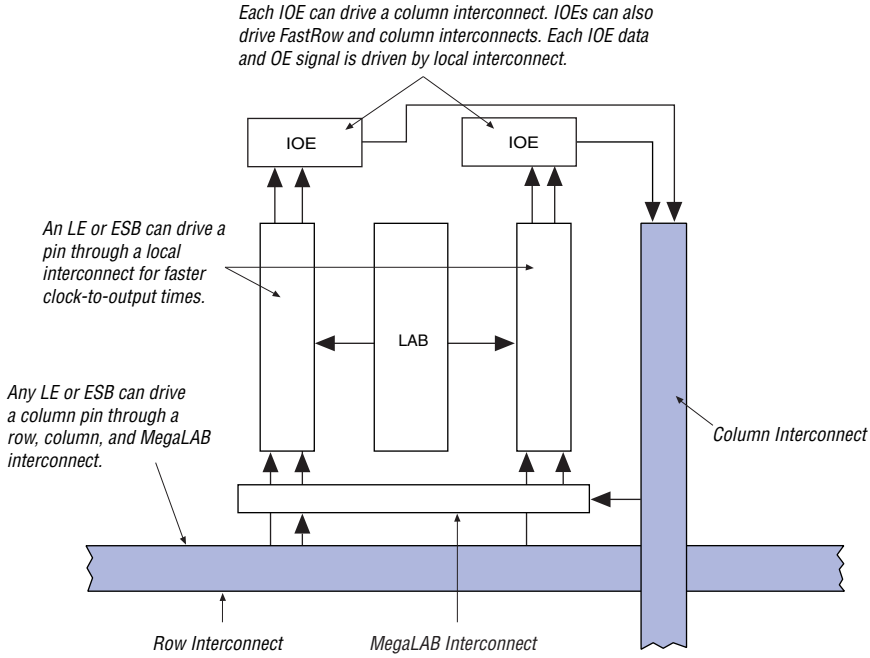


Figure 27 shows how a column IOE connects to the interconnect.

*Figure 27. Column IOE Connection to the Interconnect*




## Dedicated Fast I/O Pins

APEX 20KC devices incorporate an enhancement to support bidirectional pins with high internal fan-out such as PCI control signals. These pins are called dedicated fast I/O pins (`FAST1`, `FAST2`, `FAST3`, and `FAST4`) and replace dedicated inputs. These pins can be used for fast clock, clear, or high fan-out logic signal distribution. They also can drive out. The dedicated fast I/O pin data output and tri-state control are driven by local interconnect from the adjacent MegaLAB for high speed.

## Advanced I/O Standard Support

APEX 20KC IOEs support the following I/O standards: LVTTL, LVCMOS, 1.8-V I/O, 2.5-V I/O, 3.3-V PCI, PCI-X, 3.3-V AGP, LVDS, LVPECL, GTL+, CTT, HSTL Class I, SSTL-3 Class I and II, and SSTL-2 Class I and II.

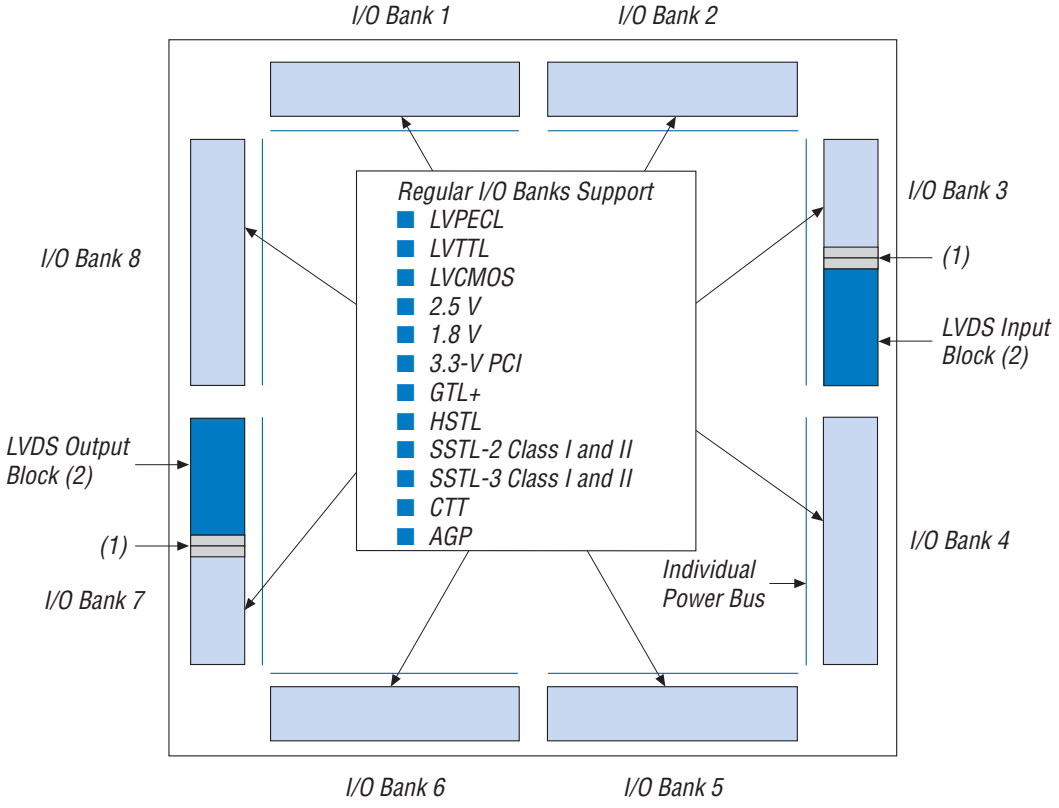
For more information on I/O standards supported by APEX 20KC devices, see *Application Note 117 (Using Selectable I/O Standards in Altera Devices)*.

The APEX 20KC device contains eight I/O banks. In QFP packages, the banks are linked to form four I/O banks. The I/O banks directly support all standards except LVDS and LVPECL. All I/O banks can support LVDS and LVPECL at up to 156 Mbps per channel with the addition of external resistors. In addition, one block within a bank contains circuitry to support high-speed True-LVDS and LVPECL inputs, and another block within a bank supports high-speed True-LVDS and LVPECL outputs. The LVDS blocks support all of the I/O standards. Each I/O bank has its own VCCIO pins. A single device can support 1.8-V, 2.5-V, and 3.3-V interfaces; each bank can support a different standard independently. Each bank can also use a separate $V_{REF}$ level so that each bank can support any of the terminated standards (such as SSTL-3) independently. Within a bank, any one of the terminated standards can be supported. EP20K400C and larger APEX 20KC devices support the LVDS interface for data pins (EP20K200C devices support LVDS clock pins, but not data pins). EP20K400C and EP20K600C devices support LVDS for data pins at up to 840 Mbps per channel. EP20K1000C devices support LVDS on 16 channels at up to 750 Mbps.

Each bank can support multiple standards with the same VCCIO for output pins. Each bank can support one voltage-referenced I/O standard, but it can support multiple I/O standards with the same VCCIO voltage level. For example, when VCCIO is 3.3 V, a bank can support LVTTL, LVCMOS, 3.3-V PCI, and SSTL-3 for inputs and outputs.

When the LVDS banks are not used for the LVDS I/O standard, they support all of the other I/O standards. Figure 28 shows the arrangement of the APEX 20KC I/O banks.

*Figure 28. APEX 20KC I/O Banks*




*Notes to Figure 28:*

(1) For more information on placing I/O pins in LVDS blocks, refer to the "Guidelines for Using LVDS Blocks" section in *Application Note 120 (Using LVDS in APEX 20KE Devices)*.

(2) If the LVDS input and output blocks are not used for LVDS, they can support all of the I/O standards and can be used as input, output, or bidirectional pins with $V_{CCIO}$ set to 3.3 V, 2.5 V, or 1.8 V.

## Power Sequencing & Hot Socketing

Because APEX 20KC devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. Therefore, the $V_{CCIO}$ and $V_{CCINT}$ power supplies may be powered in any order.

Signals can be driven into APEX 20KC devices before and during power-up without damaging the device. In addition, APEX 20KC devices do not drive out during power-up. Once operating conditions are reached and the device is configured, APEX 20KC devices operate as specified by the user.

## MultiVolt I/O Interface

The APEX architecture supports the MultiVolt I/O interface feature, which allows APEX devices in all packages to interface with systems of different supply voltages. The devices have one set of VCC pins for internal operation and input buffers (VCCINT), and another set for I/O output drivers (VCCIO).

APEX 20KC devices support the MultiVolt I/O interface feature. The APEX 20KC VCCINT pins must always be connected to a 1.8-V power supply. With a 1.8-V $V_{CCINT}$ level, input pins are 1.8-V, 2.5-V, and 3.3-V tolerant. The VCCIO pins can be connected to either a 1.8-V, 2.5-V, or 3.3-V power supply, depending on the I/O standard requirements. When the VCCIO pins are connected to a 1.8-V power supply, the output levels are compatible with 1.8-V systems. When VCCIO pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When VCCIO pins are connected to a 3.3-V power supply, the output high is 3.3 V and compatible with 3.3-V or 5.0-V systems. An APEX 20KC device is 5.0-V tolerant with the addition of a resistor and the PCI clamp diode enabled.

For more information on 5.0-V tolerance, refer to the "5.0-V Tolerance in APEX 20KE Devices White Paper," as the information found therein also applies to APEX 20KC devices.

Table 10 summarizes APEX 20KC MultiVolt I/O support.

*Table 10. APEX 20KC MultiVolt I/O Support*

| $V_{CCIO}$ (V) | Input Signals (V) | | | | Output Signals (V) | | | |
|---|---|---|---|---|---|---|---|---|
| | 1.8 | 2.5 | 3.3 | 5.0 | 1.8 | 2.5 | 3.3 | 5.0 |
| 1.8 | ✓ | ✓ *(1)* | ✓ *(1)* | | ✓ | | | |
| 2.5 | | ✓ | ✓ *(1)* | | | ✓ | | |
| 3.3 | | ✓ | ✓ | ✓ *(2)* | | ✓ *(3)* | ✓ | ✓ |

*Notes to Table 10:*

(1) The PCI clamping diode must be disabled to drive an input with voltages higher than $V_{CCIO}$, except for the 5.0-V input case.

(2) An APEX 20KC device can be made 5.0-V tolerant with the addition of an external resistor and the PCI clamp diode enabled.

(3) When $V_{CCIO}$ = 3.3 V, an APEX 20KC device can drive a 2.5-V device with 3.3-V tolerant inputs.

Open-drain output pins on APEX 20KC devices (with a series resistor and a pull-up resistor to the 5.0-V supply) can drive 5.0-V CMOS input pins that require a $V_{IH}$ of 3.5 V. When the pin is inactive, the trace will be pulled up to 5.0 V by the resistor. The open-drain pin will only drive low or tri-state; it will never drive high. The rise time is dependent on the value of the pull-up resistor and load impedance. The $I_{OL}$ current specification should be considered when selecting a pull-up resistor.

## ClockLock & ClockBoost Features

APEX 20KC devices support the ClockLock and ClockBoost clock management features, which are implemented with PLLs. The ClockLock circuitry uses a synchronizing PLL that reduces the clock delay and skew within a device. This reduction minimizes clock-to-output and setup times while maintaining zero hold times. The ClockBoost circuitry, which provides a clock multiplier, allows the designer to enhance device area efficiency by sharing resources within the device. The ClockBoost circuitry allows the designer to distribute a low-speed clock and multiply that clock on-device. APEX 20KC devices include a high-speed clock tree; unlike ASICs, the user does not have to design and optimize the clock tree. The ClockLock and ClockBoost features work in conjunction with the APEX 20KC device's high-speed clock to provide significant improvements in system performance and bandwidth. APEX 20KC devices in -7 and -8 speed grades have PLLs and support the ClockLock and ClockBoost features.

The ClockLock and ClockBoost features in APEX 20KC devices are enabled through the Quartus II software. External devices are not required to use these features.

### APEX 20KC ClockLock Feature

APEX 20KC devices include up to four PLLs, which can be used independently. Two PLLs are designed for either general-purpose use or LVDS use (on devices that support LVDS I/O pins). The remaining two PLLs are designed for general-purpose use. The EP20K200C devices have two PLLs; the EP20K400C and larger devices have four PLLs.

The following sections describe some of the features offered by the APEX 20KC PLLs.

#### *External PLL Feedback*

The ClockLock circuit's output can be driven off-chip to clock other devices in the system; further, the feedback loop of the PLL can be routed off-chip. This feature allows the designer to exercise fine control over the I/O interface between the APEX 20KC device and another high-speed device, such as SDRAM.

### *Clock Multiplication*

The APEX 20KC ClockBoost circuit can multiply or divide clocks by a programmable number. The clock can be multiplied by $m/(n \times k)$, where $m$ and $k$ range from 2 to 160 and $n$ ranges from 1 to 16. Clock multiplication and division can be used for time-domain multiplexing and other functions, which can reduce design LE requirements.

### *Clock Phase & Delay Adjustment*

The APEX 20KC ClockShift feature allows the clock phase and delay to be adjusted. The clock phase can be adjusted by 90° steps. The clock delay can be adjusted to increase or decrease the clock delay by an arbitrary amount, up to one clock period.

### *LVDS Support*

All APEX 20KC devices support differential LVDS buffers on the input and output clock signals that interface with external devices. This is controlled in the Quartus II software by assigning the clock pins with an LVDS I/O standard assignment.

Two high-speed PLLs are designed to support the LVDS interface. When using LVDS, the I/O clock runs at a slower rate than the data transfer rate. Thus, PLLs are used to multiply the I/O clock internally to capture the LVDS data. For example, an I/O clock may run at 105 MHz to support 840 Mbps LVDS data transfer. In this example, the PLL multiplies the incoming clock by eight to support the high-speed data transfer. You can use PLLs in EP20K400C and larger devices for high-speed LVDS interfacing.

### *Lock Signals*

The APEX 20KC ClockLock circuitry supports individual `LOCK` signals. The `LOCK` signal drives high when the ClockLock circuit has locked onto the input clock. The `LOCK` signals are optional for each ClockLock circuit; when not used, they are I/O pins.

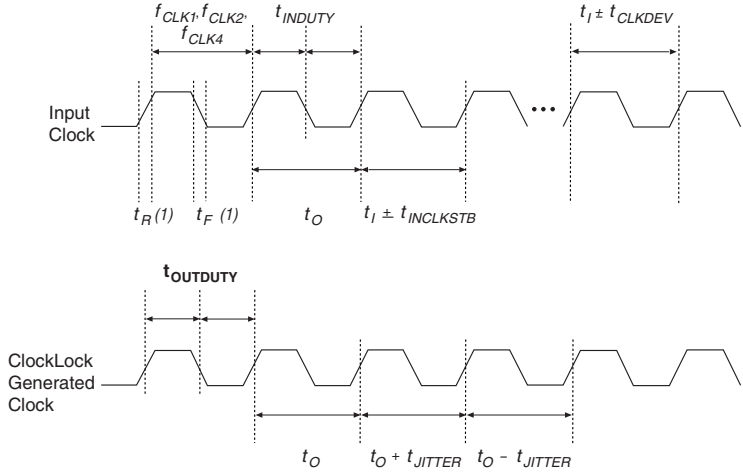
## ClockLock & ClockBoost Timing Parameters

For the ClockLock and ClockBoost circuitry to function properly, the incoming clock must meet certain requirements. If these specifications are not met, the circuitry may not lock onto the incoming clock, which generates an erroneous clock within the device. The clock generated by the ClockLock and ClockBoost circuitry must also meet certain specifications. If the incoming clock meets these requirements during configuration, the APEX 20KC ClockLock and ClockBoost circuitry will lock onto the clock during configuration. The circuit will be ready for use immediately after configuration. In APEX 20KC devices, the clock input standard is programmable, so the PLL cannot respond to the clock until the device is configured. The PLL locks onto the input clock as soon as configuration is complete. Figure 29 shows the incoming and generated clock specifications.

For more information on ClockLock and ClockBoost circuitry, see *Application Note 115: Using the ClockLock and ClockBoost PLL Features in APEX Devices*.

***Figure 29. Specifications for the Incoming & Generated Clocks***

*The $t_I$ parameter refers to the nominal input clock period; the $t_O$ parameter refers to the nominal output clock period.*




***Note to Figure 29:***

(1) Rise and fall times are measured from 10% to 90%.

Tables 11 and 12 summarize the ClockLock and ClockBoost parameters for APEX 20KC devices.

*Table 11. APEX 20KC ClockLock & ClockBoost Parameters* *Note (1)*

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_R$ | Input rise time | | | | 5 | ns |
| $t_F$ | Input fall time | | | | 5 | ns |
| $t_{INDUTY}$ | Input duty cycle | | 40 | | 60 | % |
| $t_{INJITTER}$ | Input jitter peak-to-peak | | | | 2% of input period | % |
| $t_{OUTJITTER}$ | RMS jitter on ClockLock or ClockBoost-generated clock | | | | 0.35% of output period | % |
| $t_{OUTDUTY}$ | Duty cycle for ClockLock or ClockBoost-generated clock | | 45 | | 55 | % |
| $t_{LOCK}$ (2), (3) | Time required for ClockLock or ClockBoost to acquire lock | | | | 40 | µs |

*Table 12. APEX 20KC Clock Input & Output Parameters (Part 1 of 2)* *Note (1)*

| Symbol | Parameter | I/O Standard | -7 Speed Grade | | -8 Speed Grade | | Units |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| $f_{VCO}$ (4) | Voltage controlled oscillator operating range | | 200 | 500 | 200 | 500 | MHz |
| $f_{CLOCK0}$ | Clock0 PLL output frequency for internal use | | 1.5 | 335 | 1.5 | 200 | MHz |
| $f_{CLOCK1}$ | Clock1 PLL output frequency for internal use | | 20 | 335 | 20 | 200 | MHz |
| $f_{CLOCK0\_EXT}$ | Output clock frequency for external clock0 output | 3.3-V LVTTL | (5) | (5) | (5) | (5) | MHz |
| | | 2.5-V LVTTL | (5) | (5) | (5) | (5) | MHz |
| | | 1.8-V LVTTL | (5) | (5) | (5) | (5) | MHz |
| | | GTL+ | (5) | (5) | (5) | (5) | MHz |
| | | SSTL-2 Class I | (5) | (5) | (5) | (5) | MHz |
| | | SSTL-2 Class II | (5) | (5) | (5) | (5) | MHz |
| | | SSTL-3 Class I | (5) | (5) | (5) | (5) | MHz |
| | | SSTL-3 Class II | (5) | (5) | (5) | (5) | MHz |
| | | LVDS | (5) | (5) | (5) | (5) | MHz |

*Table 12. APEX 20KC Clock Input & Output Parameters (Part 2 of 2)* *Note (1)*

| Symbol | Parameter | I/O Standard | -7 Speed Grade | | -8 Speed Grade | | Units |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| $f_{CLOCK1\_EXT}$ | Output clock frequency for external clock1 output | 3.3-V LVTTL | *(5)* | *(5)* | *(5)* | *(5)* | MHz |
| | | 2.5-V LVTTL | *(5)* | *(5)* | *(5)* | *(5)* | MHz |
| | | 1.8-V LVTTL | *(5)* | *(5)* | *(5)* | *(5)* | MHz |
| | | GTL+ | *(5)* | *(5)* | *(5)* | *(5)* | MHz |
| | | SSTL-2 Class I | *(5)* | *(5)* | *(5)* | *(5)* | MHz |
| | | SSTL-2 Class II | *(5)* | *(5)* | *(5)* | *(5)* | MHz |
| | | SSTL-3 Class I | *(5)* | *(5)* | *(5)* | *(5)* | MHz |
| | | SSTL-3 Class II | *(5)* | *(5)* | *(5)* | *(5)* | MHz |
| | | LVDS | *(5)* | *(5)* | *(5)* | *(5)* | MHz |
| $f_{IN}$ | Input clock frequency | 3.3-V LVTTL | *(5)* | *(5)* | *(5)* | *(5)* | MHz |
| | | 2.5-V LVTTL | *(5)* | *(5)* | *(5)* | *(5)* | MHz |
| | | 1.8-V LVTTL | *(5)* | *(5)* | *(5)* | *(5)* | MHz |
| | | GTL+ | *(5)* | *(5)* | *(5)* | *(5)* | MHz |
| | | SSTL-2 Class I | *(5)* | *(5)* | *(5)* | *(5)* | MHz |
| | | SSTL-2 Class II | *(5)* | *(5)* | *(5)* | *(5)* | MHz |
| | | SSTL-3 Class I | *(5)* | *(5)* | *(5)* | *(5)* | MHz |
| | | SSTL-3 Class II | *(5)* | *(5)* | *(5)* | *(5)* | MHz |
| | | LVDS | *(5)* | *(5)* | *(5)* | *(5)* | MHz |

***Notes to Tables 11 and 12:***

(1) All input clock specifications must be met. The PLL may not lock onto an incoming clock if the clock specifications are not met, creating an erroneous clock within the device.
(2) The maximum lock time is 40 µs or 2,000 input clock cycles, whichever occurs first.
(3) Before configuration, the PLL circuits are disable and powered down. During configuration, the PLLs remain disabled. The PLLs begin to lock once the device is in the user mode. If the clock enable feature is used, lock begins once the `CLKLK_ENA` pin goes high in user mode.
(4) The PLL VCO operating range is 200 MHz ≤ $f_{VCO}$ ≤ 840 MHz for LVDS mode.
(5) Contact Altera Applications for information on these parameters.

## SignalTap Embedded Logic Analyzer

APEX 20KC devices include device enhancements to support the SignalTap embedded logic analyzer. By including this circuitry, the APEX 20KC device provides the ability to monitor design operation over a period of time through the IEEE Std. 1149.1 (JTAG) circuitry; a designer can analyze internal logic at speed without bringing internal signals to the I/O pins. This feature is particularly important for advanced packages such as FineLine BGA packages because adding a connection to a pin during the debugging process can be difficult after a board is designed and manufactured.

## IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

All APEX 20KC devices provide JTAG BST circuitry that complies with the IEEE Std. 1149.1-1990 specification. JTAG boundary-scan testing can be performed before or after configuration, but not during configuration. APEX 20KC devices can also use the JTAG port for configuration with the Quartus II software or with hardware using either Jam Files (**.jam**) or Jam Byte-Code Files (**.jbc**). Finally, APEX 20KC devices use the JTAG port to monitor the logic operation of the device with the SignalTap embedded logic analyzer. APEX 20KC devices support the JTAG instructions shown in Table 13.

*Table 13. APEX 20KC JTAG Instructions*

| JTAG Instruction | Description |
|---|---|
| SAMPLE/PRELOAD | Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins. Also used by the SignalTap embedded logic analyzer. |
| EXTEST | Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins. |
| BYPASS | Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation. |
| USERCODE | Selects the 32-bit USERCODE register and places it between the TDI and TDO pins, allowing the USERCODE to be serially shifted out of TDO. |
| IDCODE | Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO. |
| ICR Instructions | Used when configuring an APEX 20KC device via the JTAG port with a MasterBlaster™ or ByteBlasterMV™ download cable, or when using a Jam File or Jam Byte-Code File via an embedded processor. |
| SignalTap Instructions | Monitors internal device operation with the SignalTap embedded logic analyzer. |

The APEX 20KC device instruction register length is 10 bits. The APEX 20KC device USERCODE register length is 32 bits. Tables 14 and 15 show the boundary-scan register length and device IDCODE information for APEX 20KC devices.

*Table 14. APEX 20KC Boundary-Scan Register Length*

| Device | Boundary-Scan Register Length |
|---|---|
| EP20K200C | 1,164 |
| EP20K400C | 1,506 |
| EP20K600C | 1,806 |
| EP20K1000C | 2,190 |

*Table 15. 32-Bit APEX 20KC Device IDCODE*

| Device | IDCODE (32 Bits) *(1)* | | | |
|---|---|---|---|---|
| | Version (4 Bits) | Part Number (16 Bits) | Manufacturer Identity (11 Bits) | 1 (1 Bit) *(2)* |
| EP20K200C | 0000 | 1000 0010 0000 0000 | 000 0110 1110 | 1 |
| EP20K400C | 0000 | 1000 0100 0000 0000 | 000 0110 1110 | 1 |
| EP20K600C | 0000 | 1000 0110 0000 0000 | 000 0110 1110 | 1 |
| EP20K1000C | 0000 | 1001 0000 0000 0000 | 000 0110 1110 | 1 |

*Notes to Table 15:*
(1) The most significant bit (MSB) is on the left.
(2) The IDCODE's least significant bit (LSB) is always 1.

Figure 30 shows the timing requirements for the JTAG signals.

*Figure 30. APEX 20KC JTAG Waveforms*

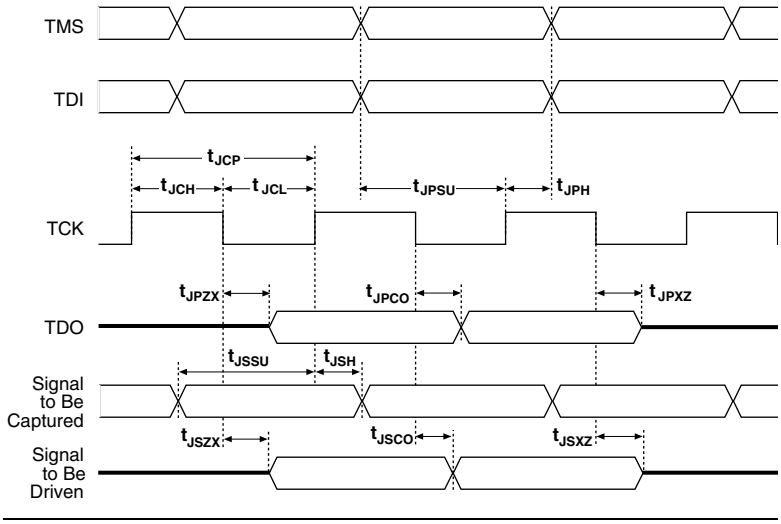



Table 16 shows the JTAG timing parameters and values for APEX 20KC devices.

*Table 16. APEX 20KC JTAG Timing Parameters & Values*

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{JCP}$ | TCK clock period | 100 | | ns |
| $t_{JCH}$ | TCK clock high time | 50 | | ns |
| $t_{JCL}$ | TCK clock low time | 50 | | ns |
| $t_{JPSU}$ | JTAG port setup time | 20 | | ns |
| $t_{JPH}$ | JTAG port hold time | 45 | | ns |
| $t_{JPCO}$ | JTAG port clock to output | | 25 | ns |
| $t_{JPZX}$ | JTAG port high impedance to valid output | | 25 | ns |
| $t_{JPXZ}$ | JTAG port valid output to high impedance | | 25 | ns |
| $t_{JSSU}$ | Capture register setup time | 20 | | ns |
| $t_{JSH}$ | Capture register hold time | 45 | | ns |
| $t_{JSCO}$ | Update register clock to output | | 35 | ns |
| $t_{JSZX}$ | Update register high impedance to valid output | | 35 | ns |
| $t_{JSXZ}$ | Update register valid output to high impedance | | 35 | ns |

For more information, see the following documents:

- *Application Note 39 (IEEE Std. 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)*

- *Jam Programming & Test Language Specification*

## Generic Testing

Each APEX 20KC device is functionally tested. Complete testing of each configurable SRAM bit and all logic functionality ensures 100% yield. AC test measurements for APEX 20KC devices are made under conditions equivalent to those defined in the "Timing Model" section on page 65. Multiple test patterns can be used to configure devices during all stages of the production flow. AC test criteria include:

- Power supply transients can affect AC measurements.
- Simultaneous transitions of multiple outputs should be avoided for accurate measurement.
- Threshold tests must not be performed under AC conditions.
- Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result.

## Operating Conditions

Tables 17 through 20 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for 1.8-V APEX 20KC devices.

*Table 17. APEX 20KC Device Absolute Maximum Ratings* *Note (1)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CCINT}$ | Supply voltage | With respect to ground *(2)* | –0.5 | 2.5 | V |
| $V_{CCIO}$ | | | –0.5 | 4.6 | V |
| $V_I$ | DC input voltage | | –0.5 | 4.6 | V |
| $I_{OUT}$ | DC output current, per pin | | –25 | 25 | mA |
| $T_{STG}$ | Storage temperature | No bias | –65 | 150 | ° C |
| $T_{AMB}$ | Ambient temperature | Under bias | –65 | 135 | ° C |
| $T_J$ | Junction temperature | PQFP, RQFP, TQFP, and BGA packages, under bias | | 135 | ° C |
| | | Ceramic PGA packages, under bias | | 150 | ° C |

*Table 18. APEX 20KC Device Recommended Operating Conditions*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CCINT}$ | Supply voltage for internal logic and input buffers | *(3)*, *(4)* | 1.71 (1.71) | 1.89 (1.89) | V |
| $V_{CCIO}$ | Supply voltage for output buffers, 3.3-V operation | *(3)*, *(4)* | 3.00 (3.00) | 3.60 (3.60) | V |
| | Supply voltage for output buffers, 2.5-V operation | *(3)*, *(4)* | 2.375 (2.375) | 2.625 (2.625) | V |
| | Supply voltage for output buffers, 1.8-V operation | *(3)*, *(4)* | 1.71 (1.71) | 1.89 (1.89) | V |
| $V_I$ | Input voltage | *(2)*, *(5)* | –0.5 | 4.1 | V |
| $V_O$ | Output voltage | | 0 | $V_{CCIO}$ | V |
| $T_J$ | Operating junction temperature | For commercial use | 0 | 85 | ° C |
| | | For industrial use | –40 | 100 | ° C |
| $t_R$ | Input rise time (10% to 90%) | | | 40 | ns |
| $t_F$ | Input fall time (90% to 10%) | | | 40 | ns |

*Table 19. APEX 20KC Device DC Operating Conditions* *Notes (6), (7)*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_I$ | Input pin leakage current *(8)* | $V_I$ = 3.6 to 0.0 V | –10 | | 10 | µA |
| $I_{OZ}$ | Tri-stated I/O pin leakage current *(8)* | $V_O$ = 4.1 to –0.5 V | –10 | | 10 | µA |
| $I_{CC0}$ | $V_{CC}$ supply current (standby) (All ESBs in power-down mode) | $V_I$ = ground, no load, no toggling inputs, -7 speed grade | | 10 | | mA |
| | | $V_I$ = ground, no load, no toggling inputs, -8, -9 speed grades | | 5 | | mA |
| $R_{CONF}$ | Value of I/O pin pull-up resistor before and during configuration | $V_{CCIO}$ = 3.0 V *(9)* | 20 | | 50 | kΩ |
| | | $V_{CCIO}$ = 2.375 V *(9)* | 30 | | 80 | kΩ |
| | | $V_{CCIO}$ = 1.71 V *(9)* | 60 | | 150 | kΩ |

DC operating specifications on APEX 20KC I/O standards are listed in Tables 21 to 35.

*Table 20. APEX 20KC Device Capacitance* *Note (10)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | $V_{IN}$ = 0 V, f = 1.0 MHz | | 8 | pF |
| $C_{INCLK}$ | Input capacitance on dedicated clock pin | $V_{IN}$ = 0 V, f = 1.0 MHz | | 12 | pF |
| $C_{OUT}$ | Output capacitance | $V_{OUT}$ = 0 V, f = 1.0 MHz | | 8 | pF |

***Notes to Tables 17 through 20:***

(1) See the *Operating Requirements for Altera Devices Data Sheet*.
(2) Minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 4.6 V for input currents less than 100 mA and time periods shorter than 20 ns.
(3) Numbers in parentheses are for industrial-temperature-range devices.
(4) Maximum $V_{CC}$ rise time is 100 ms, and $V_{CC}$ must rise monotonically.
(5) All pins, including dedicated inputs, clock, I/O, and JTAG pins, may be driven before $V_{CCINT}$ and $V_{CCIO}$ are powered.
(6) Typical values are for $T_A$ = 25° C, $V_{CCINT}$ = 1.8 V, and $V_{CCIO}$ = 1.8 V, 2.5 V or 3.3 V.
(7) These values are specified under the APEX 20KC device recommended operating conditions, shown in Table 18 on page 55.
(8) This value is specified for normal device operation. The value may vary during power-up.
(9) Pin pull-up resistance values will be lower if an external source drives the pin higher than $V_{CCIO}$.
(10) Capacitance is sample-tested only.

Tables 21 through 35 list the DC operating specifications for the supported I/O standards. These tables list minimal specifications only; APEX 20KC devices may exceed these specifications.

*Table 21. LVTTL I/O Specifications*

| Symbol | Parameter | Conditions | Minimum | Maximum | Units |
|---|---|---|---|---|---|
| $V_{CCIO}$ | Output supply voltage | | 3.0 | 3.6 | V |
| $V_{IH}$ | High-level input voltage | | 2.0 | $V_{CCIO}$ + 0.3 | V |
| $V_{IL}$ | Low-level input voltage | | –0.3 | 0.8 | V |
| $I_I$ | Input pin leakage current | $V_{IN}$ = 0 V or 3.3 V | –10 | 10 | µA |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = –12 mA, $V_{CCIO}$ = 3.0 V *(1)* | 2.4 | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 12 mA, $V_{CCIO}$ = 3.0 V *(2)* | | 0.4 | V |

*Table 22. LVCMOS I/O Specifications*

| Symbol | Parameter | Conditions | Minimum | Maximum | Units |
|---|---|---|---|---|---|
| $V_{CCIO}$ | Power supply voltage range | | 3.0 | 3.6 | V |
| $V_{IH}$ | High-level input voltage | | 2.0 | $V_{CCIO}$ + 0.3 | V |
| $V_{IL}$ | Low-level input voltage | | –0.3 | 0.8 | V |
| $I_I$ | Input pin leakage current | $V_{IN}$ = 0 V or 3.3 V | –10 | 10 | µA |
| $V_{OH}$ | High-level output voltage | $V_{CCIO}$ = 3.0 V<br>$I_{OH}$ = –0.1 mA *(1)* | $V_{CCIO}$ – 0.2 | | V |
| $V_{OL}$ | Low-level output voltage | $V_{CCIO}$ = 3.0 V<br>$I_{OL}$ = 0.1 mA *(2)* | | 0.2 | V |

*Table 23. 2.5-V I/O Specifications*

| Symbol | Parameter | Conditions | Minimum | Maximum | Units |
|---|---|---|---|---|---|
| $V_{CCIO}$ | Output supply voltage | | 2.375 | 2.625 | V |
| $V_{IH}$ | High-level input voltage | | 1.7 | $V_{CCIO}$ + 0.3 | V |
| $V_{IL}$ | Low-level input voltage | | –0.3 | 0.8 | V |
| $I_I$ | Input pin leakage current | $V_{IN}$ = 0 V or 3.3 V | –10 | 10 | µA |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = –0.1 mA *(1)* | 2.1 | | V |
| | | $I_{OH}$ = –1 mA *(1)* | 2.0 | | V |
| | | $I_{OH}$ = –2 mA *(1)* | 1.7 | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 0.1 mA *(2)* | | 0.2 | V |
| | | $I_{OL}$ = 1 mA *(2)* | | 0.4 | V |
| | | $I_{OL}$ = 2 mA *(2)* | | 0.7 | V |

*Table 24. 1.8-V I/O Specifications*

| Symbol | Parameter | Conditions | Minimum | Maximum | Units |
|---|---|---|---|---|---|
| $V_{CCIO}$ | Output supply voltage | | 1.7 | 1.9 | V |
| $V_{IH}$ | High-level input voltage | | 0.65 × $V_{CCIO}$ | $V_{CCIO}$ + 0.3 | V |
| $V_{IL}$ | Low-level input voltage | | | 0.35 × $V_{CCIO}$ | V |
| $I_I$ | Input pin leakage current | $V_{IN}$ = 0 V or 3.3 V | –10 | 10 | µA |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = –2 mA *(1)* | $V_{CCIO}$ – 0.45 | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 2 mA *(2)* | | 0.45 | V |

*Table 25. 3.3-V PCI Specifications*

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{CCIO}$ | I/O supply voltage | | 3.0 | 3.3 | 3.6 | V |
| $V_{IH}$ | High-level input voltage | | 0.5 × $V_{CCIO}$ | | $V_{CCIO}$ + 0.5 | V |
| $V_{IL}$ | Low-level input voltage | | –0.5 | | 0.3 × $V_{CCIO}$ | V |
| $I_I$ | Input pin leakage current | 0 < $V_{IN}$ < $V_{CCIO}$ | –10 | | 10 | µA |
| $V_{OH}$ | High-level output voltage | $I_{OUT}$ = –500 µA | 0.9 × $V_{CCIO}$ | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OUT}$ = 1,500 µA | | | 0.1 × $V_{CCIO}$ | V |

*Table 26. 3.3-V PCI-X Specifications*

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{CCIO}$ | Output supply voltage | | 3.0 | 3.3 | 3.6 | V |
| $V_{IH}$ | High-level input voltage | | 0.5 × $V_{CCIO}$ | | $V_{CCIO}$ + 0.5 | V |
| $V_{IL}$ | Low-level input voltage | | –0.5 | | 0.35 × $V_{CCIO}$ | V |
| $V_{IPU}$ | Input pull-up voltage | | 0.7 × $V_{CCIO}$ | | | V |
| $I_{IL}$ | Input pin leakage current | 0 < $V_{IN}$ < $V_{CCIO}$ | –10.0 | | 10.0 | µA |
| $V_{OH}$ | High-level output voltage | $I_{OUT}$ = –500 µA | 0.9 × $V_{CCIO}$ | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OUT}$ = 1,500 µA | | | 0.1 × $V_{CCIO}$ | V |
| $L_{pin}$ | Pin Inductance | | | | 15.0 | nH |

*Table 27. 3.3-V LVDS I/O Specifications*

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{CCIO}$ | I/O supply voltage | | 3.135 | 3.3 | 3.465 | V |
| $V_{OD}$ | Differential output voltage | $R_L$ = 100 Ω | 250 | | 650 | mV |
| Δ $V_{OD}$ | Change in $V_{OD}$ between high and low | $R_L$ = 100 Ω | | | 50 | mV |
| $V_{OS}$ | Output offset voltage | $R_L$ = 100 Ω | 1.125 | 1.25 | 1.375 | V |
| Δ $V_{OS}$ | Change in $V_{OS}$ between high and low | $R_L$ = 100 Ω | | | 50 | mV |
| $V_{TH}$ | Differential input threshold | $V_{CM}$ = 1.2 V | –100 | | 100 | mV |
| $V_{IN}$ | Receiver input voltage range | | 0.0 | | 2.4 | V |
| $R_L$ | Receiver differential input resistor (external to APEX devices) | | 90 | 100 | 110 | Ω |

*Table 28. GTL+ I/O Specifications*

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{TT}$ | Termination voltage | | 1.35 | 1.5 | 1.65 | V |
| $V_{REF}$ | Reference voltage | | 0.88 | 1.0 | 1.12 | V |
| $V_{IH}$ | High-level input voltage | | $V_{REF}$ + 0.1 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | $V_{REF}$ – 0.1 | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 36 mA *(2)* | | | 0.65 | V |

*Table 29. SSTL-2 Class I Specifications*

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{CCIO}$ | I/O supply voltage | | 2.375 | 2.5 | 2.625 | V |
| $V_{TT}$ | Termination voltage | | $V_{REF}$ – 0.04 | $V_{REF}$ | $V_{REF}$ + 0.04 | V |
| $V_{REF}$ | Reference voltage | | 1.15 | 1.25 | 1.35 | V |
| $V_{IH}$ | High-level input voltage | | $V_{REF}$ + 0.18 | | $V_{CCIO}$ + 0.3 | V |
| $V_{IL}$ | Low-level input voltage | | –0.3 | | $V_{REF}$ – 0.18 | V |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = –7.6 mA *(1)* | $V_{TT}$ + 0.57 | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 7.6 mA *(2)* | | | $V_{TT}$ – 0.57 | V |

*Table 30. SSTL-2 Class II Specifications*

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{CCIO}$ | I/O supply voltage | | 2.375 | 2.5 | 2.625 | V |
| $V_{TT}$ | Termination voltage | | $V_{REF}$ – 0.04 | $V_{REF}$ | $V_{REF}$ + 0.04 | V |
| $V_{REF}$ | Reference voltage | | 1.15 | 1.25 | 1.35 | V |
| $V_{IH}$ | High-level input voltage | | $V_{REF}$ + 0.18 | | $V_{CCIO}$ + 0.3 | V |
| $V_{IL}$ | Low-level input voltage | | –0.3 | | $V_{REF}$ – 0.18 | V |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = –15.2 mA *(1)* | $V_{TT}$ + 0.76 | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 15.2 mA *(2)* | | | $V_{TT}$ – 0.76 | V |

*Table 31. SSTL-3 Class I Specifications*

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{CCIO}$ | I/O supply voltage | | 3.0 | 3.3 | 3.6 | V |
| $V_{TT}$ | Termination voltage | | $V_{REF}$ – 0.05 | $V_{REF}$ | $V_{REF}$ + 0.05 | V |
| $V_{REF}$ | Reference voltage | | 1.3 | 1.5 | 1.7 | V |
| $V_{IH}$ | High-level input voltage | | $V_{REF}$ + 0.2 | | $V_{CCIO}$ + 0.3 | V |
| $V_{IL}$ | Low-level input voltage | | –0.3 | | $V_{REF}$ – 0.2 | V |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = –8 mA *(1)* | $V_{TT}$ + 0.6 | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 8 mA *(2)* | | | $V_{TT}$ – 0.6 | V |

*Table 32. SSTL-3 Class II Specifications*

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{CCIO}$ | I/O supply voltage | | 3.0 | 3.3 | 3.6 | V |
| $V_{TT}$ | Termination voltage | | $V_{REF}$ – 0.05 | $V_{REF}$ | $V_{REF}$ + 0.05 | V |
| $V_{REF}$ | Reference voltage | | 1.3 | 1.5 | 1.7 | V |
| $V_{IH}$ | High-level input voltage | | $V_{REF}$ + 0.2 | | $V_{CCIO}$ + 0.3 | V |
| $V_{IL}$ | Low-level input voltage | | –0.3 | | $V_{REF}$ – 0.2 | V |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = –16 mA *(1)* | $V_{TT}$ + 0.8 | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 16 mA *(2)* | | | $V_{TT}$ – 0.8 | V |

*Table 33. HSTL Class I I/O Specifications*

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{CCIO}$ | I/O supply voltage | | 1.71 | 1.8 | 1.89 | V |
| $V_{TT}$ | Termination voltage | | $V_{REF}$ – 0.05 | $V_{REF}$ | $V_{REF}$ + 0.05 | V |
| $V_{REF}$ | Reference voltage | | 0.68 | 0.75 | 0.90 | V |
| $V_{IH}$ | High-level input voltage | | $V_{REF}$ + 0.1 | | $V_{CCIO}$ + 0.3 | V |
| $V_{IL}$ | Low-level input voltage | | –0.3 | | $V_{REF}$ – 0.1 | V |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = –8 mA *(1)* | $V_{CCIO}$ – 0.4 | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 8 mA *(2)* | | | 0.4 | V |

*Table 34. 3.3-V AGP I/O Specifications*

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{CCIO}$ | I/O supply voltage | | 3.15 | 3.3 | 3.45 | V |
| $V_{REF}$ | Reference voltage | | 0.39 × $V_{CCIO}$ | | 0.41 × $V_{CCIO}$ | V |
| $V_{IH}$ | High-level input voltage | | 0.5 × $V_{CCIO}$ | | $V_{CCIO}$ + 0.5 | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.3 × $V_{CCIO}$ | V |
| $V_{OH}$ | High-level output voltage | $I_{OUT}$ = –500 µA | 0.9 × $V_{CCIO}$ | | 3.6 | V |
| $V_{OL}$ | Low-level output voltage | $I_{OUT}$ = 1,500 µA | | | 0.1 × $V_{CCIO}$ | V |
| $I_I$ | Input pin leakage current | 0 < $V_{IN}$ < $V_{CCIO}$ | –10 | | 10 | µA |

*Table 35. CTT I/O Specifications*

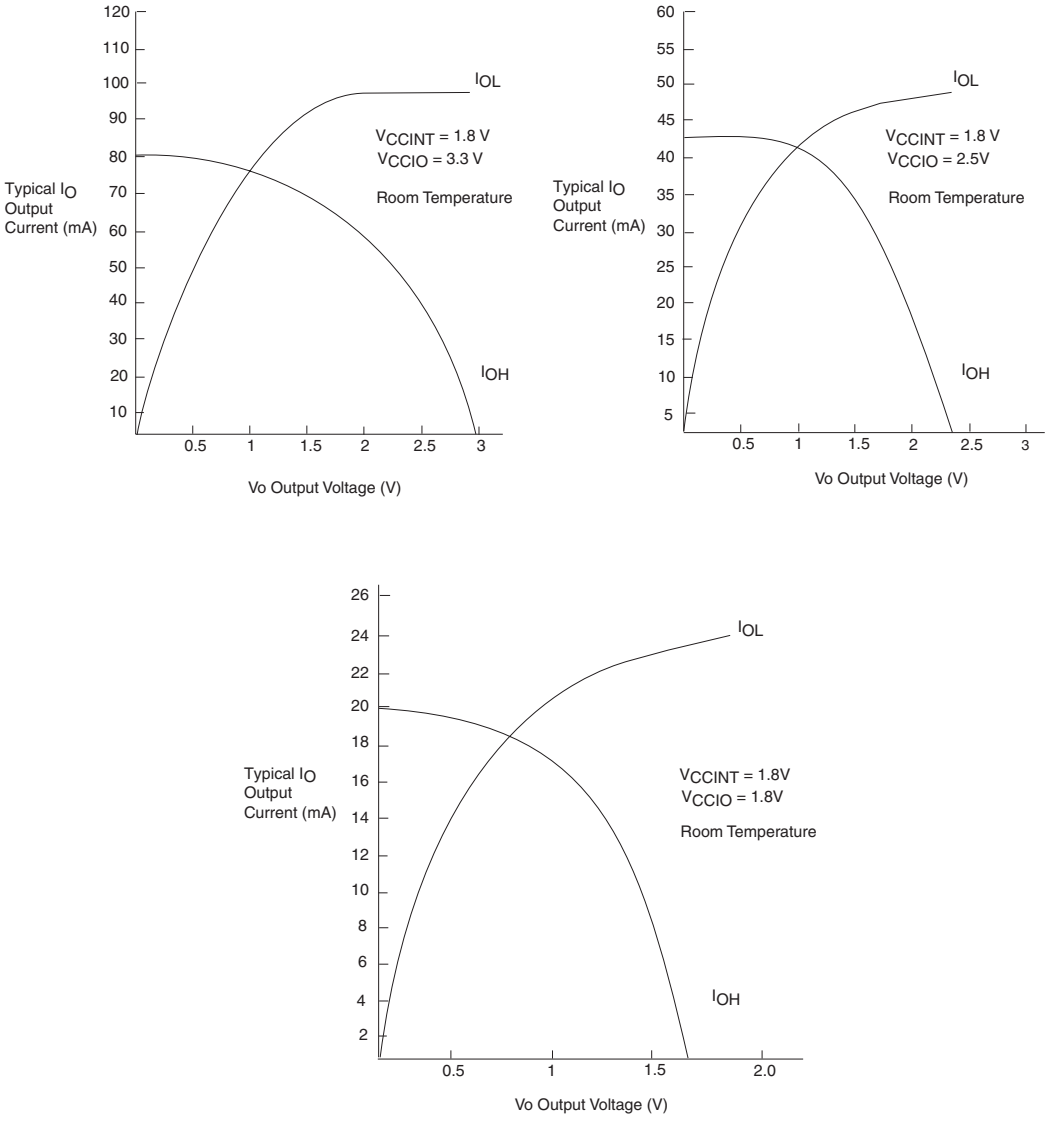
| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{CCIO}$ | I/O supply voltage | | 3.0 | 3.3 | 3.6 | V |
| $V_{TT}/V_{REF}$ *(3)* | Termination and reference voltage | | 1.35 | 1.5 | 1.65 | V |
| $V_{IH}$ | High-level input voltage | | $V_{REF}$ + 0.2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | $V_{REF}$ – 0.2 | V |
| $I_I$ | Input pin leakage current | 0 < $V_{IN}$ < $V_{CCIO}$ | –10 | | 10 | µA |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = –8 mA *(1)* | $V_{REF}$ + 0.4 | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 8 mA *(2)* | | | $V_{REF}$ – 0.4 | V |
| $I_O$ | Output leakage current (when output is high Z) | GND ≤ $V_{OUT}$ ≤ $V_{CCIO}$ | –10 | | 10 | µA |

***Notes to Tables 21 through 35:***

(1) The $I_{OH}$ parameter refers to high-level output current.
(2) The $I_{OL}$ parameter refers to low-level output current. This parameter applies to open-drain pins as well as output pins.
(3) $V_{REF}$ specifies center point of switching range.

Figure 31 shows the output drive characteristics of APEX 20KC devices.

***Figure 31. Output Drive Characteristics of APEX 20KC Devices*** *Note (1)*




*Note to Figure 31:*

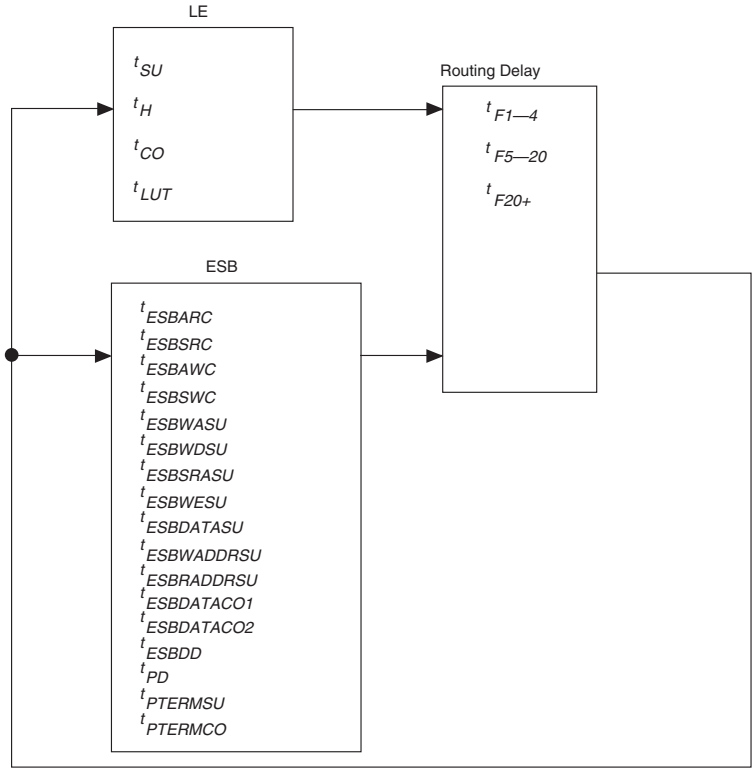
(1) These are transient (AC) currents.

## Timing Model

The high-performance FastTrack and MegaLAB interconnect routing resources ensure predictable performance, accurate simulation, and accurate timing analysis. This predictable performance contrasts with that of FPGAs, which use a segmented connection scheme and therefore have unpredictable performance.

Figure 32 shows the $f_{MAX}$ timing model for APEX 20KC devices.

***Figure 32. $f_{MAX}$ Timing Model***




Figures 33 and 34 show the asynchronous and synchronous timingwaveforms, respectively, for the ESB macroparameters in Table 37.

*Figure 33. ESB Asynchronous Timing Waveforms*

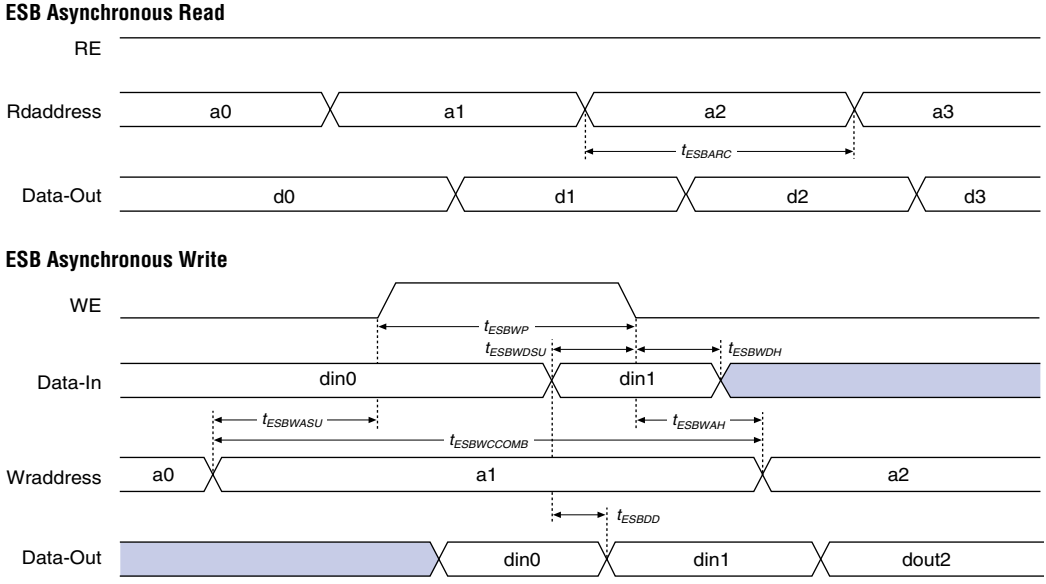


*Figure 34. ESB Synchronous Timing Waveforms*

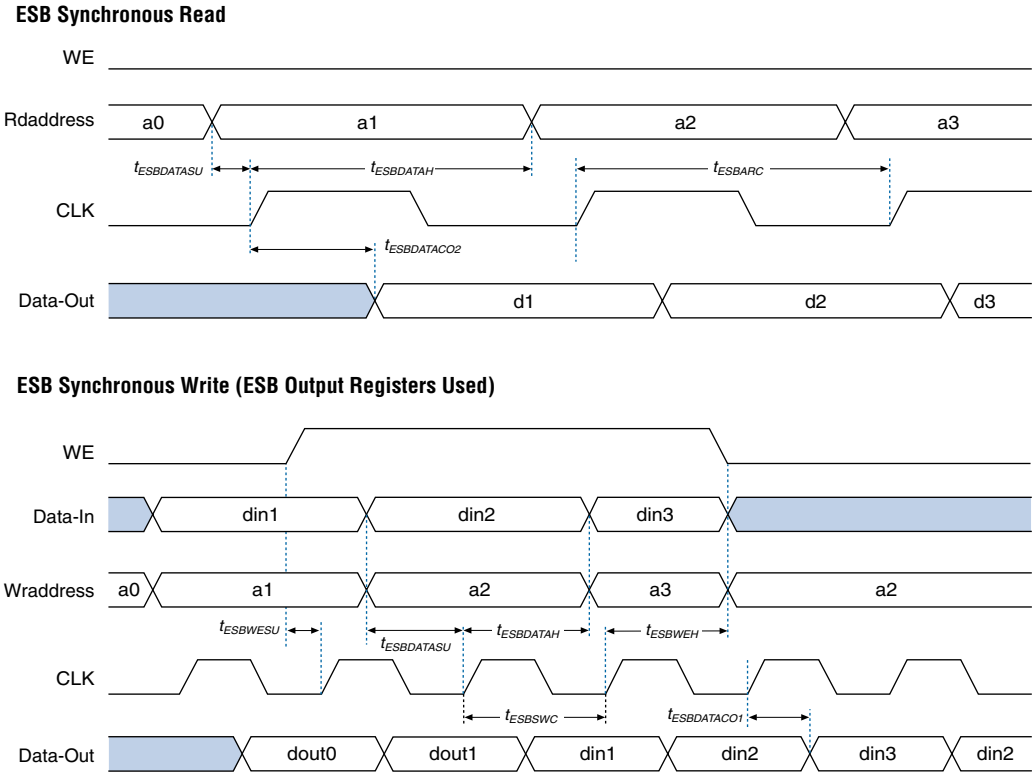
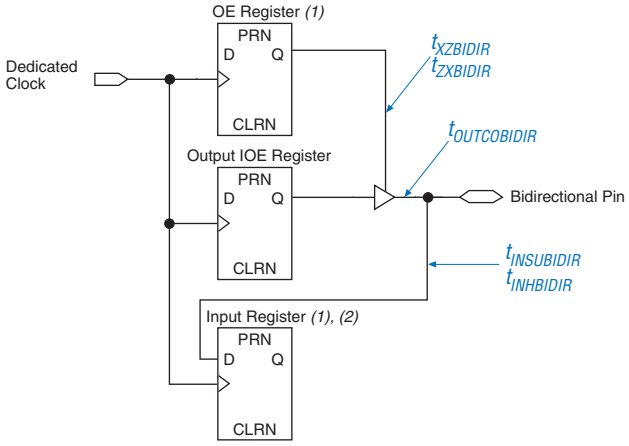



Figure 35 shows the timing model for bidirectional I/O pin timing.

*Figure 35. Synchronous Bidirectional Pin External Timing*




*Notes to Figure 35:*

(1) The output enable and input registers are LE registers in the LAB adjacent to the bidirectional pin. Use the "Output Enable Routing = Single-Pin" option in the Quartus II software to set the output enable register.

(2) Use the "Decrease Input Delay to Internal Cells = OFF" option in the Quartus II software to set the LAB-adjacent input register. This maintains a zero hold time for LAB-adjacent registers while giving a fast, position-independent setup time. Set "Decrease Input Delay to Internal Cells = ON" and move the input register farther away from the bidirectional pin for a faster setup time with zero hold time. The exact position where zero hold occurs with the minimum setup time varies with device density and speed grade.

Tables 36 to 38 describes the $f_{MAX}$ timing parameters shown in Figure 32. Table 39 describes the functional timing parameters.

*Table 36. APEX 20KC $f_{MAX}$ LE Timing Parameters*

| Symbol | Parameter |
|---|---|
| $t_{SU}$ | LE register setup time before clock |
| $t_{H}$ | LE register hold time before clock |
| $t_{CO}$ | LE register clock-to-output delay |
| $t_{LUT}$ | LUT delay for data-in to data-out |

| *Table 37. APEX 20KC $f_{MAX}$ ESB Timing Parameters* | |
|---|---|
| **Symbol** | **Parameter** |
| $t_{ESBARC}$ | ESB asynchronous read cycle time |
| $t_{ESBSRC}$ | ESB synchronous read cycle time |
| $t_{ESBAWC}$ | ESB asynchronous write cycle time |
| $t_{ESBSWC}$ | ESB synchronous write cycle time |
| $t_{ESBWASU}$ | ESB write address setup time with respect to WE |
| $t_{ESBWAH}$ | ESB write address hold time with respect to WE |
| $t_{ESBWDSU}$ | ESB data setup time with respect to WE |
| $t_{ESBWDH}$ | ESB data hold time with respect to WE |
| $t_{ESBRASU}$ | ESB read address setup time with respect to RE |
| $t_{ESBRAH}$ | ESB read address hold time with respect to RE |
| $t_{ESBWESU}$ | ESB WE setup time before clock when using input register |
| $t_{ESBDATASU}$ | ESB data setup time before clock when using input register |
| $t_{ESBWADDRSU}$ | ESB write address setup time before clock when using input registers |
| $t_{ESBRADDRSU}$ | ESB read address setup time before clock when using input registers |
| $t_{ESBDATACO1}$ | ESB clock-to-output delay when using output registers |
| $t_{ESBDATACO2}$ | ESB clock-to-output delay without output registers |
| $t_{ESBDD}$ | ESB data-in to data-out delay for RAM mode |
| $t_{PD}$ | ESB macrocell input to non-registered output |
| $t_{PTERMSU}$ | ESB macrocell register setup time before clock |
| $t_{PTERMCO}$ | ESB macrocell register clock-to-output delay |

| *Table 38. APEX 20KC $f_{MAX}$ Routing Delays* | |
|---|---|
| **Symbol** | **Parameter** |
| $t_{F1-4}$ | Fan-out delay estimate using local interconnect |
| $t_{F5-20}$ | Fan-out delay estimate using MegaLab interconnect |
| $t_{F20+}$ | Fan-out delay estimate using FastTrack interconnect |

| *Table 39. APEX 20KC Minimum Pulse Width Timing Parameters* | |
|---|---|
| **Symbol** | **Parameter** |
| $t_{CH}$ | Minimum clock high time from clock pin |
| $t_{CL}$ | Minimum clock low time from clock pin |
| $t_{CLRP}$ | LE clear pulse width |
| $t_{PREP}$ | LE preset pulse width |
| $t_{ESBCH}$ | Clock high time |
| $t_{ESBCL}$ | Clock low time |
| $t_{ESBWP}$ | Write pulse width |
| $t_{ESBRP}$ | Read pulse width |

Tables 40 and 41 describe APEX 20KC external timing parameters. The timing values for these pin-to-pin delays are reported for all pins using the 3.3-V LVTTL I/O standard.

| *Table 40. APEX 20KC External Timing Parameters* *Note (1)* | | |
|---|---|---|
| **Symbol** | **Clock Parameter** | **Conditions** |
| $t_{INSU}$ | Setup time with global clock at IOE register | |
| $t_{INH}$ | Hold time with global clock at IOE register | |
| $t_{OUTCO}$ | Clock-to-output delay with global clock at IOE output register | *(2)* |
| $t_{INSUPLL}$ | Setup time with PLL clock at IOE input register | |
| $t_{INHPLL}$ | Hold time with PLL clock at IOE input register | |
| $t_{OUTCOPLL}$ | Clock-to-output delay with PLL clock at IOE output register | *(2)* |

| *Table 41. APEX 20KC External Bidirectional Timing Parameters* *Note (1)* | | |
|---|---|---|
| **Symbol** | **Parameter** | **Condition** |
| $t_{INSUBIDIR}$ | Setup time for bidirectional pins with global clock at LAB-adjacent input register | |
| $t_{INHBIDIR}$ | Hold time for bidirectional pins with global clock at LAB-adjacent input register | |
| $t_{OUTCOBIDIR}$ | Clock-to-output delay for bidirectional pins with global clock at IOE register | *(2)* |
| $t_{XZBIDIR}$ | Synchronous output enable register to output buffer disable delay | *(2)* |
| $t_{ZXBIDIR}$ | Synchronous output enable register to output buffer enable delay | *(2)* |
| $t_{INSUBIDIRPLL}$ | Setup time for bidirectional pins with PLL clock at LAB-adjacent input register | |
| $t_{INHBIDIRPLL}$ | Hold time for bidirectional pins with PLL clock at LAB-adjacent input register | |
| $t_{OUTCOBIDIRPLL}$ | Clock-to-output delay for bidirectional pins with PLL clock at IOE register | *(2)* |
| $t_{XZBIDIRPLL}$ | Synchronous output enable register to output buffer disable delay with PLL | *(2)* |
| $t_{ZXBIDIRPLL}$ | Synchronous output enable register to output buffer enable delay with PLL | *(2)* |

*Notes to Tables 40 and 41:*
(1) These timing parameters are sample-tested only.
(2) For more information, refer to Table 43.

Tables 42 and 43 define the timing delays for each I/O standard. Some output standards require test load circuits for AC timing measurements as shown in Figures 36 through 38.

| *Table 42. APEX 20KC Selectable I/O Standard Input Adder Delays (Part 1 of 2)* *Note (1)* | | |
|---|---|---|
| **Symbol** | **Parameter** | **Condition** |
| LVCMOS | Input adder delay for the LVCMOS I/O standard | |
| LVTTL | Input adder delay for the LVTTL I/O standard | |
| 2.5 V | Input adder delay for the 2.5-V I/O standard | |
| 1.8 V | Input adder delay for the 1.8-V I/O standard | |
| PCI | Input adder delay for the PCI I/O standard | |
| GTl+ | Input adder delay for the GTL+ I/O standard | |
| SSTL-3 Class I | Input adder delay for the SSTL-3 Class I I/O standard | |
| SSTL-3 Class II | Input adder delay for the SSTL-3 Class II I/O standard | |
| SSTL-2 Class I | Input adder delay for the SSTL -2 Class I I/O standard | |
| SSTL-2 Class II | Input adder delay for the SSTL -2 Class II I/O standard | |

| *Table 42. APEX 20KC Selectable I/O Standard Input Adder Delays (Part 2 of 2)* *Note (1)* | | |
|---|---|---|
| **Symbol** | **Parameter** | **Condition** |
| LVDS | Input adder delay for the LVDS I/O standard | |
| CTT | Input adder delay for the CTT I/O standard | |
| AGP | Input adder delay for the AGP I/O standard | |

| *Table 43. APEX 20KC Selectable I/O Standard Output Adder Delays* *Note (1)* | | |
|---|---|---|
| **Symbol** | **Parameter** | **Condition** |
| LVCMOS | Output adder delay for the LVCMOS I/O standard | |
| LVTTL | Output adder delay for the LVTTL I/O standard | Cload = 35 pF<br>Rup = 564.5 Ω<br>Rdn = 430 Ω *(2)* |
| 2.5 V | Output adder delay for the 2.5-V I/O standard | Cload = 35 pF<br>Rup = 450 Ω<br>Rdn = 450 Ω *(2)* |
| 1.8 V | Output adder delay for the 1.8-V I/O standard | Cload = 35 pF<br>Rup = 520 Ω<br>Rdn = 480 Ω *(2)* |
| PCI | Output adder delay for the PCI I/O standard | Cload = 10 pF<br>Rup = 1M Ω<br>Rdn = 25 Ω *(2)* |
| GTl+ | Output adder delay for the GTL+ I/O standard | Cload = 30 pF<br>Rup = 25 Ω *(2)* |
| SSTL-3 Class I | Output adder delay for the SSTL-3 Class I I/O standard | Cload1 = 0 pF<br>Cload2 = 30 pF<br>R = 25 Ω *(2)* |
| SSTL-3 Class II | Output adder delay for the SSTL-3 Class II I/O standard | Cload1 = 0 pF<br>Cload2 = 30 pF<br>R = 25 Ω *(2)* |
| SSTL-2 Class I | Output adder delay for the SSTL-2 Class I I/O standard | |
| SSTL-2 Class II | Output adder delay for the SSTL-2 Class II I/O standard | |
| LVDS | Output adder delay for the LVDS I/O standard | Cload = 4 pF<br>R=100 Ω *(2)* |
| CTT | Output adder delay for the CTT I/O standard | |
| AGP | Output adder delay for the AGP I/O standard | |

*Note to Tables 42 and 43:*

(1) These delays report the differences in delays for different I/O standards. Add the delay for the I/O standard that is used to the external timing parameters.

(2) See Figure 36 for more information.

*Figure 36. AC Test Conditions for LVTTL, 2.5 V, 1.8 V, PCI & GTL+ I/O Standards*

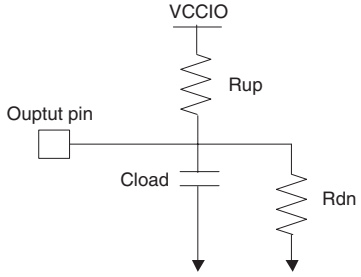



*Figure 37. AC Test Conditions for SSTL-3 Class I & II I/O Standards*

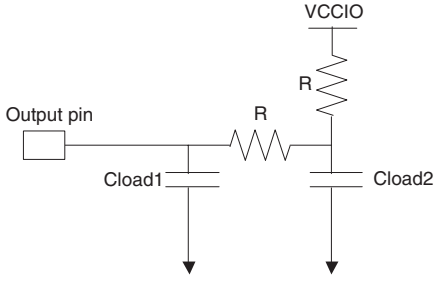
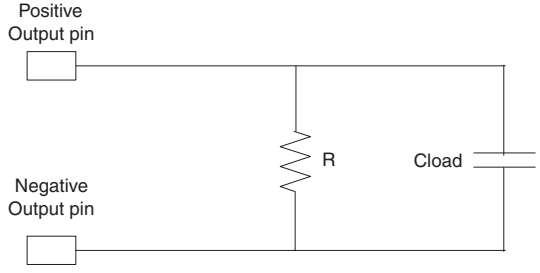



*Figure 38. AC Test Conditions for the LVDS I/O Standard*



Tables 44 through 67 show the $f_{MAX}$ and external timing parameters for EPC20K200C, EP20K400C, EP20K600C, and EP20K1000C devices.

*Table 44. EP20K200C $f_{MAX}$ LE Timing Microparameters*

| Symbol | -7 Speed Grade | | -8 Speed Grade | | -9 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{SU}$ | 0.01 | | 0.01 | | 0.01 | | ns |
| $t_{H}$ | 0.10 | | 0.10 | | 0.10 | | ns |
| $t_{CO}$ | | 0.27 | | 0.30 | | 0.32 | ns |
| $t_{LUT}$ | | 0.65 | | 0.78 | | 0.92 | ns |

*Table 45. EP20K200C $f_{MAX}$ ESB Timing Microparameters*

| Symbol | -7 Speed Grade | | -8 Speed Grade | | -9 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{ESBARC}$ | | 1.30 | | 1.51 | | 1.69 | ns |
| $t_{ESBSRC}$ | | 2.35 | | 2.49 | | 2.72 | ns |
| $t_{ESBAWC}$ | | 2.92 | | 3.46 | | 3.86 | ns |
| $t_{ESBSWC}$ | | 3.05 | | 3.44 | | 3.85 | ns |
| $t_{ESBWASU}$ | 0.45 | | 0.50 | | 0.54 | | ns |
| $t_{ESBWAH}$ | 0.44 | | 0.50 | | 0.55 | | ns |
| $t_{ESBWDSU}$ | 0.57 | | 0.63 | | 0.68 | | ns |
| $t_{ESBWDH}$ | 0.44 | | 0.50 | | 0.55 | | ns |
| $t_{ESBRASU}$ | 1.25 | | 1.43 | | 1.56 | | ns |
| $t_{ESBRAH}$ | 0.00 | | 0.03 | | 0.11 | | ns |
| $t_{ESBWESU}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBDATASU}$ | 2.01 | | 2.27 | | 2.45 | | ns |
| $t_{ESBWADDRSU}$ | –0.20 | | –0.24 | | –0.28 | | ns |
| $t_{ESBRADDRSU}$ | 0.02 | | 0.00 | | –0.02 | | ns |
| $t_{ESBDATACO1}$ | | 1.09 | | 1.28 | | 1.43 | ns |
| $t_{ESBDATACO2}$ | | 2.10 | | 2.52 | | 2.82 | ns |
| $t_{ESBDD}$ | | 2.50 | | 2.97 | | 3.32 | ns |
| $t_{PD}$ | | 1.48 | | 1.78 | | 2.00 | ns |
| $t_{PTERMSU}$ | 0.58 | | 0.72 | | 0.81 | | ns |
| $t_{PTERMCO}$ | | 1.10 | | 1.29 | | 1.45 | ns |

*Table 46. EP20K200C $f_{MAX}$ Routing Delays*

| Symbol | -7 Speed Grade | | -8 Speed Grade | | -9 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{F1-4}$ | | 0.15 | | 0.17 | | 0.20 | ns |
| $t_{F5-20}$ | | 0.81 | | 0.94 | | 1.12 | ns |
| $t_{F20+}$ | | 0.98 | | 1.13 | | 1.35 | ns |

*Table 47. EP20K200C Minimum Pulse Width Timing Parameters*

| Symbol | -7 Speed Grade | | -8 Speed Grade | | -9 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{CH}$ | 1.33 | | 1.66 | | 2.00 | | ns |
| $t_{CL}$ | 1.33 | | 1.66 | | 2.00 | | ns |
| $t_{CLRP}$ | 0.20 | | 0.20 | | 0.20 | | ns |
| $t_{PREP}$ | 0.20 | | 0.20 | | 0.20 | | ns |
| $t_{ESBCH}$ | 1.33 | | 1.66 | | 2.00 | | ns |
| $t_{ESBCL}$ | 1.33 | | 1.66 | | 2.00 | | ns |
| $t_{ESBWP}$ | 1.05 | | 1.28 | | 1.44 | | ns |
| $t_{ESBRP}$ | 0.87 | | 1.06 | | 1.19 | | ns |

*Table 48. EP20K200C External Timing Parameters*

| Symbol | -7 Speed Grade | | -8 Speed Grade | | -9 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 1.23 | | 1.26 | | 1.33 | | ns |
| $t_{INH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCO}$ | 2.00 | 3.79 | 2.00 | 4.31 | 2.00 | 4.70 | ns |
| $t_{INSUPLL}$ | 0.81 | | 0.92 | | - | | ns |
| $t_{INHPLL}$ | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOPLL}$ | 0.50 | 2.36 | 0.50 | 2.62 | - | - | ns |

*Table 49. EP20K200C External Bidirectional Timing Parameters*

| Symbol | -7 Speed Grade | | -8 Speed Grade | | -9 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ | 1.38 | | 1.78 | | 1.99 | | ns |
| $t_{INHBIDIR}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCOBIDIR}$ | 2.00 | 3.79 | 2.00 | 4.31 | 2.00 | 4.70 | ns |
| $t_{XZBIDIR}$ | | 6.12 | | 6.51 | | 7.89 | ns |
| $t_{ZXBIDIR}$ | | 6.12 | | 6.51 | | 7.89 | ns |
| $t_{INSUBIDIRPLL}$ | 2.82 | | 3.47 | | - | | ns |
| $t_{INHBIDIRPLL}$ | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOBIDIRPLL}$ | 0.50 | 2.36 | 0.50 | 2.62 | - | - | ns |
| $t_{XZBIDIRPLL}$ | | 4.69 | | 4.82 | | - | ns |
| $t_{ZXBIDIRPLL}$ | | 4.69 | | 4.82 | | - | ns |

*Table 50. EP20K400C $f_{MAX}$ LE Timing Parameters*

| Symbol | -7 Speed Grade | | -8 Speed Grade | | -9 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{SU}$ | 0.01 | | 0.01 | | 0.01 | | ns |
| $t_{H}$ | 0.10 | | 0.10 | | 0.10 | | ns |
| $t_{CO}$ | | 0.27 | | 0.30 | | 0.32 | ns |
| $t_{LUT}$ | | 0.65 | | 0.78 | | 0.92 | ns |

*Table 51. EP20K400C $f_{MAX}$ ESB Timing Parameters*

| Symbol | -7 Speed Grade | | -8 Speed Grade | | -9 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{ESBARC}$ | | 1.30 | | 1.51 | | 1.69 | ns |
| $t_{ESBSRC}$ | | 2.35 | | 2.49 | | 2.72 | ns |
| $t_{ESBAWC}$ | | 2.92 | | 3.46 | | 3.86 | ns |
| $t_{ESBSWC}$ | | 3.05 | | 3.44 | | 3.85 | ns |
| $t_{ESBWASU}$ | 0.45 | | 0.50 | | 0.54 | | ns |
| $t_{ESBWAH}$ | 0.44 | | 0.50 | | 0.55 | | ns |
| $t_{ESBWDSU}$ | 0.57 | | 0.63 | | 0.68 | | ns |
| $t_{ESBWDH}$ | 0.44 | | 0.50 | | 0.55 | | ns |
| $t_{ESBRASU}$ | 1.25 | | 1.43 | | 1.56 | | ns |
| $t_{ESBRAH}$ | 0.00 | | 0.03 | | 0.11 | | ns |
| $t_{ESBWESU}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBDATASU}$ | 2.01 | | 2.27 | | 2.45 | | ns |
| $t_{ESBWADDRSU}$ | –0.20 | | –0.24 | | –0.28 | | ns |
| $t_{ESBRADDRSU}$ | 0.02 | | 0.00 | | –0.02 | | ns |
| $t_{ESBDATACO1}$ | | 1.09 | | 1.28 | | 1.43 | ns |
| $t_{ESBDATACO2}$ | | 2.10 | | 2.52 | | 2.82 | ns |
| $t_{ESBDD}$ | | 2.50 | | 2.97 | | 3.32 | ns |
| $t_{PD}$ | | 1.48 | | 1.78 | | 2.00 | ns |
| $t_{PTERMSU}$ | 0.58 | | 0.72 | | 0.81 | | ns |
| $t_{PTERMCO}$ | | 1.10 | | 1.29 | | 1.45 | ns |

*Table 52. EP20K400C $f_{MAX}$ Routing Delays*

| Symbol | -7 Speed Grade | | -8 Speed Grade | | -9 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{F1-4}$ | | 0.15 | | 0.17 | | 0.19 | ns |
| $t_{F5-20}$ | | 0.94 | | 1.06 | | 1.25 | ns |
| $t_{F20+}$ | | 1.73 | | 1.96 | | 2.30 | ns |

*Table 53. EP20K400C Minimum Pulse Width Timing Parameters*

| Symbol | -7 Speed Grade | | -8 Speed Grade | | -9 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{CH}$ | 1.33 | | 1.66 | | 2.00 | | ns |
| $t_{CL}$ | 1.33 | | 1.66 | | 2.00 | | ns |
| $t_{CLRP}$ | 0.20 | | 0.20 | | 0.20 | | ns |
| $t_{PREP}$ | 0.20 | | 0.20 | | 0.20 | | ns |
| $t_{ESBCH}$ | 1.33 | | 1.66 | | 2.00 | | ns |
| $t_{ESBCL}$ | 1.33 | | 1.66 | | 2.00 | | ns |
| $t_{ESBWP}$ | 1.05 | | 1.28 | | 1.44 | | ns |
| $t_{ESBRP}$ | 0.87 | | 1.06 | | 1.19 | | ns |

*Table 54. EP20K400C External Timing Parameters*

| Symbol | -7 Speed Grade | | -8 Speed Grade | | -9 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 1.37 | | 1.52 | | 1.64 | | ns |
| $t_{INH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCO}$ | 2.00 | 4.25 | 2.00 | 4.61 | 2.00 | 5.03 | ns |
| $t_{INSUPLL}$ | 0.80 | | 0.91 | | - | | ns |
| $t_{INHPLL}$ | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOPLL}$ | 0.50 | 2.27 | 0.50 | 2.55 | - | - | ns |

*Table 55. EP20K400C External Bidirectional Timing Parameters*

| Symbol | -7 Speed Grade | | -8 Speed Grade | | -9 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ | 1.29 | | 1.67 | | 1.92 | | ns |
| $t_{INHBIDIR}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCOBIDIR}$ | 2.00 | 4.25 | 2.00 | 4.61 | 2.00 | 5.03 | ns |
| $t_{XZBIDIR}$ | | 6.55 | | 6.97 | | 7.35 | ns |
| $t_{ZXBIDIR}$ | | 6.55 | | 6.97 | | 7.36 | ns |
| $t_{INSUBIDIRPLL}$ | 3.22 | | 3.80 | | - | | ns |
| $t_{INHBIDIRPLL}$ | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOBIDIRPLL}$ | 0.50 | 2.27 | 0.50 | 2.55 | - | - | ns |
| $t_{XZBIDIRPLL}$ | | 4.62 | | 4.84 | | - | ns |
| $t_{ZXBIDIRPLL}$ | | 4.62 | | 4.84 | | - | ns |

*Table 56. EP20K600C $f_{MAX}$ LE Timing Parameters*

| Symbol | -7 Speed Grade | | -8 Speed Grade | | -9 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{SU}$ | 0.01 | | 0.01 | | 0.01 | | ns |
| $t_{H}$ | 0.10 | | 0.10 | | 0.10 | | ns |
| $t_{CO}$ | | 0.27 | | 0.30 | | 0.32 | ns |
| $t_{LUT}$ | | 0.65 | | 0.78 | | 0.92 | ns |

*Table 57. EP20K600C $f_{MAX}$ ESB Timing Parameters*

| Symbol | -7 Speed Grade | | -8 Speed Grade | | -9 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{ESBARC}$ | | 1.30 | | 1.51 | | 1.69 | ns |
| $t_{ESBSRC}$ | | 2.35 | | 2.49 | | 2.72 | ns |
| $t_{ESBAWC}$ | | 2.92 | | 3.46 | | 3.86 | ns |
| $t_{ESBSWC}$ | | 3.05 | | 3.44 | | 3.85 | ns |
| $t_{ESBWASU}$ | 0.45 | | 0.50 | | 0.54 | | ns |
| $t_{ESBWAH}$ | 0.44 | | 0.50 | | 0.55 | | ns |
| $t_{ESBWDSU}$ | 0.57 | | 0.63 | | 0.68 | | ns |
| $t_{ESBWDH}$ | 0.44 | | 0.50 | | 0.55 | | ns |
| $t_{ESBRASU}$ | 1.25 | | 1.43 | | 1.56 | | ns |
| $t_{ESBRAH}$ | 0.00 | | 0.03 | | 0.11 | | ns |
| $t_{ESBWESU}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBDATASU}$ | 2.01 | | 2.27 | | 2.45 | | ns |
| $t_{ESBWADDRSU}$ | –0.20 | | –0.24 | | –0.28 | | ns |
| $t_{ESBRADDRSU}$ | 0.02 | | 0.00 | | –0.02 | | ns |
| $t_{ESBDATACO1}$ | | 1.09 | | 1.28 | | 1.43 | ns |
| $t_{ESBDATACO2}$ | | 2.10 | | 2.52 | | 2.82 | ns |
| $t_{ESBDD}$ | | 2.50 | | 2.97 | | 3.32 | ns |
| $t_{PD}$ | | 1.48 | | 1.78 | | 2.00 | ns |
| $t_{PTERMSU}$ | 0.58 | | 0.72 | | 0.81 | | ns |
| $t_{PTERMCO}$ | | 1.10 | | 1.29 | | 1.45 | ns |

*Table 58. EP20K600C $f_{MAX}$ Routing Delays*

| Symbol | -7 Speed Grade | | -8 Speed Grade | | -9 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{F1-4}$ | | 0.15 | | 0.16 | | 0.18 | ns |
| $t_{F5-20}$ | | 0.94 | | 1.05 | | 1.20 | ns |
| $t_{F20+}$ | | 1.76 | | 1.98 | | 2.23 | ns |

*Table 59. EP20K600C Minimum Pulse Width Timing Parameters*

| Symbol | -7 Speed Grade | | -8 Speed Grade | | -9 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{CH}$ | 1.33 | | 1.66 | | 2.00 | | ns |
| $t_{CL}$ | 1.33 | | 1.66 | | 2.00 | | ns |
| $t_{CLRP}$ | 0.20 | | 0.20 | | 0.20 | | ns |
| $t_{PREP}$ | 0.20 | | 0.20 | | 0.20 | | ns |
| $t_{ESBCH}$ | 1.33 | | 1.66 | | 2.00 | | ns |
| $t_{ESBCL}$ | 1.33 | | 1.66 | | 2.00 | | ns |
| $t_{ESBWP}$ | 1.05 | | 1.28 | | 1.44 | | ns |
| $t_{ESBRP}$ | 0.87 | | 1.06 | | 1.19 | | ns |

*Table 60. EP20K600C External Timing Parameters*

| Symbol | -7 Speed Grade | | -8 Speed Grade | | -9 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 1.28 | | 1.40 | | 1.45 | | ns |
| $t_{INH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCO}$ | 2.00 | 4.29 | 2.00 | 4.77 | 2.00 | 5.11 | ns |
| $t_{INSUPLL}$ | 0.80 | | 0.91 | | - | | ns |
| $t_{INHPLL}$ | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOPLL}$ | 0.50 | 2.37 | 0.50 | 2.63 | - | - | ns |

*Table 61. EP20K600C External Bidirectional Timing Parameters*

| Symbol | -7 Speed Grade | | -8 Speed Grade | | -9 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ | 2.03 | | 2.57 | | 2.97 | | ns |
| $t_{INHBIDIR}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCOBIDIR}$ | 2.00 | 4.29 | 2.00 | 4.77 | 2.00 | 5.11 | ns |
| $t_{XZBIDIR}$ | | 8.31 | | 9.14 | | 9.76 | ns |
| $t_{ZXBIDIR}$ | | 8.31 | | 9.14 | | 9.76 | ns |
| $t_{INSUBIDIRPLL}$ | 3.99 | | 4.77 | | - | | ns |
| $t_{INHBIDIRPLL}$ | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOBIDIRPLL}$ | 0.50 | 2.37 | 0.50 | 2.63 | - | - | ns |
| $t_{XZBIDIRPLL}$ | | 6.35 | | 6.94 | | - | ns |
| $t_{ZXBIDIRPLL}$ | | 6.35 | | 6.94 | | - | ns |

*Table 62. EP20K1000C $f_{MAX}$ LE Timing Microparameters*

| Symbol | -7 Speed Grade | | -8 Speed Grade | | -9 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{SU}$ | 0.01 | | 0.01 | | 0.01 | | ns |
| $t_{H}$ | 0.10 | | 0.10 | | 0.10 | | ns |
| $t_{CO}$ | | 0.27 | | 0.30 | | 0.32 | ns |
| $t_{LUT}$ | | 0.66 | | 0.79 | | 0.92 | ns |

*Table 63. EP20K1000C $f_{MAX}$ ESB Timing Microparameters*

| Symbol | -7 Speed Grade | | -8 Speed Grade | | -9 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{ESBARC}$ | | 1.48 | | 1.57 | | 1.65 | ns |
| $t_{ESBSRC}$ | | 2.36 | | 2.50 | | 2.73 | ns |
| $t_{ESBAWC}$ | | 2.93 | | 3.46 | | 3.86 | ns |
| $t_{ESBSWC}$ | | 3.08 | | 3.43 | | 3.83 | ns |
| $t_{ESBWASU}$ | 0.51 | | 0.50 | | 0.52 | | ns |
| $t_{ESBWAH}$ | 0.38 | | 0.51 | | 0.57 | | ns |
| $t_{ESBWDSU}$ | 0.62 | | 0.62 | | 0.66 | | ns |
| $t_{ESBWDH}$ | 0.38 | | 0.51 | | 0.57 | | ns |
| $t_{ESBRASU}$ | 1.40 | | 1.47 | | 1.53 | | ns |
| $t_{ESBRAH}$ | 0.00 | | 0.07 | | 0.18 | | ns |
| $t_{ESBWESU}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBDATASU}$ | 1.92 | | 2.19 | | 2.35 | | ns |
| $t_{ESBWADDRSU}$ | –0.20 | | –0.28 | | –0.32 | | ns |
| $t_{ESBRADDRSU}$ | 0.00 | | –0.03 | | –0.05 | | ns |
| $t_{ESBDATACO1}$ | | 1.12 | | 1.30 | | 1.46 | ns |
| $t_{ESBDATACO2}$ | | 2.11 | | 2.53 | | 2.84 | ns |
| $t_{ESBDD}$ | | 2.56 | | 2.96 | | 3.30 | ns |
| $t_{PD}$ | | 1.49 | | 1.79 | | 2.02 | ns |
| $t_{PTERMSU}$ | 0.61 | | 0.69 | | 0.77 | | ns |
| $t_{PTERMCO}$ | | 1.13 | | 1.32 | | 1.48 | ns |

*Table 64. EP20K1000C $f_{MAX}$ Routing Delays*

| Symbol | -7 Speed Grade | | -8 Speed Grade | | -9 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{F1-4}$ | | 0.15 | | 0.17 | | 0.19 | ns |
| $t_{F5-20}$ | | 1.13 | | 1.31 | | 1.50 | ns |
| $t_{F20+}$ | | 2.30 | | 2.71 | | 3.19 | ns |

*Table 65. EP20K1000C Minimum Pulse Width Timing Parameters*

| Symbol | -7 Speed Grade | | -8 Speed Grade | | -9 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{CH}$ | 1.33 | | 1.66 | | 2.00 | | ns |
| $t_{CL}$ | 1.33 | | 1.66 | | 2.00 | | ns |
| $t_{CLRP}$ | 0.20 | | 0.20 | | 0.20 | | ns |
| $t_{PREP}$ | 0.20 | | 0.20 | | 0.20 | | ns |
| $t_{ESBCH}$ | 1.33 | | 1.66 | | 2.00 | | ns |
| $t_{ESBCL}$ | 1.33 | | 1.66 | | 2.00 | | ns |
| $t_{ESBWP}$ | 1.04 | | 1.26 | | 1.41 | | ns |
| $t_{ESBRP}$ | 0.87 | | 1.05 | | 1.18 | | ns |

*Table 66. EP20K1000C External Timing Parameters*

| Symbol | -7 Speed Grade | | -8 Speed Grade | | -9 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 1.14 | | 1.14 | | 1.11 | | ns |
| $t_{INH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCO}$ | 2.00 | 4.63 | 2.00 | 5.26 | 2.00 | 5.69 | ns |
| $t_{INSUPLL}$ | 0.81 | | 0.92 | | - | | ns |
| $t_{INHPLL}$ | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOPLL}$ | 0.50 | 2.32 | 0.50 | 2.55 | - | - | ns |

*Table 67. EP20K1000C External Bidirectional Timing Parameters*

| Symbol | -7 Speed Grade | | -8 Speed Grade | | -9 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ | 1.86 | | 2.54 | | 3.15 | | ns |
| $t_{INHBIDIR}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCOBIDIR}$ | 2.00 | 4.63 | 2.00 | 5.26 | 2.00 | 5.69 | ns |
| $t_{XZBIDIR}$ | | 8.98 | | 9.89 | | 10.67 | ns |
| $t_{ZXBIDIR}$ | | 8.98 | | 9.89 | | 10.67 | ns |
| $t_{INSUBIDIRPLL}$ | 4.17 | | 5.27 | | - | | ns |
| $t_{INHBIDIRPLL}$ | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOBIDIRPLL}$ | 0.50 | 2.32 | 0.50 | 2.55 | - | - | ns |
| $t_{XZBIDIRPLL}$ | | 6.67 | | 7.18 | | - | ns |
| $t_{ZXBIDIRPLL}$ | | 6.67 | | 7.18 | | - | ns |

Tables 68 and 69 show selectable I/O standard input and output delays for APEX 20KC devices. If you select an I/O standard input or output delay other than LVCMOS, add the delay for the selected speed grade to the LVCMOS value.

*Table 68. Selectable I/O Standard Input Delays*

| Symbol | -7 Speed Grade | | -8 Speed Grade | | -9 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | Min |
| LVCMOS | | 0.00 | | 0.00 | | 0.00 | ns |
| LVTTL | | 0.00 | | 0.00 | | 0.00 | ns |
| 2.5 V | | 0.00 | | 0.00 | | 0.00 | ns |
| 1.8 V | | 0.04 | | 0.11 | | 0.14 | ns |
| PCI | | 0.00 | | 0.04 | | 0.03 | ns |
| GTL+ | | –0.30 | | 0.25 | | 0.23 | ns |
| SSTL-3 Class I | | –0.19 | | –0.13 | | –0.13 | ns |
| SSTL-3 Class II | | –0.19 | | –0.13 | | –0.13 | ns |
| SSTL-2 Class I | | –0.19 | | –0.13 | | –0.13 | ns |
| SSTL-2 Class II | | –0.19 | | –0.13 | | –0.13 | ns |
| LVDS | | –0.19 | | –0.17 | | –0.16 | ns |
| CTT | | 0.00 | | 0.00 | | 0.00 | ns |
| AGP | | 0.00 | | 0.00 | | 0.00 | ns |

*Table 69. Selectable I/O Standard Output Delays*

| Symbol | -7 Speed Grade | | -8 Speed Grad | | -9 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | Min |
| LVCMOS | | 0.00 | | 0.00 | | 0.00 | ns |
| LVTTL | | 0.00 | | 0.00 | | 0.00 | ns |
| 2.5 V | | 0.00 | | 0.00 | | 0.00 | ns |
| 1.8 V | | 1.18 | | 1.41 | | 1.57 | ns |
| PCI | | –0.52 | | –0.53 | | –0.56 | ns |
| GTL+ | | –0.18 | | –0.29 | | –0.39 | ns |
| SSTL-3 Class I | | –0.67 | | –0.71 | | –0.75 | ns |
| SSTL-3 Class II | | –0.67 | | –0.71 | | –0.75 | ns |
| SSTL-2 Class I | | –0.67 | | –0.71 | | –0.75 | ns |
| SSTL-2 Class II | | –0.67 | | –0.71 | | –0.75 | ns |
| LVDS | | –0.69 | | –0.70 | | –0.73 | ns |
| CTT | | 0.00 | | 0.00 | | 0.00 | ns |
| AGP | | 0.00 | | 0.00 | | 0.00 | ns |

# Power Consumption

To estimate device power consumption, use the interactive power estimator on the Altera web site at **http://www.altera.com**.

# Configuration & Operation

The APEX 20KC architecture supports several configuration schemes. This section summarizes the device operating modes and available device configuration schemes.

## Operating Modes

The APEX architecture uses SRAM configuration elements that require configuration data to be loaded each time the circuit powers up. The process of physically loading the SRAM data into the device is called configuration. During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. The I/O pins are tri-stated during power-up, and before and during configuration. Together, the configuration and initialization processes are called *command mode*; normal device operation is called *user mode*.

Before and during device configuration, all I/O pins are pulled to $V_{CCIO}$ by a built-in weak pull-up resistor.

SRAM configuration elements allow APEX 20KC devices to be reconfigured in-circuit by loading new configuration data into the device. Real-time reconfiguration is performed by forcing the device into command mode with a device pin, loading different configuration data, reinitializing the device, and resuming user-mode operation. In-field upgrades can be performed by distributing new configuration files.

### Configuration Schemes

The configuration data for an APEX 20KC device can be loaded with one of five configuration schemes (see Table 70), chosen on the basis of the target application. An EPC16, EPC2, or EPC1 configuration device, intelligent controller, or the JTAG port can be used to control the configuration of an APEX 20KC device. When a configuration device is used, the system can configure automatically at system power-up.

Multiple APEX 20KC devices can be configured in any of five configuration schemes by connecting the configuration enable (nCE) and configuration enable output (nCEO) pins on each device.

*Table 70. Data Sources for Configuration*

| Configuration Scheme | Data Source |
|---|---|
| Configuration device | EPC16, EPC8, EPC4, EPC2, or EPC1 configuration device |
| Passive serial (PS) | MasterBlaster or ByteBlasterMV download cable or serial data source |
| Passive parallel asynchronous (PPA) | Parallel data source |
| Passive parallel synchronous (PPS) | Parallel data source |
| JTAG | MasterBlaster or ByteBlasterMV download cable or a microprocessor with a Jam Standard Test and Programming Language (STAPL) or JBC File |

For more information on configuration, see *Application Note 116 (Configuring SRAM-Based LUT Devices)*.

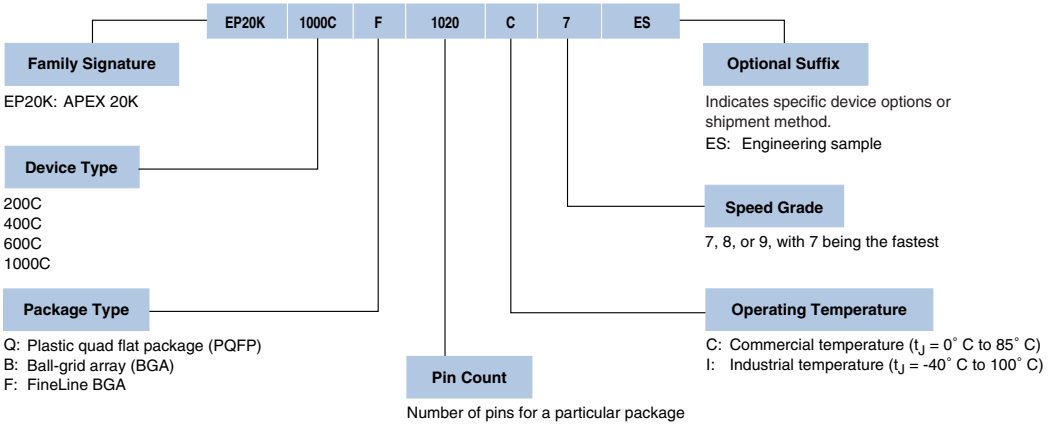
## Device Pin-Outs

See the Altera web site **(http://www.altera.com)** or the ***Altera Digital Library*** for pin-out information.

## Ordering Information

Figure 39 describes the ordering codes for Stratix devices. For more information on a specific package, refer to the *Altera Device Package Information Data Sheet*.

*Figure 39. APEX 20KC Device Packaging Ordering Information*




# Revision History

The information contained in the *APEX 20KC Programmable Logic Device Data Sheet* version 2.2 supersedes information published in previous versions.

## Version 2.2

The following changes were made to the *APEX 20KC Programmable Logic Device Data Sheet* version 2.2:

- Updated Tables 1.
- Updated notes in Tables 20.

## Version 2.1

The following changes were made to the *APEX 20KC Programmable Logic Device Data Sheet* version 2.1:

- Removed figure on AC Test Conditions.
- Updated conditions in Tables 40 and 41.
- Added Tables 42 and 43.
- Updated $V_{OD}$ in Table 27.
- Added Figures 36 through 38.
- Updated Tables 44 through 49.
- Updated Tables 62 through 67.
- Removed notes in Tables 44 through 67.
- Various textual changes throughout the document.

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