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Virtex-6 FPGA Data Sheet: DC and Switching Characteristics

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Product Specification

Virtex-6 FPGA Electrical Characteristics

Virtex®-6 FPGAs are available in -3, -2, -1, and -1L speed grades, with -3 having the highest performance. Virtex-6 FPGA DC and AC characteristics are specified in commercial, extended, industrial, and military temperature ranges. Unless noted, the Virtex-6Q FPGA DC and AC characteristics are equivalent to the commercial specifications. Except for the operating temperature range or unless otherwise noted, all the DC and AC electrical parameters are the same for a particular speed grade (that is, the timing characteristics of a -1 speed grade industrial device are the same as for a -1 speed grade commercial device). However, only selected speed grades and/or devices are available in the extended, industrial, or military temperature ranges.

All supply voltage and junction temperature specifications are representative of worst-case conditions. The parameters included are common to popular designs and typical applications.

Available device and package combinations can be found at:

- [DS150](#): Virtex-6 Family Overview
- [DS155](#): Defense-Grade Virtex-6Q Family Overview

This Virtex-6 FPGA data sheet, part of an overall set of documentation on the Virtex-6 FPGAs, is available on the Xilinx website at: www.xilinx.com/support/index.html/content/xilinx/en/supportNav/silicon_devices/fpga/virtex-6.html.

Virtex-6 FPGA DC Characteristics

Table 1: Absolute Maximum Ratings ⁽¹⁾

| Symbol | Description | Range | Units |
|--------------------------------|--|--------------------------------|-------|
| V _{CCINT} | Internal supply voltage relative to GND | -0.5 to 1.1 | V |
| | For -1L devices: Internal supply voltage relative to GND | -0.5 to 1.0 | V |
| V _{CCAUX} | Auxiliary supply voltage relative to GND | -0.5 to 3.0 | V |
| V _{CCO} | Output drivers supply voltage relative to GND | -0.5 to 3.0 | V |
| V _{BATT} | Key memory battery backup supply | -0.5 to 3.0 | V |
| V _{FS} | External voltage supply for eFUSE programming ⁽²⁾ | -0.5 to 3.0 | V |
| V _{REF} | Input reference voltage | -0.5 to 3.0 | V |
| V _{IN} ⁽³⁾ | 2.5V or below I/O input voltage relative to GND ⁽⁴⁾ (user and dedicated I/Os) | -0.5 to V _{CCO} + 0.5 | V |
| V _{TS} | Voltage applied to 3-state 2.5V or below output ⁽⁴⁾ (user and dedicated I/Os) | -0.5 to V _{CCO} + 0.5 | V |
| T _{STG} | Storage temperature (ambient) | -65 to 150 | °C |
| T _{SOL} | Maximum soldering temperature ⁽⁵⁾ | +220 | °C |
| T _j | Maximum junction temperature ⁽⁵⁾ | +125 | °C |

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. When not programming eFUSE, connect V_{FS} to GND.
3. 2.5V I/O absolute maximum limit applied to DC and AC signals.
4. For I/O operation, refer to [UG361](#): *Virtex-6 FPGA SelectIO Resources User Guide*.
5. For soldering guidelines and thermal considerations, see [UG365](#): *Virtex-6 FPGA Packaging and Pinout Specification*.

Table 2: Recommended Operating Conditions

| Symbol | Description | Min | Max | Units |
|--------------------------------|--|------------|-----------------|--------------------|
| V_{CCINT} | Internal supply voltage relative to GND for all devices except -1L devices. | 0.95 | 1.05 | V |
| | For -1L commercial temperature range devices: internal supply voltage relative to GND, $T_j = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ | 0.87 | 0.93 | V |
| | For -1L industrial temperature range devices: internal supply voltage relative to GND, $T_j = -40^{\circ}\text{C}$ to $+100^{\circ}\text{C}$ | 0.91 | 0.97 | V |
| V_{CCAUX} | Auxiliary supply voltage relative to GND | 2.375 | 2.625 | V |
| V_{CCO} ⁽¹⁾⁽²⁾⁽³⁾ | Supply voltage relative to GND | 1.14 | 2.625 | V |
| V_{IN} | 2.5V supply voltage relative to GND | GND – 0.20 | 2.625 | V |
| | 2.5V and below supply voltage relative to GND | GND – 0.20 | $V_{CCO} + 0.2$ | V |
| I_{IN} ⁽⁵⁾ | Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode. | – | 10 | mA |
| V_{BATT} ⁽⁶⁾ | Battery voltage relative to GND | 1.0 | 2.5 | V |
| V_{FS} ⁽⁷⁾ | External voltage supply for eFUSE programming | 2.375 | 2.625 | V |
| T_j | Junction temperature operating range for commercial (C) temperature devices | 0 | 85 | $^{\circ}\text{C}$ |
| | Junction temperature operating range for extended (E) temperature devices | 0 | 100 | $^{\circ}\text{C}$ |
| | Junction temperature operating range for industrial (I) temperature devices | –40 | 100 | $^{\circ}\text{C}$ |
| | Junction temperature operating range for military (M) temperature devices | –55 | 125 | $^{\circ}\text{C}$ |

Notes:

1. Configuration data is retained even if V_{CCO} drops to 0V.
2. Includes V_{CCO} of 1.2V, 1.5V, 1.8V, and 2.5V.
3. The configuration supply voltage V_{CC_CONFIG} is also known as V_{CCO_0} .
4. All voltages are relative to ground.
5. A total of 100 mA per bank should not be exceeded.
6. V_{BATT} is required only when using bitstream encryption. If battery is not used, connect V_{BATT} to either ground or V_{CCAUX} .
7. During eFUSE programming, V_{FS} must be within the recommended operating range and $T_j = +15^{\circ}\text{C}$ to $+85^{\circ}\text{C}$. Otherwise, V_{FS} can be connected to GND.

Table 3: DC Characteristics Over Recommended Operating Conditions (1)(2)

| Symbol | Description | Min | Typ | Max | Units |
|----------------|---|------|--------|-----|----------|
| V_{DRINT} | Data retention V_{CCINT} voltage (below which configuration data might be lost) | 0.75 | – | – | V |
| V_{DRI} | Data retention V_{CCAUX} voltage (below which configuration data might be lost) | 2.0 | – | – | V |
| I_{REF} | V_{REF} leakage current per pin | – | – | 10 | μ A |
| I_L | Input or output leakage current per pin (sample-tested) | – | – | 10 | μ A |
| $C_{IN}^{(3)}$ | Die input capacitance at the pad | – | – | 8 | pF |
| I_{RPU} | Pad pull-up (when selected) @ $V_{IN} = 0V$, $V_{CCO} = 2.5V$ | 20 | – | 80 | μ A |
| | Pad pull-up (when selected) @ $V_{IN} = 0V$, $V_{CCO} = 1.8V$ | 8 | – | 40 | μ A |
| | Pad pull-up (when selected) @ $V_{IN} = 0V$, $V_{CCO} = 1.5V$ | 5 | – | 30 | μ A |
| | Pad pull-up (when selected) @ $V_{IN} = 0V$, $V_{CCO} = 1.2V$ | 1 | – | 20 | μ A |
| I_{RPD} | Pad pull-down (when selected) @ $V_{IN} = 2.5V$ | 3 | – | 80 | μ A |
| I_{BATT} | Battery supply current | – | – | 150 | nA |
| n | Temperature diode ideality factor | – | 1.0002 | – | n |
| r | Series resistance | – | 5 | – | Ω |

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. Maximum value specified for worst case process at 25°C.
3. This measurement represents the die capacitance at the pad, not including the package.

Important Note

Typical values for quiescent supply current are specified at nominal voltage, 85°C junction temperatures (T_j). Xilinx recommends analyzing static power consumption at $T_j = 85^\circ\text{C}$ because the majority of designs operate near the high end of the commercial temperature range. Quiescent supply current is specified by speed grade for Virtex-6 devices. Use the Xilinx Power Estimator (XPE) spreadsheet tool (download at <http://www.xilinx.com/power>) to calculate static power consumption for conditions other than those specified in Table 4.

Table 4: Typical Quiescent Supply Current

| Symbol | Description | Device | Speed and Temperature Grade | | | | | Units | |
|--------------|--------------------------------------|---------------------------|-----------------------------|----------------|------------|---------------------------|---------|-------|------------------------|
| | | | -3 (C) | -2 (C, E, & I) | -1 (C & I) | -1 (I & M) ⁽²⁾ | -1L (C) | | -1L (I) ⁽¹⁾ |
| I_{CCINTQ} | Quiescent V_{CCINT} supply current | XC6VLX75T | 927 | 927 | 927 | N/A | 656 | 741 | mA |
| | | XC6VLX130T | 1563 | 1563 | 1563 | N/A | 1102 | 1245 | mA |
| | | XC6VLX195T | 2059 | 2059 | 2059 | N/A | 1441 | 1628 | mA |
| | | XC6VLX240T | 2478 | 2478 | 2478 | N/A | 1733 | 1957 | mA |
| | | XC6VLX365T | 3001 | 3001 | 3001 | N/A | 2092 | 2363 | mA |
| | | XC6VLX550T ⁽³⁾ | N/A | 4515 | 4515 | N/A | 3147 | 3555 | mA |
| | | XC6VLX760 ⁽³⁾ | N/A | 5094 | 5094 | N/A | 3471 | 3921 | mA |
| | | XC6VSX315T | 3476 | 3476 | 3476 | N/A | 2409 | 2721 | mA |
| | | XC6VSX475T ⁽³⁾ | N/A | 5227 | 5227 | N/A | 3622 | 4091 | mA |
| | | XC6VHX250T | 2906 | 2906 | 2906 | N/A | N/A | N/A | mA |
| | | XC6VHX255T | 2746 | 2746 | 2746 | N/A | N/A | N/A | mA |
| | | XC6VHX380T ⁽⁴⁾ | 4160 | 4160 | 4160 | N/A | N/A | N/A | mA |
| | | XC6VHX565T ⁽⁵⁾ | N/A | 5207 | 5207 | N/A | N/A | N/A | mA |
| | | XQ6VLX130T | N/A | 1563 | N/A | 1563 | N/A | 1245 | mA |
| | | XQ6VLX240T | N/A | 2478 | N/A | 2478 | N/A | 1957 | mA |
| | | XQ6VLX550T ⁽⁷⁾ | N/A | N/A | N/A | 4515 | N/A | 3555 | mA |
| | | XQ6VSX315T | N/A | 3476 | N/A | 3476 | N/A | 2721 | mA |
| | | XQ6VSX475T ⁽⁷⁾ | N/A | N/A | N/A | 5227 | N/A | 4091 | mA |

Table 4: Typical Quiescent Supply Current (Cont'd)

| Symbol | Description | Device | Speed and Temperature Grade | | | | | Units | |
|-------------------|---|---------------------------|-----------------------------|----------------|------------|---------------------------|---------|-------|------------------------|
| | | | -3 (C) | -2 (C, E, & I) | -1 (C & I) | -1 (I & M) ⁽²⁾ | -1L (C) | | -1L (I) ⁽¹⁾ |
| I _{CCOQ} | Quiescent V _{CCO} supply current | XC6VLX75T | 1 | 1 | 1 | N/A | 1 | 1 | mA |
| | | XC6VLX130T | 1 | 1 | 1 | N/A | 1 | 1 | mA |
| | | XC6VLX195T | 1 | 1 | 1 | N/A | 1 | 1 | mA |
| | | XC6VLX240T | 2 | 2 | 2 | N/A | 2 | 2 | mA |
| | | XC6VLX365T | 2 | 2 | 2 | N/A | 2 | 2 | mA |
| | | XC6VLX550T ⁽³⁾ | N/A | 3 | 3 | N/A | 3 | 3 | mA |
| | | XC6VLX760 ⁽³⁾ | N/A | 3 | 3 | N/A | 3 | 3 | mA |
| | | XC6VSX315T | 2 | 2 | 2 | N/A | 2 | 2 | mA |
| | | XC6VSX475T ⁽³⁾ | N/A | 2 | 2 | N/A | 2 | 2 | mA |
| | | XC6VHX250T | 1 | 1 | 1 | N/A | N/A | N/A | mA |
| | | XC6VHX255T | 1 | 1 | 1 | N/A | N/A | N/A | mA |
| | | XC6VHX380T ⁽⁴⁾ | 2 | 2 | 2 | N/A | N/A | N/A | mA |
| | | XC6VHX565T ⁽⁵⁾ | N/A | 2 | 2 | N/A | N/A | N/A | mA |
| | | XQ6VLX130T | N/A | 1 | N/A | 1 | N/A | 1 | mA |
| | | XQ6VLX240T | N/A | 2 | N/A | 2 | N/A | 2 | mA |
| | | XQ6VLX550T ⁽⁷⁾ | N/A | N/A | N/A | 3 | N/A | 3 | mA |
| | | XQ6VSX315T | N/A | 2 | N/A | 2 | N/A | 2 | mA |
| | | XQ6VSX475T ⁽⁷⁾ | N/A | N/A | N/A | 2 | N/A | 2 | mA |

Table 4: Typical Quiescent Supply Current (Cont'd)

| Symbol | Description | Device | Speed and Temperature Grade | | | | | Units | |
|---------------------|---|---------------------------|-----------------------------|----------------|------------|---------------------------|---------|-------|------------------------|
| | | | -3 (C) | -2 (C, E, & I) | -1 (C & I) | -1 (I & M) ⁽²⁾ | -1L (C) | | -1L (I) ⁽¹⁾ |
| I _{CCAUXQ} | Quiescent V _{CCAUX} supply current | XC6VLX75T | 45 | 45 | 45 | N/A | 45 | 45 | mA |
| | | XC6VLX130T | 75 | 75 | 75 | N/A | 75 | 75 | mA |
| | | XC6VLX195T | 113 | 113 | 113 | N/A | 113 | 113 | mA |
| | | XC6VLX240T | 135 | 135 | 135 | N/A | 135 | 135 | mA |
| | | XC6VLX365T | 191 | 191 | 191 | N/A | 191 | 191 | mA |
| | | XC6VLX550T ⁽³⁾ | N/A | 286 | 286 | N/A | 286 | 286 | mA |
| | | XC6VLX760 ⁽³⁾ | N/A | 387 | 387 | N/A | 387 | 387 | mA |
| | | XC6VSX315T | 186 | 186 | 186 | N/A | 186 | 186 | mA |
| | | XC6VSX475T ⁽³⁾ | N/A | 279 | 279 | N/A | 279 | 279 | mA |
| | | XC6VHX250T | 152 | 152 | 152 | N/A | N/A | N/A | mA |
| | | XC6VHX255T | 152 | 152 | 152 | N/A | N/A | N/A | mA |
| | | XC6VHX380T ⁽⁴⁾ | 227 | 227 | 227 | N/A | N/A | N/A | mA |
| | | XC6VHX565T ⁽⁵⁾ | N/A | 315 | 315 | N/A | N/A | N/A | mA |
| | | XQ6VLX130T ⁽⁶⁾ | N/A | 75 | N/A | 75 | N/A | 75 | mA |
| | | XQ6VLX240T ⁽⁶⁾ | N/A | 135 | N/A | 135 | N/A | 135 | mA |
| | | XQ6VLX550T ⁽⁷⁾ | N/A | N/A | N/A | 286 | N/A | 286 | mA |
| | | XQ6VSX315T ⁽⁶⁾ | N/A | 186 | N/A | 186 | N/A | 186 | mA |
| | | XQ6VSX475T ⁽⁷⁾ | N/A | N/A | N/A | 279 | N/A | 279 | mA |

Notes:

1. Typical values are specified at nominal voltage, 85°C junction temperatures (T_j). -1 and -2 industrial (I) grade devices have the same typical values as commercial (C) grade devices at 85°C, but higher values at 100°C. Use the XPE tool to calculate 100°C values. -1L industrial temperature range devices have the values specified in this column.
2. Use the XPE tool to calculate 125°C values for -1M temperature range devices.
3. The -2E extended temperature range (T_j = 0°C to +100°C) is only available in these devices. The -2I temperature range (T_j = -40°C to +100°C) is available for all other devices except the XC6VHX565T.
4. The XC6VHX380T is available with both -2E and -2I temperature ranges.
5. The XC6VHX565T is only available in the following temperature ranges: -1C, -1I, -2C, and -2E.
6. The XQ6VLX130T, XQ6VLX240T, and XQ6VSX315T are available in -2I, -1I, -1M, and -1LI temperature ranges.
7. The XQ6VLX550T and the XQ6VSX475T are only available in -1I and -1LI temperature ranges.
8. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
9. If DCI or differential signaling is used, more accurate quiescent current estimates can be obtained by using the XPE or XPower Analyzer (XPA) tools.

Power-On Power Supply Requirements

Xilinx FPGAs require a certain amount of supply current during power-on to insure proper device initialization. The actual current consumed depends on the power-on sequence and ramp rate of the power supply.

The recommended power-on sequence for Virtex-6 devices is V_{CCINT}, V_{CCAUX}, and V_{CCO} to meet the power-up current requirements listed in Table 5. V_{CCINT} can be powered up or down at any time, but power up current specifications can vary from Table 5. The device will have no physical damage or reliability concerns if V_{CCINT}, V_{CCAUX}, and V_{CCO} sequence cannot be followed.

If the recommended power-up sequence cannot be followed and the I/Os must remain 3-stated throughout configuration, then V_{CCAUX} must be powered prior to V_{CCO} or V_{CCAUX} and V_{CCO} must be powered by the same supply. Similarly, for power-down, the reverse V_{CCAUX} and V_{CCO} sequence is recommended if the I/Os are to remain 3-stated.

The GTH transceiver supplies must be powered using a MGTHAVCC, MGTHAVCCR_X, MGTHAVCCPLL, and MGTHAVTT sequence. There are no sequencing requirements for these supplies with respect to the other FPGA supply voltages. For more detail see [Table 27: GTH Transceiver Power Supply Sequencing](#). There are no sequencing requirements for the GTX transceivers power supplies.

[Table 5](#) shows the minimum current, in addition to I_{CCQ} , that are required by Virtex-6 devices for proper power-on and configuration. If the current minimums shown in [Table 4](#) and [Table 5](#) are met, the device powers on after all three supplies have passed through their power-on reset threshold voltages. The FPGA must be configured after applying V_{CCINT} , V_{CCAUX} , and V_{CCO} for the appropriate configuration banks. Once initialized and configured, use the XPE tools to estimate current drain on these supplies.

Table 5: Power-On Current for Virtex-6 Devices

| Device | $I_{CCINTMIN}$ | $I_{CCAUXMIN}$ | I_{CCOMIN} | Units |
|------------|---|--------------------|-----------------------------|-------|
| | Typ ⁽¹⁾ | Typ ⁽¹⁾ | Typ ⁽¹⁾ | |
| XC6VLX75T | See I_{CCINTQ} in Table 4 | $I_{CCAUXQ} + 10$ | $I_{CCOQ} + 30$ mA per bank | mA |
| XC6VLX130T | See I_{CCINTQ} in Table 4 | $I_{CCAUXQ} + 10$ | $I_{CCOQ} + 30$ mA per bank | mA |
| XC6VLX195T | See I_{CCINTQ} in Table 4 | $I_{CCAUXQ} + 40$ | $I_{CCOQ} + 30$ mA per bank | mA |
| XC6VLX240T | See I_{CCINTQ} in Table 4 | $I_{CCAUXQ} + 40$ | $I_{CCOQ} + 30$ mA per bank | mA |
| XC6VLX365T | See I_{CCINTQ} in Table 4 | $I_{CCAUXQ} + 40$ | $I_{CCOQ} + 30$ mA per bank | mA |
| XC6VLX550T | See I_{CCINTQ} in Table 4 | $I_{CCAUXQ} + 40$ | $I_{CCOQ} + 30$ mA per bank | mA |
| XC6VLX760 | See I_{CCINTQ} in Table 4 | $I_{CCAUXQ} + 40$ | $I_{CCOQ} + 30$ mA per bank | mA |
| XC6VSX315T | See I_{CCINTQ} in Table 4 | $I_{CCAUXQ} + 40$ | $I_{CCOQ} + 30$ mA per bank | mA |
| XC6VSX475T | See I_{CCINTQ} in Table 4 | $I_{CCAUXQ} + 50$ | $I_{CCOQ} + 30$ mA per bank | mA |
| XC6VHX250T | See I_{CCINTQ} in Table 4 | $I_{CCAUXQ} + 40$ | $I_{CCOQ} + 30$ mA per bank | mA |
| XC6VHX255T | See I_{CCINTQ} in Table 4 | $I_{CCAUXQ} + 40$ | $I_{CCOQ} + 30$ mA per bank | mA |
| XC6VHX380T | See I_{CCINTQ} in Table 4 | $I_{CCAUXQ} + 40$ | $I_{CCOQ} + 30$ mA per bank | mA |
| XC6VHX565T | See I_{CCINTQ} in Table 4 | $I_{CCAUXQ} + 40$ | $I_{CCOQ} + 30$ mA per bank | mA |
| XQ6VLX130T | See I_{CCINTQ} in Table 4 | $I_{CCAUXQ} + 100$ | $I_{CCOQ} + 30$ mA per bank | mA |
| XQ6VLX240T | See I_{CCINTQ} in Table 4 | $I_{CCAUXQ} + 100$ | $I_{CCOQ} + 30$ mA per bank | mA |
| XQ6VLX550T | See I_{CCINTQ} in Table 4 | $I_{CCAUXQ} + 100$ | $I_{CCOQ} + 30$ mA per bank | mA |
| XQ6VSX315T | See I_{CCINTQ} in Table 4 | $I_{CCAUXQ} + 100$ | $I_{CCOQ} + 40$ mA per bank | mA |
| XQ6VSX475T | See I_{CCINTQ} in Table 4 | $I_{CCAUXQ} + 100$ | $I_{CCOQ} + 40$ mA per bank | mA |

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. Use the Xilinx Power Estimator (XPE) spreadsheet tool (download at <http://www.xilinx.com/power>) to calculate maximum power-on currents.

Table 6: Power Supply Ramp Time

| Symbol | Description | Ramp Time | Units |
|-------------|---|--------------|-------|
| V_{CCINT} | Internal supply voltage relative to GND | 0.20 to 50.0 | ms |
| V_{CCO} | Output drivers supply voltage relative to GND | 0.20 to 50.0 | ms |
| V_{CCAUX} | Auxiliary supply voltage relative to GND | 0.20 to 50.0 | ms |

SelectIO™ DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 7: SelectIO DC Input and Output Levels

| I/O Standard | V_{IL} | | V_{IH} | | V_{OL} | V_{OH} | I_{OL} | I_{OH} |
|-----------------------------|----------|-----------------------|-----------------------|-----------------|------------------|------------------|----------|----------|
| | V, Min | V, Max | V, Min | V, Max | V, Max | V, Min | mA | mA |
| LVC MOS25, LVDCI25 | -0.3 | 0.7 | 1.7 | $V_{CCO} + 0.3$ | 0.4 | $V_{CCO} - 0.4$ | Note(3) | Note(3) |
| LVC MOS18, LVDCI18 | -0.3 | 35% V_{CCO} | 65% V_{CCO} | $V_{CCO} + 0.3$ | 0.45 | $V_{CCO} - 0.45$ | Note(4) | Note(4) |
| LVC MOS15, LVDCI15 | -0.3 | 35% V_{CCO} | 65% V_{CCO} | $V_{CCO} + 0.3$ | 25% V_{CCO} | 75% V_{CCO} | Note(4) | Note(4) |
| LVC MOS12 | -0.3 | 35% V_{CCO} | 65% V_{CCO} | $V_{CCO} + 0.3$ | 25% V_{CCO} | 75% V_{CCO} | Note(5) | Note(5) |
| HSTL I ₁₂ | -0.3 | $V_{REF} - 0.1$ | $V_{REF} + 0.1$ | $V_{CCO} + 0.3$ | 25% V_{CCO} | 75% V_{CCO} | 6.3 | -6.3 |
| HSTL I ⁽²⁾ | -0.3 | $V_{REF} - 0.1$ | $V_{REF} + 0.1$ | $V_{CCO} + 0.3$ | 0.4 | $V_{CCO} - 0.4$ | 8 | -8 |
| HSTL II ⁽²⁾ | -0.3 | $V_{REF} - 0.1$ | $V_{REF} + 0.1$ | $V_{CCO} + 0.3$ | 0.4 | $V_{CCO} - 0.4$ | 16 | -16 |
| HSTL III ⁽²⁾ | -0.3 | $V_{REF} - 0.1$ | $V_{REF} + 0.1$ | $V_{CCO} + 0.3$ | 0.4 | $V_{CCO} - 0.4$ | 24 | -8 |
| DIFF HSTL I ⁽²⁾ | -0.3 | 50% $V_{CCO} - 0.1$ | 50% $V_{CCO} + 0.1$ | $V_{CCO} + 0.3$ | - | - | - | - |
| DIFF HSTL II ⁽²⁾ | -0.3 | 50% $V_{CCO} - 0.1$ | 50% $V_{CCO} + 0.1$ | $V_{CCO} + 0.3$ | - | - | - | - |
| SSTL2 I | -0.3 | $V_{REF} - 0.15$ | $V_{REF} + 0.15$ | $V_{CCO} + 0.3$ | $V_{TT} - 0.61$ | $V_{TT} + 0.61$ | 8.1 | -8.1 |
| SSTL2 II | -0.3 | $V_{REF} - 0.15$ | $V_{REF} + 0.15$ | $V_{CCO} + 0.3$ | $V_{TT} - 0.81$ | $V_{TT} + 0.81$ | 16.2 | -16.2 |
| DIFF SSTL2 I | -0.3 | 50% $V_{CCO} - 0.15$ | 50% $V_{CCO} + 0.15$ | $V_{CCO} + 0.3$ | - | - | - | - |
| DIFF SSTL2 II | -0.3 | 50% $V_{CCO} - 0.15$ | 50% $V_{CCO} + 0.15$ | $V_{CCO} + 0.3$ | - | - | - | - |
| SSTL18 I | -0.3 | $V_{REF} - 0.125$ | $V_{REF} + 0.125$ | $V_{CCO} + 0.3$ | $V_{TT} - 0.47$ | $V_{TT} + 0.47$ | 6.7 | -6.7 |
| SSTL18 II | -0.3 | $V_{REF} - 0.125$ | $V_{REF} + 0.125$ | $V_{CCO} + 0.3$ | $V_{TT} - 0.60$ | $V_{TT} + 0.60$ | 13.4 | -13.4 |
| DIFF SSTL18 I | -0.3 | 50% $V_{CCO} - 0.125$ | 50% $V_{CCO} + 0.125$ | $V_{CCO} + 0.3$ | - | - | - | - |
| DIFF SSTL18 II | -0.3 | 50% $V_{CCO} - 0.125$ | 50% $V_{CCO} + 0.125$ | $V_{CCO} + 0.3$ | - | - | - | - |
| SSTL15 | -0.3 | $V_{REF} - 0.1$ | $V_{REF} + 0.1$ | $V_{CCO} + 0.3$ | $V_{TT} - 0.175$ | $V_{TT} + 0.175$ | 14.3 | -14.3 |
| DIFF SSTL15 | -0.3 | 50% $V_{CCO} - 0.1$ | 50% $V_{CCO} + 0.1$ | $V_{CCO} + 0.3$ | - | - | - | - |

Notes:

1. Tested according to relevant specifications.
2. Applies to both 1.5V and 1.8V HSTL.
3. Using drive strengths of 2, 4, 6, 8, 12, 16, or 24 mA.
4. Using drive strengths of 2, 4, 6, 8, 12, or 16 mA.
5. Supported drive strengths of 2, 4, 6, or 8 mA.
6. For detailed interface specific DC voltage levels, see [UG361](#): Virtex-6 FPGA SelectIO Resources User Guide.

HT DC Specifications (HT_25)

Table 8: HT DC Specifications

| Symbol | DC Parameter | Conditions | Min | Typ | Max | Units |
|------------------|--|---|------|-----|------|-------|
| V_{CCO} | Supply Voltage | | 2.38 | 2.5 | 2.63 | V |
| V_{OD} | Differential Output Voltage for XC devices | $R_T = 100 \Omega$ across Q and \bar{Q} signals | 480 | 600 | 885 | mV |
| | Differential Output Voltage for XQ devices | | 480 | 600 | 930 | mV |
| ΔV_{OD} | Change in V_{OD} Magnitude | | -15 | - | 15 | mV |
| V_{OCM} | Output Common Mode Voltage | $R_T = 100 \Omega$ across Q and \bar{Q} signals | 440 | 600 | 760 | mV |
| ΔV_{OCM} | Change in V_{OCM} Magnitude | | -15 | - | 15 | mV |
| V_{ID} | Input Differential Voltage | | 200 | 600 | 1000 | mV |
| ΔV_{ID} | Change in V_{ID} Magnitude | | -15 | - | 15 | mV |
| V_{ICM} | Input Common Mode Voltage | | 440 | 600 | 780 | mV |
| ΔV_{ICM} | Change in V_{ICM} Magnitude | | -15 | - | 15 | mV |

LVDS DC Specifications (LVDS_25)

Table 9: LVDS DC Specifications

| Symbol | DC Parameter | Conditions | Min | Typ | Max | Units |
|-------------|---|---|-------|-------|-------|-------|
| V_{CCO} | Supply Voltage | | 2.38 | 2.5 | 2.63 | V |
| V_{OH} | Output High Voltage for Q and \bar{Q} | $R_T = 100 \Omega$ across Q and \bar{Q} signals | - | - | 1.675 | V |
| V_{OL} | Output Low Voltage for Q and \bar{Q} | $R_T = 100 \Omega$ across Q and \bar{Q} signals | 0.825 | - | - | V |
| V_{ODIFF} | Differential Output Voltage (Q - \bar{Q}), Q = High ($\bar{Q} - Q$), \bar{Q} = High | $R_T = 100 \Omega$ across Q and \bar{Q} signals | 247 | 350 | 600 | mV |
| V_{OCM} | Output Common-Mode Voltage for XC devices | $R_T = 100 \Omega$ across Q and \bar{Q} signals | 1.075 | 1.250 | 1.425 | V |
| | Output Common-Mode Voltage for XQ devices | | 1.000 | 1.250 | 1.425 | V |
| V_{IDIFF} | Differential Input Voltage (Q - \bar{Q}), Q = High ($\bar{Q} - Q$), \bar{Q} = High | | 100 | 350 | 600 | mV |
| V_{ICM} | Input Common-Mode Voltage | | 0.3 | 1.2 | 2.2 | V |

Extended LVDS DC Specifications (LVDSEXT_25)

Table 10: Extended LVDS DC Specifications

| Symbol | DC Parameter | Conditions | Min | Typ | Max | Units |
|-------------|---|---|-------|-------|-------|-------|
| V_{CCO} | Supply Voltage | | 2.38 | 2.5 | 2.63 | V |
| V_{OH} | Output High Voltage for Q and \bar{Q} | $R_T = 100 \Omega$ across Q and \bar{Q} signals | - | - | 1.785 | V |
| V_{OL} | Output Low Voltage for Q and \bar{Q} | $R_T = 100 \Omega$ across Q and \bar{Q} signals | 0.715 | - | - | V |
| V_{ODIFF} | Differential Output Voltage (Q - \bar{Q}), Q = High ($\bar{Q} - Q$), \bar{Q} = High for XC devices | $R_T = 100 \Omega$ across Q and \bar{Q} signals | 350 | - | 840 | mV |
| | Differential Output Voltage (Q - \bar{Q}), Q = High ($\bar{Q} - Q$), \bar{Q} = High for XQ devices | | 350 | - | 850 | mV |
| V_{OCM} | Output Common-Mode Voltage for XC devices | $R_T = 100 \Omega$ across Q and \bar{Q} signals | 1.075 | 1.250 | 1.425 | V |
| | Output Common-Mode Voltage for XQ devices | | 1.000 | 1.250 | 1.425 | V |
| V_{IDIFF} | Differential Input Voltage (Q - \bar{Q}), Q = High ($\bar{Q} - Q$), \bar{Q} = High | Common-mode input voltage = 1.25V | 100 | - | 1000 | mV |
| V_{ICM} | Input Common-Mode Voltage | Differential input voltage = ± 350 mV | 0.3 | 1.2 | 2.2 | V |

LVPECL DC Specifications (LVPECL_25)

These values are valid when driving a 100Ω differential load only, i.e., a 100Ω resistor between the two receiver pins. The V_{OH} levels are 200 mV below standard LVPECL levels and are compatible with devices tolerant of lower common-mode ranges. [Table 11](#) summarizes the DC output specifications of LVPECL. For more information on using LVPECL, see [UG361: Virtex-6 FPGA SelectIO Resources User Guide](#).

Table 11: LVPECL DC Specifications

| Symbol | DC Parameter | Min | Typ | Max | Units |
|------------|--|------------------|-------|-----------------|-------|
| V_{OH} | Output High Voltage | $V_{CC} - 1.025$ | 1.545 | $V_{CC} - 0.88$ | V |
| V_{OL} | Output Low Voltage | $V_{CC} - 1.81$ | 0.795 | $V_{CC} - 1.62$ | V |
| V_{ICM} | Input Common-Mode Voltage | 0.6 | – | 2.2 | V |
| V_{DIFF} | Differential Input Voltage ⁽¹⁾⁽²⁾ | 0.100 | – | 1.5 | V |

Notes:

1. Recommended input maximum voltage not to exceed $V_{CCAUX} + 0.2V$.
2. Recommended input minimum voltage not to go below $-0.5V$.

eFUSE Read Endurance

[Table 12](#) lists the maximum number of read cycle operations expected. For more information, see [UG360: Virtex-6 FPGA Configuration User Guide](#).

Table 12: eFUSE Read Endurance

| Symbol | Description | Speed Grade | | | | Units |
|------------|---|-------------|----|----|-----|-------------|
| | | -3 | -2 | -1 | -1L | |
| DNA_CYCLES | Number of DNA_PORT READ operations or JTAG ISC_DNA read command operations. Unaffected by SHIFT operations. | 30,000,000 | | | | Read Cycles |
| AES_CYCLES | Number of JTAG FUSE_KEY or FUSE_CNTL read command operations. Unaffected by SHIFT operations. | 30,000,000 | | | | Read Cycles |

GTX Transceiver Specifications

GTX Transceiver DC Characteristics

Table 13: Absolute Maximum Ratings for GTX Transceivers⁽¹⁾

| Symbol | Description | Min | Max | Units |
|------------------------|---|------|------|-------|
| MGTAVCC | Analog supply voltage for the GTX transmitter and receiver circuits relative to GND | -0.5 | 1.1 | V |
| MGTAVTT | Analog supply voltage for the GTX transmitter and receiver termination circuits relative to GND | -0.5 | 1.32 | V |
| MGTAVTTRCAL | Analog supply voltage for the resistor calibration circuit of the GTX transceiver column | -0.5 | 1.32 | V |
| V _{IN} | Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage | -0.5 | 1.32 | V |
| V _{MGTREFCLK} | Reference clock absolute input voltage | -0.5 | 1.32 | V |

Notes:

- Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.

Table 14: Recommended Operating Conditions for GTX Transceivers⁽¹⁾⁽²⁾

| Symbol | Description | Speed Grade | PLL Frequency | Min | Typ | Max | Units |
|-------------|---|-----------------------|---------------|------|------|------|-------|
| MGTAVCC | Analog supply voltage for the GTX transmitter and receiver circuits relative to GND | -3, -2 ⁽³⁾ | > 2.7 GHz | 1.0 | 1.03 | 1.06 | V |
| | | -3, -2 ⁽³⁾ | ≤ 2.7 GHz | 0.95 | 1.0 | 1.06 | V |
| | | -1 | ≤ 2.7 GHz | 0.95 | 1.0 | 1.06 | V |
| | | -1L | ≤ 2.7 GHz | 0.95 | 1.0 | 1.05 | V |
| MGTAVTT | Analog supply voltage for the GTX transmitter and receiver termination circuits relative to GND | All | – | 1.14 | 1.2 | 1.26 | V |
| MGTAVTTRCAL | Analog supply voltage for the resistor calibration circuit of the GTX transceiver column | All | – | 1.14 | 1.2 | 1.26 | V |

Notes:

- Each voltage listed requires the filter circuit described in [UG366: Virtex-6 FPGA GTX Transceivers User Guide](#).
- Voltages are specified for the temperature range of T_j = -40°C to +100°C for all XC devices and T_j = -55°C to +125°C for the XQ devices
- If a GTX Quad contains transceivers operating with a mixture of PLL frequencies above and below 2.7 GHz, the MGTAVCC voltage supply must be in the range of 1.0V to 1.06V.

Table 15: GTX Transceiver Supply Current (per Lane) ⁽¹⁾⁽²⁾

| Symbol | Description | Typ | Max | Units |
|----------------------|---|----------------------|--------|-------|
| I _{MGTAVTT} | MGTAVTT supply current for one GTX transceiver | 55.9 | Note 2 | mA |
| I _{MGTAVCC} | MGTAVCC supply current for one GTX transceiver | 56.1 | | mA |
| MGTR _{REF} | Precision reference resistor for internal calibration termination | 100.0 ± 1% tolerance | | Ω |

Notes:

- Typical values are specified at nominal voltage, 25°C, with a 3.125 Gb/s line rate.
- Values for currents of other transceiver configurations and conditions can be obtained by using the Xilinx Power Estimator (XPE) or XPower Analyzer (XPA) tools.

Table 16: GTX Transceiver Quiescent Supply Current (per Lane) (1)(2)(3)

| Symbol | Description | Typ ⁽⁴⁾ | Max | Units |
|-----------------------|---|--------------------|--------|-------|
| I _{MGTAVTTQ} | Quiescent MGTA VTT supply current for one GTX transceiver | 0.9 | Note 2 | mA |
| I _{MGTAVCCQ} | Quiescent MGTA VCC supply current for one GTX transceiver | 3.5 | | mA |

Notes:

1. Device powered and unconfigured.
2. Currents for conditions other than values specified in this table can be obtained by using the XPE or XPA tools.
3. GTX transceiver quiescent supply current for an entire device can be calculated by multiplying the values in this table by the number of available GTX transceivers.
4. Typical values are specified at nominal voltage, 25°C.

GTX Transceiver DC Input and Output Levels

Table 17 summarizes the DC output specifications of the GTX transceivers in Virtex-6 FPGAs. Consult [UG366: Virtex-6 FPGA GTX Transceivers User Guide](#) for further details.

Table 17: GTX Transceiver DC Specifications

| Symbol | DC Parameter | Conditions | Min | Typ | Max | Units |
|----------------------|---|--|-----------------------------------|--------------|----------|-------|
| DV _{PPIN} | Differential peak-to-peak input voltage | External AC coupled ≤ 4.25 Gb/s | 125 | – | 2000 | mV |
| | | External AC coupled > 4.25 Gb/s | 175 | – | 2000 | mV |
| V _{IN} | Absolute input voltage | DC coupled MGTA VTT = 1.2V | –400 | – | MGTA VTT | mV |
| V _{CMIN} | Common mode input voltage | DC coupled MGTA VTT = 1.2V | – | 2/3 MGTA VTT | – | mV |
| DV _{PPOUT} | Differential peak-to-peak output voltage ⁽¹⁾ | Transmitter output swing is set to maximum setting | – | – | 1000 | mV |
| V _{CMOUTDC} | DC common mode output voltage. | Equation based | MGTA VTT – DV _{PPOUT} /4 | | | mV |
| R _{IN} | Differential input resistance | | 80 | 100 | 130 | Ω |
| R _{OUT} | Differential output resistance | | 80 | 100 | 120 | Ω |
| T _{OSKEW} | Transmitter output pair (TXP and TXN) intra-pair skew | | – | 2 | 8 | ps |
| C _{EXT} | Recommended external AC coupling capacitor ⁽²⁾ | | – | 100 | – | nF |

Notes:

1. The output swing and preemphasis levels are programmable using the attributes discussed in [UG366: Virtex-6 FPGA GTX Transceivers User Guide](#) and can result in values lower than reported in this table.
2. Other values can be used as appropriate to conform to specific protocols and standards.



Figure 1: Single-Ended Peak-to-Peak Voltage

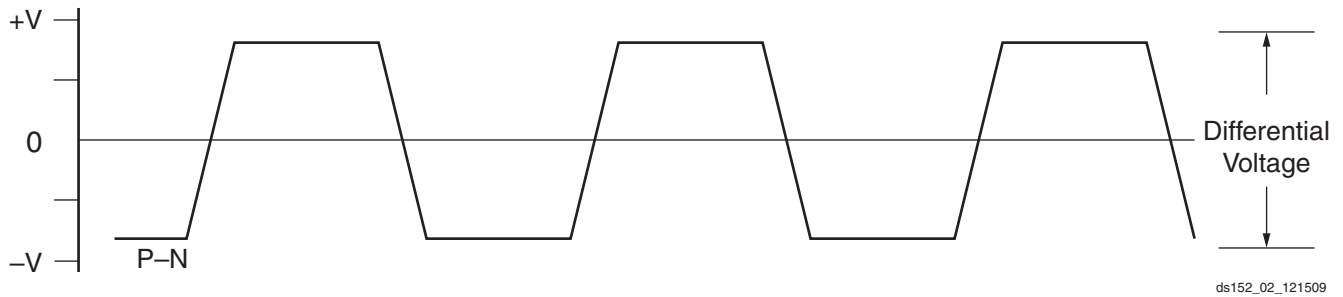


Figure 2: Differential Peak-to-Peak Voltage

Table 18 summarizes the DC specifications of the clock input of the GTX transceiver. Consult [UG366: Virtex-6 FPGA GTX Transceivers User Guide](#) for further details.

Table 18: GTX Transceiver Clock DC Input Level Specification

| Symbol | DC Parameter | Min | Typ | Max | Units |
|--------------------|--|-----|-----|------|-------|
| V _{IDIFF} | Differential peak-to-peak input voltage | 210 | 800 | 2000 | mV |
| R _{IN} | Differential input resistance | 90 | 100 | 130 | Ω |
| C _{EXT} | Required external AC coupling capacitor ⁽¹⁾ | – | 100 | – | nF |

Notes:

1. Other values can be used as appropriate to conform to specific protocols and standards.

GTX Transceiver Switching Characteristics

Consult [UG366: Virtex-6 FPGA GTX Transceivers User Guide](#) for further information.

Table 19: GTX Transceiver Performance

| Symbol | Description | Speed Grade | | | | Units |
|----------------------|-----------------------------------|--------------------|--------------------|-----|-----|-------|
| | | -3 | -2 | -1 | -1L | |
| F _{GTXMAX} | Maximum GTX transceiver data rate | 6.6 | 6.6 | 5.0 | 5.0 | Gb/s |
| F _{GPLLMAX} | Maximum PLL frequency | 3.3 ⁽¹⁾ | 3.3 ⁽¹⁾ | 2.7 | 2.7 | GHz |
| F _{GPLLMIN} | Minimum PLL frequency | 1.2 | 1.2 | 1.2 | 1.2 | GHz |

Notes:

1. See Table 14 for MGTAVCC requirements when PLL frequency is greater than 2.7 GHz.

Table 20: GTX Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics

| Symbol | Description | Speed Grade | | | | Units |
|------------------------|-----------------------------|-------------|-----|-----|-----|-------|
| | | -3 | -2 | -1 | -1L | |
| F _{GTXDRPCLK} | GTXDRPCLK maximum frequency | 150 | 150 | 125 | 100 | MHz |

Table 21: GTX Transceiver Reference Clock Switching Characteristics

| Symbol | Description | Conditions | All Speed Grades | | | Units |
|--------------------|---|--|------------------|-----|-----|-------|
| | | | Min | Typ | Max | |
| F _{GCLK} | Reference clock frequency range | | 62.5 | – | 650 | MHz |
| T _{RCLK} | Reference clock rise time | 20% – 80% | – | 200 | – | ps |
| T _{FCLK} | Reference clock fall time | 80% – 20% | – | 200 | – | ps |
| T _{DCREF} | Reference clock duty cycle | Transceiver PLL only | 45 | 50 | 55 | % |
| T _{LOCK} | Clock recovery frequency acquisition time | Initial PLL lock | – | – | 1 | ms |
| T _{PHASE} | Clock recovery phase acquisition time | Lock to data after PLL has locked to the reference clock | – | – | 200 | µs |



Figure 3: Reference Clock Timing Parameters

Table 22: GTX Transceiver User Clock Switching Characteristics⁽¹⁾

| Symbol | Description | Conditions | Speed Grade | | | | Units |
|--------------------|-----------------------------|---------------------------|----------------------|----------------------|--------|-----|-------|
| | | | -3 | -2 | -1 | -1L | |
| F _{TXOUT} | TXOUTCLK maximum frequency | Internal 20-bit data path | 330 | 330 | 250 | 250 | MHz |
| | | Internal 16-bit data path | 412.5 | 412.5 | 312.5 | 250 | MHz |
| F _{RXREC} | RXRECCLK maximum frequency | Internal 20-bit data path | 330 | 330 | 250 | 250 | MHz |
| | | Internal 16-bit data path | 412.5 | 412.5 | 312.5 | 250 | MHz |
| T _{RX} | RXUSRCLK maximum frequency | | 412.5 ⁽²⁾ | 412.5 ⁽²⁾ | 312.5 | 250 | MHz |
| T _{RX2} | RXUSRCLK2 maximum frequency | 1 byte interface | 376 | 376 | 312.5 | 250 | MHz |
| | | 2 byte interface | 406.25 | 406.25 | 312.5 | 250 | MHz |
| | | 4 byte interface | 206.25 | 206.25 | 156.25 | 125 | MHz |
| T _{TX} | TXUSRCLK maximum frequency | | 412.5 ⁽³⁾ | 412.5 ⁽³⁾ | 312.5 | 250 | MHz |
| T _{TX2} | TXUSRCLK2 maximum frequency | 1 byte interface | 376 | 376 | 312.5 | 250 | MHz |
| | | 2 byte interface | 406.25 | 406.25 | 312.5 | 250 | MHz |
| | | 4 byte interface | 206.25 | 206.25 | 156.25 | 125 | MHz |

Notes:

1. Clocking must be implemented as described in [UG366: Virtex-6 FPGA GTX Transceivers User Guide](#).
2. 406.25 MHz when the RX elastic buffer is bypassed.
3. 406.25 MHz when the TX buffer is bypassed.

Table 23: GTX Transceiver Transmitter Switching Characteristics

| Symbol | Description | Condition | Min | Typ | Max | Units |
|------------------------------|--|---------------------------|-------|-----|---------------------|-------|
| F _{GTXTX} | Serial data rate range | | 0.480 | – | F _{GTXMAX} | Gb/s |
| T _{RTX} | TX Rise time | 20%–80% | – | 120 | – | ps |
| T _{FTX} | TX Fall time | 80%–20% | – | 120 | – | ps |
| T _{LLSKEW} | TX lane-to-lane skew ⁽¹⁾ | | – | – | 350 | ps |
| V _{TXOOBVDPP} | Electrical idle amplitude | | – | – | 15 | mV |
| T _{TXOOBTRANSITION} | Electrical idle transition time | | – | – | 75 | ns |
| T _{J6.5} | Total Jitter ⁽²⁾⁽³⁾ | 6.5 Gb/s | – | – | 0.33 | UI |
| D _{J6.5} | Deterministic Jitter ⁽²⁾⁽³⁾ | | – | – | 0.17 | UI |
| T _{J5.0} | Total Jitter ⁽²⁾⁽³⁾ | 5.0 Gb/s | – | – | 0.33 | UI |
| D _{J5.0} | Deterministic Jitter ⁽²⁾⁽³⁾ | | – | – | 0.15 | UI |
| T _{J4.25} | Total Jitter ⁽²⁾⁽³⁾ | 4.25 Gb/s | – | – | 0.33 | UI |
| D _{J4.25} | Deterministic Jitter ⁽²⁾⁽³⁾ | | – | – | 0.14 | UI |
| T _{J3.75} | Total Jitter ⁽²⁾⁽³⁾ | 3.75 Gb/s | – | – | 0.34 | UI |
| D _{J3.75} | Deterministic Jitter ⁽²⁾⁽³⁾ | | – | – | 0.16 | UI |
| T _{J3.125} | Total Jitter ⁽²⁾⁽³⁾ | 3.125 Gb/s | – | – | 0.2 | UI |
| D _{J3.125} | Deterministic Jitter ⁽²⁾⁽³⁾ | | – | – | 0.1 | UI |
| T _{J3.125L} | Total Jitter ⁽²⁾⁽³⁾ | 3.125 Gb/s ⁽⁴⁾ | – | – | 0.35 | UI |
| D _{J3.125L} | Deterministic Jitter ⁽²⁾⁽³⁾ | | – | – | 0.16 | UI |
| T _{J2.5} | Total Jitter ⁽²⁾⁽³⁾ | 2.5 Gb/s ⁽⁵⁾ | – | – | 0.20 | UI |
| D _{J2.5} | Deterministic Jitter ⁽²⁾⁽³⁾ | | – | – | 0.08 | UI |
| T _{J1.25} | Total Jitter ⁽²⁾⁽³⁾ | 1.25 Gb/s ⁽⁶⁾ | – | – | 0.15 | UI |
| D _{J1.25} | Deterministic Jitter ⁽²⁾⁽³⁾ | | – | – | 0.06 | UI |
| T _{J600} | Total Jitter ⁽²⁾⁽³⁾ | 600 Mb/s | – | – | 0.1 | UI |
| D _{J600} | Deterministic Jitter ⁽²⁾⁽³⁾ | | – | – | 0.03 | UI |
| T _{J480} | Total Jitter ⁽²⁾⁽³⁾ | 480 Mb/s | – | – | 0.1 | UI |
| D _{J480} | Deterministic Jitter ⁽²⁾⁽³⁾ | | – | – | 0.03 | UI |

Notes:

- Using same REFCLK input with TXENPMPHASEALIGN enabled for up to 12 consecutive transmitters (three fully populated GTX Quads).
- Using PLL_DIVSEL_FB = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
- All jitter values are based on a bit-error ratio of 1e⁻¹².
- PLL frequency at 1.5625 GHz and OUTDIV = 1.
- PLL frequency at 2.5 GHz and OUTDIV = 2.
- PLL frequency at 2.5 GHz and OUTDIV = 4.

Table 24: GTX Transceiver Receiver Switching Characteristics

| Symbol | Description | | Min | Typ | Max | Units |
|--|---|--|-------|-----|---------------------|-------|
| F _{GTXRX} | Serial data rate | RX oversampler not enabled | 0.600 | – | F _{GTXMAX} | Gb/s |
| | | RX oversampler enabled | 0.480 | – | 0.600 | Gb/s |
| T _{RXELECIDLE} | Time for RXELECIDLE to respond to loss or restoration of data | | – | 75 | – | ns |
| RX _{OOBVDPP} | OOB detect threshold peak-to-peak | | 60 | – | 150 | mV |
| RX _{SST} | Receiver spread-spectrum tracking ⁽¹⁾ | Modulated @ 33 KHz | –5000 | – | 0 | ppm |
| RX _{RL} | Run length (CID) | Internal AC capacitor bypassed | – | – | 512 | UI |
| RX _{PPMTOL} | Data/REFCLK PPM offset tolerance | CDR 2 nd -order loop disabled | –200 | – | 200 | ppm |
| | | CDR 2 nd -order loop enabled | –2000 | – | 2000 | ppm |
| SJ Jitter Tolerance⁽²⁾ | | | | | | |
| JT_SJ _{6.5} | Sinusoidal Jitter ⁽³⁾ | 6.5 Gb/s | 0.44 | – | – | UI |
| JT_SJ _{5.0} | Sinusoidal Jitter ⁽³⁾ | 5.0 Gb/s | 0.44 | – | – | UI |
| JT_SJ _{4.25} | Sinusoidal Jitter ⁽³⁾ | 4.25 Gb/s | 0.44 | – | – | UI |
| JT_SJ _{3.75} | Sinusoidal Jitter ⁽³⁾ | 3.75 Gb/s | 0.44 | – | – | UI |
| JT_SJ _{3.125} | Sinusoidal Jitter ⁽³⁾ | 3.125 Gb/s | 0.45 | – | – | UI |
| JT_SJ _{3.125L} | Sinusoidal Jitter ⁽³⁾ | 3.125 Gb/s ⁽⁴⁾ | 0.45 | – | – | UI |
| JT_SJ _{2.5} | Sinusoidal Jitter ⁽³⁾ | 2.5 Gb/s ⁽⁵⁾ | 0.5 | – | – | UI |
| JT_SJ _{1.25} | Sinusoidal Jitter ⁽³⁾ | 1.25 Gb/s ⁽⁶⁾ | 0.5 | – | – | UI |
| JT_SJ ₆₀₀ | Sinusoidal Jitter ⁽³⁾ | 600 Mb/s | 0.4 | – | – | UI |
| JT_SJ ₄₈₀ | Sinusoidal Jitter ⁽³⁾ | 480 Mb/s | 0.4 | – | – | UI |
| SJ Jitter Tolerance with Stressed Eye⁽²⁾ | | | | | | |
| JT_TJSE _{3.125} | Total Jitter with Stressed Eye ⁽⁷⁾ | 3.125 Gb/s | 0.70 | – | – | UI |
| | | 5.0 Gb/s | 0.70 | – | – | UI |
| JT_SJSE _{3.125} | Sinusoidal Jitter with Stressed Eye ⁽⁷⁾ | 3.125 Gb/s | 0.1 | – | – | UI |
| | | 5.0 Gb/s | 0.1 | – | – | UI |

Notes:

- Using PLL_RXDIVSEL_OUT = 1, 2, and 4.
- All jitter values are based on a bit error ratio of 1e⁻¹².
- The frequency of the injected sinusoidal jitter is 80 MHz.
- PLL frequency at 1.5625 GHz and OUTDIV = 1.
- PLL frequency at 2.5 GHz and OUTDIV = 2.
- PLL frequency at 2.5 GHz and OUTDIV = 4.
- Composite jitter with RX equalizer enabled. DFE disabled.

GTH Transceiver Specifications

GTH Transceiver DC Characteristics

Table 25: Absolute Maximum Ratings for GTH Transceivers⁽¹⁾

| Symbol | Description | Min | Max | Units |
|------------------------|---|------|-------|-------|
| MGTHAVCC | Analog supply voltage for the GTH transmitter, receiver, and common analog circuits | -0.5 | 1.125 | V |
| MGTHAVCCR _X | Analog supply voltage for the GTH receiver circuits and common analog circuits | -0.5 | 1.125 | V |
| MGTHAVTT | Analog supply voltage for the GTH transmitter termination circuits | -0.5 | 1.32 | V |
| MGTHAVCCPLL | Analog supply voltage for the GTH receiver and PLL circuits | -0.5 | 1.935 | V |
| V _{IN} | Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage | -0.5 | 1.125 | V |
| V _{MGTREFCLK} | Reference clock absolute input voltage | -0.5 | 1.935 | V |

Notes:

- Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.

Table 26: Recommended Operating Conditions for GTH Transceivers⁽¹⁾⁽²⁾

| Symbol | Description | Min | Typ | Max | Units |
|------------------------|---|-------|-----|-------|-------|
| MGTHAVCC | Analog supply voltage for the GTH transmitter, receiver, and common analog circuits | 1.075 | 1.1 | 1.125 | V |
| MGTHAVCCR _X | Analog supply voltage for the GTH receiver circuits and common analog circuits | 1.075 | 1.1 | 1.125 | V |
| MGTHAVTT | Analog supply voltage for the GTH transmitter termination circuits | 1.140 | 1.2 | 1.26 | V |
| MGTHAVCCPLL | Analog supply voltage for the GTH receiver and PLL circuit | 1.710 | 1.8 | 1.89 | V |

Notes:

- Each voltage listed requires the filter circuit described in [UG371: Virtex-6 FPGA GTH Transceivers User Guide](#).
- Voltages are specified for the temperature range of T_j = -40°C to +100°C.

Table 27: GTH Transceiver Power Supply Sequencing⁽¹⁾⁽²⁾⁽³⁾

| Symbol | Description | Min | Max | Units |
|--|--|-----|-----|-------|
| T _{HAVCC2HAVCCR_X} | Maximum time between powering MGTHAVCC to when MGTHAVCCR _X must be powered. | 0 | 5 | ms |
| T _{HAVCCR_X2HAVCCPLL} | Minimum time between powering MGTHAVCCR _X to when MGTHAVCCPLL can be powered. | 10 | - | μs |
| T _{HAVCCR_X2HAVTT} | Minimum time between powering MGTHAVCCR _X to when MGTHAVTT can be powered. | 10 | - | μs |

Notes:

- MGTHAVCCR_X must be powered simultaneously or within T_{HAVCC2HAVCCR_X} of MGTHAVCC, but it must not precede MGTHAVCC.
- MGTHAVCC and MGTHAVCCR_X must be powered before MGTHAVCCPLL and MGTHAVTT. This minimum time is defined by T_{HAVCCR_X2HAVCCPLL} and T_{HAVCCR_X2HAVTT}.
- At any time, the condition of MGTHAVCC being present and MGTHAVCCR_X not being present should not occur for more than the maximum T_{HAVCC2HAVCCR_X}.

Figure 4 shows the timing parameters in Table 27.



DS152_04_051110

Figure 4: GTH Transceiver Power Supply Power-On Sequencing

Table 28: GTH Transceiver Supply Current

| Symbol | Description | Typ ⁽¹⁾ | Max | Units |
|--------------------------|---|-----------------------|--------|-------|
| I _{MGTHAVCC} | MGTHAVCC supply current for one GTH Quad (4 lanes) | 571 | Note 2 | mA |
| I _{MGTHAVCCR} | MGTHAVCCR supply current for a GTH Quad (4 lanes) | 254 | Note 2 | mA |
| I _{MGTHAVTT} | MGTHAVTT supply current for one GTH Quad (4 lanes) | 93 | Note 2 | mA |
| I _{MGTHAVCCPLL} | MGTHAVCCPLL supply current for one GTH Quad (4 lanes) | 219 | Note 2 | mA |
| MGTR _{REF} | Precision reference resistor for internal calibration termination | 1000.0 ± 1% tolerance | | Ω |

Notes:

1. Typical values are specified at nominal voltage, 25°C, with a 10.3125 Gb/s line rate.
2. Values for currents other than the values specified in this table can be obtained by using the Xilinx Power Estimator (XPE) or XPower Analyzer (XPA) tools.

Table 29: GTH Transceiver Quiescent Supply Current⁽¹⁾⁽²⁾

| Symbol | Description | Typ ⁽³⁾ | Max | Units |
|---------------------------|---|--------------------|--------|-------|
| I _{MGTHAVCCQ} | Quiescent MGTHAVCC Supply Current for one GTH Quad (4 lanes) | 65 | Note 4 | mA |
| I _{MGTHAVCCRQ} | Quiescent MGTHAVCCR Supply Current for one GTH Quad (4 lanes) | 17 | Note 4 | mA |
| I _{MGTHAVTTQ} | Quiescent MGTHAVTT Supply Current for one GTH Quad (4 lanes) | 1 | Note 4 | mA |
| I _{MGTHAVCCPLLQ} | Quiescent MGTHAVCCPLL Supply Current for one GTH Quad (4 lanes) | 1 | Note 4 | mA |

Notes:

1. Device powered and unconfigured.
2. GTH transceiver quiescent supply current for an entire device can be calculated by multiplying the values in this table by the number of available GTH transceivers.
3. Typical values are specified at nominal voltage, 25°C.
4. Currents for conditions other than values specified in this table can be obtained by using the XPE or XPA tools.

GTH Transceiver DC Input and Output Levels

Table 30 summarizes the DC output specifications of the GTH transceivers in Virtex-6 FPGAs. Consult [UG371: Virtex-6 FPGA GTH Transceivers User Guide](#) for further details.

Table 30: GTH Transceiver DC Specifications

| Symbol | DC Parameter | Conditions | Min | Typ | Max | Units |
|--------------|---|--|-----|-----|------|----------|
| D_{VPPIN} | Differential peak-to-peak input voltage | External AC coupled | 175 | – | 1200 | mV |
| D_{VPPOUT} | Differential peak-to-peak output voltage ⁽¹⁾ | Transmitter output swing is set to maximum setting | 800 | – | 1200 | mV |
| R_{IN} | Differential input resistance | | 80 | 100 | 120 | Ω |
| R_{OUT} | Differential output resistance | | 80 | 100 | 120 | Ω |
| T_{OSKEW} | Transmitter output pair (TXP and TXN) intra-pair skew | | – | 2 | – | ps |
| C_{EXT} | Recommended external AC coupling capacitor ⁽²⁾ | | – | 100 | – | nF |

Notes:

1. The output swing and preemphasis levels are programmable using the attributes discussed in [UG371: Virtex-6 FPGA GTH Transceivers User Guide](#) and can result in values lower than reported in this table.
2. Other values can be used as appropriate to conform to specific protocols and standards.

Table 31 summarizes the DC specifications of the clock input of the GTH transceiver. Consult [UG371: Virtex-6 FPGA GTH Transceivers User Guide](#) for further details.

Table 31: GTH Transceiver Clock DC Input Level Specification

| Symbol | DC Parameter | Conditions | Min | Typ | Max | Units |
|-------------|---|----------------|-----|-----|------|----------|
| V_{IDIFF} | Differential peak-to-peak input voltage | ≤ 600 MHz | 500 | – | 1600 | mV |
| | | > 600 MHz | 600 | – | 1600 | mV |
| R_{IN} | Differential input resistance | | 80 | 100 | 120 | Ω |
| C_{EXT} | Required external AC coupling capacitor | | – | 100 | – | nF |

GTH Transceiver Switching Characteristics

Consult [UG371: Virtex-6 FPGA GTH Transceivers User Guide](#) for further information.

Table 32: GTH Transceiver Maximum Data Rate and PLL Frequency Range

| Symbol | Description | Conditions | Speed Grade | | | Units |
|----------------------|--|------------------------|-------------|--------|-------|-------|
| | | | -3 | -2 | -1 | |
| F _{GTHMAX} | Maximum GTH transceiver data rate | PLL Output Divider = 1 | 11.182 | 11.182 | 10.32 | Gb/s |
| | | PLL Output Divider = 4 | 2.795 | 2.795 | 2.58 | Gb/s |
| F _{GTHMIN} | Minimum GTH transceiver data rate ⁽¹⁾ | PLL Output Divider = 1 | 9.92 | 9.92 | 9.92 | Gb/s |
| | | PLL Output Divider = 4 | 2.48 | 2.48 | 2.48 | Gb/s |
| F _{GPLLMAX} | Maximum GTH PLL frequency | | 5.591 | 5.591 | 5.16 | GHz |
| F _{GPLLMIN} | Minimum GTH PLL frequency | | 4.96 | 4.96 | 4.96 | GHz |

Notes:

- Lower data rates can be achieved using FPGA logic based oversampling designs.

Table 33: GTH Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics

| Symbol | Description | Speed Grade | | | Units |
|------------------------|-----------------------------|-------------|----|----|-------|
| | | -3 | -2 | -1 | |
| F _{GTHDRPCLK} | GTHDRPCLK maximum frequency | 70 | 70 | 60 | MHz |

Table 34: GTH Transceiver Reference Clock Switching Characteristics

| Symbol | Description | Conditions | All Speed Grades | | | Units |
|--------------------|---|--|------------------|-----|-----|-------|
| | | | Min | Typ | Max | |
| F _{GCLK} | Reference clock frequency range | -1 speed grade | 150 | – | 645 | MHz |
| | | -2 and -3 speed grades | 150 | – | 700 | MHz |
| T _{RCLK} | Reference clock rise time | 20% – 80% | – | 200 | – | ps |
| T _{FCLK} | Reference clock fall time | 80% – 20% | – | 200 | – | ps |
| T _{DCREF} | Reference clock duty cycle | CLK | 45 | 50 | 55 | % |
| T _{LOCK} | Clock recovery frequency acquisition time | Initial PLL lock | – | – | 2 | ms |
| T _{PHASE} | Clock recovery phase acquisition time | Lock to data after PLL has locked to the reference clock | – | – | 20 | µs |

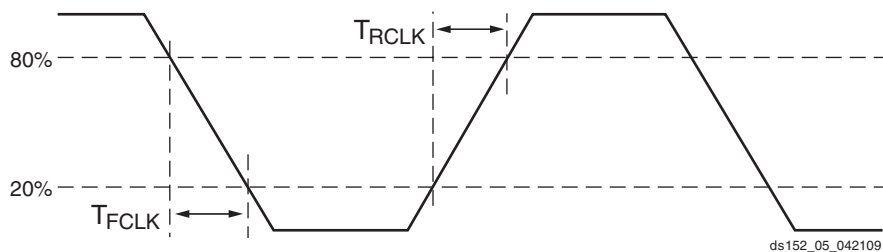


Figure 5: Reference Clock Timing Parameters

Table 35: GTH Transceiver User Clock Switching Characteristics (1)

| Symbol | Description | Conditions | Speed Grade | | | Units |
|--------------------|--------------------------------|-----------------------|-------------|-----|-----|-------|
| | | | -3 | -2 | -1 | |
| F _{TXOUT} | TXUSERCLKOUT maximum frequency | | 350 | 350 | 323 | MHz |
| F _{RXOUT} | RXUSERCLKOUT maximum frequency | | 350 | 350 | 323 | MHz |
| F _{TXIN} | TXUSERCLKIN maximum frequency | 16-bit data path | 350 | 350 | 323 | MHz |
| | | 20-bit data path | 280 | 280 | 258 | MHz |
| | | 32-bit data path | 350 | 350 | 323 | MHz |
| | | 40-bit data path | 280 | 280 | 258 | MHz |
| | | 64-bit data path | 175 | 175 | 162 | MHz |
| | | 80-bit data path | 140 | 140 | 129 | MHz |
| | | 64B/66B-bit data path | 170 | 170 | 157 | MHz |
| F _{RXIN} | RXUSERCLKIN maximum frequency | 16-bit data path | 350 | 350 | 323 | MHz |
| | | 20-bit data path | 280 | 280 | 258 | MHz |
| | | 32-bit data path | 350 | 350 | 323 | MHz |
| | | 40-bit data path | 280 | 280 | 258 | MHz |
| | | 64-bit data path | 175 | 175 | 162 | MHz |
| | | 80-bit data path | 140 | 140 | 129 | MHz |
| | | 64B/66B-bit data path | 170 | 170 | 157 | MHz |

Notes:

1. Clocking must be implemented as described in [UG371](#): *Virtex-6 FPGA GTH Transceivers User Guide*.

Table 36: GTH Transceiver Transmitter Switching Characteristics

| Symbol | Description | Condition | Min | Typ | Max | Units |
|---|----------------------|---------------------|-----|-------------------|-------|-------|
| T _{RTX} | TX Rise time | 20%–80% | – | 50 ⁽³⁾ | – | ps |
| T _{FTX} | TX Fall time | 80%–20% | – | 50 ⁽³⁾ | – | ps |
| T _{LLSKEW} | TX lane-to-lane skew | within one GTH Quad | – | – | 300 | ps |
| Transmitter Output Jitter⁽¹⁾⁽²⁾ | | | | | | |
| TJ _{11.18} | Total Jitter | 11.181 Gb/s | – | – | 0.280 | UI |
| DJ _{11.18} | Deterministic Jitter | | – | – | 0.170 | UI |
| TJ _{10.3125} | Total Jitter | 10.3125 Gb/s | – | – | 0.280 | UI |
| DJ _{10.3125} | Deterministic Jitter | | – | – | 0.170 | UI |
| TJ _{9.953} | Total Jitter | 9.953 Gb/s | – | – | 0.280 | UI |
| DJ _{9.953} | Deterministic Jitter | | – | – | 0.170 | UI |
| TJ _{2.667} | Total Jitter | 2.667 Gb/s | – | – | 0.110 | UI |
| DJ _{2.667} | Deterministic Jitter | | – | – | 0.060 | UI |
| TJ _{2.488} | Total Jitter | 2.488 Gb/s | – | – | 0.110 | UI |
| DJ _{2.488} | Deterministic Jitter | | – | – | 0.060 | UI |

Notes:

1. These values are NOT intended for protocol specific compliance determinations.
2. All jitter values are based on a bit-error ratio of 1e⁻¹².
3. Rise and fall times are specified at the transmitter package balls.

Table 37: GTH Transceiver Receiver Switching Characteristics

| Symbol | Description | | Min | Typ | Max | Units |
|---|----------------------------------|------------|------|-----|-----|-------|
| R _{XRL} | Run length (CID) | | 8000 | – | – | UI |
| R _{XPPMTOL} | Data/REFCLK PPM offset tolerance | | –200 | – | 200 | ppm |
| SJ Jitter Tolerance⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾ | | | | | | |
| JT_SJ _{11.18} | Sinusoidal Jitter | 11.18 Gb/s | 0.3 | – | – | UI |
| JT_SJ _{10.32} | Sinusoidal Jitter | 10.32 Gb/s | 0.3 | – | – | UI |
| JT_SJ _{9.95} | Sinusoidal Jitter | 9.95 Gb/s | 0.3 | – | – | UI |
| JT_SJ _{2.667} | Sinusoidal Jitter | 2.667 Gb/s | 0.5 | – | – | UI |
| JT_SJ _{2.48} | Sinusoidal Jitter | 2.48 Gb/s | 0.5 | – | – | UI |

Notes:

1. These values are NOT intended for protocol specific compliance determinations.
2. All jitter values are based on a bit error ratio of $1e^{-12}$.
3. The frequency of the injected sinusoidal jitter is 80 MHz.
4. High-frequency jitter tolerance including 6 db of channel loss at a high frequency of the data rate divided by two.

Ethernet MAC Switching Characteristics

 Consult [UG368: Virtex-6 FPGA Embedded Tri-mode Ethernet MAC User Guide](#) for further information.

Table 38: Maximum Ethernet MAC Performance

| Symbol | Description | Conditions | Speed Grade | | | | Units |
|--------------------------|--------------------------------------|--------------------------|--------------------|--------------------|--------------------|--------------------|-------|
| | | | -3 | -2 | -1 | -1L | |
| F _{TEMACCLIENT} | Client interface maximum frequency | 10 Mb/s – 8-bit width | 2.5 ⁽¹⁾ | 2.5 ⁽¹⁾ | 2.5 ⁽¹⁾ | 2.5 ⁽¹⁾ | MHz |
| | | 100 Mb/s – 8-bit width | 25 ⁽²⁾ | 25 ⁽²⁾ | 25 ⁽²⁾ | 25 ⁽²⁾ | MHz |
| | | 1000 Mb/s – 8-bit width | 125 | 125 | 125 | 125 | MHz |
| | | 1000 Mb/s – 16-bit width | 62.5 | 62.5 | 62.5 | 62.5 | MHz |
| | | 2000 Mb/s – 16-bit width | 125 | 125 | 125 | N/A | MHz |
| | | 2500 Mb/s – 16-bit width | 156.25 | 156.25 | 156.25 | N/A | MHz |
| F _{TEMACPHY} | Physical interface maximum frequency | 10 Mb/s – 4-bit width | 2.5 | 2.5 | 2.5 | 2.5 | MHz |
| | | 100 Mb/s – 4-bit width | 25 | 25 | 25 | 25 | MHz |
| | | 1000 Mb/s – 8-bit width | 125 | 125 | 125 | 125 | MHz |
| | | 2000 Mb/s – 8-bit width | 250 | 250 | 250 | N/A | MHz |
| | | 2500 Mb/s – 8-bit width | 312.5 | 312.5 | 312.5 | N/A | MHz |

Notes:

1. When not using clock enable, the F_{MAX} is lowered to 1.25 MHz.
2. When not using clock enable, the F_{MAX} is lowered to 12.5 MHz.

Integrated Interface Block for PCI Express Designs Switching Characteristics

More information and documentation on solutions for PCI Express designs can be found at:
<http://www.xilinx.com/technology/protocols/pciexpress.htm>

Table 39: Maximum Performance for PCI Express Designs

| Symbol | Description | Speed Grade | | | | Units |
|----------------------|------------------------------|-------------|-----|-----|-----|-------|
| | | -3 | -2 | -1 | -1L | |
| F _{PIPECLK} | Pipe clock maximum frequency | 250 | 250 | 250 | 250 | MHz |
| F _{USERCLK} | User clock maximum frequency | 500 | 500 | 250 | 250 | MHz |
| F _{DRPCLK} | DRP clock maximum frequency | 250 | 250 | 250 | 250 | MHz |

System Monitor Analog-to-Digital Converter Specification

Table 40: Analog-to-Digital Specifications

| Parameter | Symbol | Comments/Conditions | Min | Typ | Max | Units |
|---|--------------------|--|-----|-------|------|--------|
| AV _{DD} = 2.5V ± 5%, V _{REFP} = 1.25V, V _{REFN} = 0V, ADCCLK = 5.2 MHz, T _j = -55°C to 125°C M-Grade, Typical values at T _j =+35°C | | | | | | |
| DC Accuracy: All external input channels. Both unipolar and bipolar modes. | | | | | | |
| Resolution | | | 10 | – | – | Bits |
| Integral Nonlinearity | INL | | – | – | ±1 | LSBs |
| Differential Nonlinearity | DNL | No missing codes (T _{MIN} to T _{MAX}) Guaranteed Monotonic | – | – | ±0.9 | LSBs |
| Unipolar Offset Error ⁽¹⁾ | | Uncalibrated | – | ±2 | ±30 | LSBs |
| Bipolar Offset Error ⁽¹⁾ | | Uncalibrated measured in bipolar mode | – | ±2 | ±30 | LSBs |
| Gain Error | | Uncalibrated - External Reference | – | ±0.2 | ±2 | % |
| | | Uncalibrated - Internal Reference | – | ±2 | – | % |
| Bipolar Gain Error ⁽¹⁾ | | Uncalibrated - External Reference | – | ±0.2 | ±2 | % |
| | | Uncalibrated - Internal Reference | – | ±2 | – | % |
| Total Unadjusted Error (Uncalibrated) | TUE | Deviation from ideal transfer function. External 1.25V reference | – | ±10 | – | LSBs |
| | | Deviation from ideal transfer function. Internal reference | – | ±20 | – | LSBs |
| Total Unadjusted Error (Calibrated) | TUE | Deviation from ideal transfer function. External 1.25V reference | – | ±1 | ±2 | LSBs |
| Calibrated Gain Temperature Coefficient | | Variation of FS code with temperature | – | ±0.01 | – | LSB/°C |
| DC Common-Mode Reject | CMRR _{DC} | V _N = V _{CM} = 0.5V ± 0.5V, V _P – V _N = 100mV | – | 70 | – | dB |
| Conversion Rate⁽²⁾ | | | | | | |
| Conversion Time - Continuous | t _{CONV} | Number of CLK cycles | 26 | – | 32 | |
| Conversion Time - Event | t _{CONV} | Number of CLK cycles | – | – | 21 | |
| T/H Acquisition Time | t _{ACQ} | Number of CLK cycles | 4 | – | – | |
| DRP Clock Frequency | DCLK | DRP clock frequency | 8 | – | 80 | MHz |
| ADC Clock Frequency | ADCCLK | Derived from DCLK | 1 | – | 5.2 | MHz |
| CLK Duty cycle | | | 40 | – | 60 | % |

Table 40: Analog-to-Digital Specifications (Cont'd)

| Parameter | Symbol | Comments/Conditions | Min | Typ | Max | Units |
|--|------------|--|-------|-----------|-----------|--------------------|
| Analog Inputs⁽³⁾ | | | | | | |
| Dedicated Analog Inputs Input Voltage Range $V_P - V_N$ | | Unipolar Operation | 0 | – | 1 | Volts |
| | | Bipolar Operation | –0.5 | – | +0.5 | |
| | | Unipolar Common Mode Range (FS input) | 0 | – | +0.5 | |
| | | Bipolar Common Mode Range (FS input) | +0.5 | – | +0.6 | |
| | | Bandwidth | – | 20 | – | MHz |
| Auxiliary Analog Inputs Input Voltage Range $V_{AUXP[0]} / V_{AUXN[0]}$ to $V_{AUXP[15]} / V_{AUXN[15]}$ $T_j = -55^{\circ}\text{C}$ to 125°C | | Unipolar Operation | 0 | – | 1 | Volts |
| | | Bipolar Operation | –0.5 | – | +0.5 | |
| | | Unipolar Common Mode Range (FS input) | 0 | – | +0.5 | |
| | | Bipolar Common Mode Range (FS input) | +0.5 | – | +0.6 | |
| | | Bandwidth | – | 10 | – | kHz |
| Input Leakage Current | | A/D not converting, ADCCLK stopped | – | ± 1.0 | – | μA |
| Input Capacitance | | | – | 10 | – | pF |
| On-chip Supply Monitor Error | | V_{CCINT} and V_{CCAUX} with calibration enabled. External 1.25V reference $T_j = -55^{\circ}\text{C}$ to 125°C . | – | – | ± 1.0 | % Reading |
| | | V_{CCINT} and V_{CCAUX} with calibration enabled. Internal reference $T_j = -40^{\circ}\text{C}$ to 100°C . ⁽⁴⁾ | – | ± 2 | – | % Reading |
| On-chip Temperature Monitor Error | | $T_j = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ with calibration enabled. External 1.25V reference. | – | – | ± 4 | $^{\circ}\text{C}$ |
| | | $T_j = -40^{\circ}\text{C}$ to $+100^{\circ}\text{C}$ with calibration enabled. Internal reference. ⁽⁴⁾ | – | ± 5 | – | $^{\circ}\text{C}$ |
| External Reference Inputs⁽⁵⁾ | | | | | | |
| Positive Reference Input Voltage Range | V_{REFP} | Measured Relative to V_{REFN} | 1.20 | 1.25 | 1.30 | Volts |
| Negative Reference Input Voltage Range | V_{REFN} | Measured Relative to AGND | –50 | 0 | 100 | mV |
| Input current | I_{REF} | ADCCLK = 5.2 MHz | – | – | 100 | μA |
| Power Requirements | | | | | | |
| Analog Power Supply | AV_{DD} | Measured Relative to AV_{SS} | 2.375 | 2.5 | 2.625 | Volts |
| Analog Supply Current | AI_{DD} | ADCCLK = 5.2 MHz | – | – | 12 | mA |

Notes:

- Offset errors are removed by enabling the System Monitor automatic gain calibration feature.
- See "System Monitor Timing" in [UG370: Virtex-6 FPGA System Monitor User Guide](#)
- See "Analog Inputs" in [UG370: Virtex-6 FPGA System Monitor User Guide](#) for a detailed description.
- These internal references are not specified over the junction temperature operating range for military (M) temperature devices.
- Any variation in the reference voltage from the nominal $V_{REFP} = 1.25\text{V}$ and $V_{REFN} = 0\text{V}$ will result in a deviation from the ideal transfer function. This also impacts the accuracy of the internal sensor measurements (i.e., temperature and power supply). However, for external ratiometric type applications allowing reference to vary by $\pm 4\%$ is permitted.

Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Virtex-6 devices. The numbers reported here are worst-case values; they have all been fully characterized. These values are subject to the same guidelines as the [Switching Characteristics, page 26](#).

Table 41: Interface Performances

| Description | Speed Grade | | | |
|--|-------------|-----------|-----------|----------|
| | -3 | -2 | -1 | -1L |
| Networking Applications | | | | |
| SDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 8) | 710 Mb/s | 710 Mb/s | 650 Mb/s | 585 Mb/s |
| DDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 10) | 1.4 Gb/s | 1.3 Gb/s | 1.25 Gb/s | 1.1 Gb/s |
| SDR LVDS receiver (SFI-4.1) ⁽¹⁾ | 710 Mb/s | 710 Mb/s | 650 Mb/s | 585 Mb/s |
| DDR LVDS receiver (SPI-4.2) ⁽¹⁾ | 1.4 Gb/s | 1.3 Gb/s | 1.1 Gb/s | 0.9 Gb/s |
| Maximum Physical Interface (PHY) Rate for Memory Interfaces⁽²⁾⁽³⁾⁽⁴⁾ | | | | |
| DDR2 | 800 Mb/s | 800 Mb/s | 800 Mb/s | 606 Mb/s |
| DDR3 | 1066 Mb/s | 1066 Mb/s | 800 Mb/s | 800 Mb/s |
| QDR II + SRAM | 400 MHz | 350 MHz | 300 MHz | – |
| RLDRAM II | 500 MHz | 400 MHz | 350 MHz | – |

Notes:

1. LVDS receivers are typically bounded with certain applications where specific DPA algorithms dominate deterministic performance.
2. Verified on Xilinx memory characterization platforms designed according to the guidelines in UG: *Virtex-6 FPGA Memory Interface Solutions User Guide*.
3. Consult [DS186](#); *Virtex-6 FPGA Memory Interface Solutions Data Sheet* for performance and feature information on memory interface cores (controller plus PHY).
4. Memory Interface data rates have not been tested over the junction temperature operating range for military (M) temperature devices. Customers are responsible for specifying and testing their specific M temperature grade memory implementation.

Switching Characteristics

All values represented in this data sheet are based on these speed specifications: v1.17 for -3, -2, and -1; and v1.10 for -1L. Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

All specifications are always representative of worst-case supply voltage and junction temperature conditions.

Testing of Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Virtex-6 devices.

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device.

[Table 42](#) correlates the current status of each Virtex-6 device on a per speed grade basis.

Table 42: Virtex-6 Device Speed Grade Designations

| Device | Speed Grade Designations | | |
|------------|--------------------------|-------------|-----------------|
| | Advance | Preliminary | Production |
| XC6VLX75T | | | -3, -2, -1, -1L |
| XC6VLX130T | | | -3, -2, -1, -1L |
| XC6VLX195T | | | -3, -2, -1, -1L |
| XC6VLX240T | | | -3, -2, -1, -1L |
| XC6VLX365T | | | -3, -2, -1, -1L |
| XC6VLX550T | | | -2, -1, -1L |
| XC6VLX760 | | | -2, -1, -1L |
| XC6VSX315T | | | -3, -2, -1, -1L |
| XC6VSX475T | | | -2, -1, -1L |
| XC6VHX250T | | | -3, -2, -1 |
| XC6VHX255T | | | -3, -2, -1 |
| XC6VHX380T | | | -3, -2, -1 |
| XC6VHX565T | | | -2, -1 |
| XQ6VLX130T | | | -2, -1, -1L |
| XQ6VLX240T | | | -2, -1, -1L |
| XQ6VLX550T | | | -1, -1L |
| XQ6VSX315T | | | -2, -1, -1L |
| XQ6VSX475T | | | -1, -1L |

Production Silicon and ISE Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label ([Advance](#), [Preliminary](#), [Production](#)). Any labeling discrepancies are corrected in subsequent speed specification releases.

[Table 43](#) lists the production released Virtex-6 family member, speed grade, and the minimum corresponding supported speed specification version and ISE software revisions. The ISE® software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 43: Virtex-6 Device Production Software and Speed Specification Release

| Device | Speed Grade Designations | | | |
|-------------|---|---|---------------------------------|----------------------|
| | -3 | -2 | -1 | -1L |
| XC6VLX75T | ISE 12.2 v1.08 | | | ISE 12.3 v1.07 Patch |
| XC6VLX130T | ISE 12.1 v1.06 | ISE 11.5 v1.05 ⁽²⁾ | ISE 11.5 v1.05 ⁽²⁾ | ISE 12.2 v1.05 |
| XC6VLX195T | ISE 12.1 v1.06 | ISE 12.1 v1.06 | ISE 12.1 v1.06 | ISE 12.2 v1.04 |
| XC6VLX240T | ISE 12.1 v1.06 | ISE 11.4.1 v1.04 ⁽²⁾ | ISE 11.4.1 v1.04 ⁽²⁾ | ISE 12.2 v1.04 |
| XC6VLX365T | ISE 12.2 v1.08 | | | ISE 12.2 v1.04 |
| XC6VLX550T | N/A | ISE 12.2 v1.07 | | ISE 12.2 v1.04 |
| XC6VLX760 | N/A | ISE 12.2 v1.08 | | ISE 12.3 v1.07 Patch |
| XC6VVSX315T | ISE 12.2 v1.08 | ISE 12.1 v1.06 | | ISE 12.3 v1.07 Patch |
| XC6VVSX475T | N/A | ISE 12.2 v1.08 | | ISE 12.3 v1.07 Patch |
| XC6VHX250T | ISE 12.4 v1.10 | | | N/A |
| XC6VHX255T | ISE 13.1 v1.14 using the ISE 13.1 software update | | | N/A |
| XC6VHX380T | ISE 12.4 v1.10 | | | N/A |
| XC6VHX565T | N/A | ISE 13.1 v1.14 using the ISE 13.1 software update | | N/A |
| XQ6VLX130T | N/A | ISE 13.3 v1.17 Patch | | ISE 13.3 v1.10 |
| XQ6VLX240T | N/A | ISE 13.3 v1.17 Patch | | ISE 13.3 v1.10 |
| XQ6VLX550T | N/A | N/A | ISE 13.3 v1.17 Patch | ISE 13.3 v1.10 |
| XQ6VVSX315T | N/A | ISE 13.3 v1.17 Patch | | ISE 13.3 v1.10 |
| XQ6VVSX475T | N/A | N/A | ISE 13.3 v1.17 Patch | ISE 13.3 v1.10 |

Notes:

- Blank entries indicate a device and/or speed grade in advance or preliminary status.
- Designs utilizing the GTX transceivers must use the software version ISE 12.1 v1.06 or later.

IOB Pad Input/Output/3-State Switching Characteristics

Table 44 (for commercial (XC) Virtex-6 devices) and **Table 45** (for the Defense-grade (XQ) Virtex-6 devices) summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

T_{IOPI} is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.

T_{IOOP} is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.

T_{IOTP} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer.

Table 46 summarizes the value of T_{IOTPHZ} . T_{IOTPHZ} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state).

Table 44: IOB Switching Characteristics for the Commercial (XC) Virtex-6 Devices

| I/O Standard | T_{IOPI} | | | | T_{IOOP} | | | | T_{IOTP} | | | | Units |
|--------------------------|-------------|------|------|------|-------------|------|------|------|-------------|------|------|------|-------|
| | Speed Grade | | | | Speed Grade | | | | Speed Grade | | | | |
| | -3 | -2 | -1 | -1L | -3 | -2 | -1 | -1L | -3 | -2 | -1 | -1L | |
| LVDS_25 | 0.85 | 0.94 | 1.09 | 1.08 | 1.45 | 1.54 | 1.68 | 1.62 | 1.45 | 1.54 | 1.68 | 1.62 | ns |
| LVDSEXT_25 | 0.85 | 0.94 | 1.09 | 1.08 | 1.53 | 1.65 | 1.84 | 1.73 | 1.53 | 1.65 | 1.84 | 1.73 | ns |
| HT_25 | 0.85 | 0.94 | 1.09 | 1.08 | 1.51 | 1.62 | 1.78 | 1.69 | 1.51 | 1.62 | 1.78 | 1.69 | ns |
| BLVDS_25 | 0.85 | 0.94 | 1.09 | 1.08 | 1.39 | 1.50 | 1.67 | 1.65 | 1.39 | 1.50 | 1.67 | 1.65 | ns |
| RSDS_25 (point to point) | 0.85 | 0.94 | 1.09 | 1.08 | 1.45 | 1.54 | 1.68 | 1.62 | 1.45 | 1.54 | 1.68 | 1.62 | ns |
| HSTL_I | 0.81 | 0.91 | 1.06 | 1.06 | 1.45 | 1.56 | 1.73 | 1.71 | 1.45 | 1.56 | 1.73 | 1.71 | ns |
| HSTL_II | 0.81 | 0.91 | 1.06 | 1.06 | 1.44 | 1.56 | 1.74 | 1.72 | 1.44 | 1.56 | 1.74 | 1.72 | ns |
| HSTL_III | 0.81 | 0.91 | 1.06 | 1.06 | 1.42 | 1.54 | 1.71 | 1.69 | 1.42 | 1.54 | 1.71 | 1.69 | ns |
| HSTL_I_18 | 0.81 | 0.91 | 1.06 | 1.06 | 1.47 | 1.58 | 1.75 | 1.72 | 1.47 | 1.58 | 1.75 | 1.72 | ns |
| HSTL_II_18 | 0.81 | 0.91 | 1.06 | 1.06 | 1.50 | 1.62 | 1.81 | 1.78 | 1.50 | 1.62 | 1.81 | 1.78 | ns |
| HSTL_III_18 | 0.81 | 0.91 | 1.06 | 1.06 | 1.42 | 1.54 | 1.71 | 1.69 | 1.42 | 1.54 | 1.71 | 1.69 | ns |
| SSTL2_I | 0.81 | 0.91 | 1.06 | 1.06 | 1.49 | 1.60 | 1.77 | 1.74 | 1.49 | 1.60 | 1.77 | 1.74 | ns |
| SSTL2_II | 0.81 | 0.91 | 1.06 | 1.06 | 1.42 | 1.54 | 1.72 | 1.71 | 1.42 | 1.54 | 1.72 | 1.71 | ns |
| SSTL15 | 0.81 | 0.91 | 1.06 | 1.06 | 1.42 | 1.54 | 1.71 | 1.69 | 1.42 | 1.54 | 1.71 | 1.69 | ns |
| LVC MOS25, Slow, 2 mA | 0.51 | 0.57 | 0.66 | 0.70 | 5.09 | 5.46 | 6.01 | 5.63 | 5.09 | 5.46 | 6.01 | 5.63 | ns |
| LVC MOS25, Slow, 4 mA | 0.51 | 0.57 | 0.66 | 0.70 | 3.30 | 3.49 | 3.79 | 3.65 | 3.30 | 3.49 | 3.79 | 3.65 | ns |
| LVC MOS25, Slow, 6 mA | 0.51 | 0.57 | 0.66 | 0.70 | 2.62 | 2.81 | 3.08 | 2.95 | 2.62 | 2.81 | 3.08 | 2.95 | ns |
| LVC MOS25, Slow, 8 mA | 0.51 | 0.57 | 0.66 | 0.70 | 2.21 | 2.41 | 2.72 | 2.59 | 2.21 | 2.41 | 2.72 | 2.59 | ns |
| LVC MOS25, Slow, 12 mA | 0.51 | 0.57 | 0.66 | 0.70 | 1.80 | 1.95 | 2.17 | 2.10 | 1.80 | 1.95 | 2.17 | 2.10 | ns |
| LVC MOS25, Slow, 16 mA | 0.51 | 0.57 | 0.66 | 0.70 | 1.89 | 2.05 | 2.29 | 2.21 | 1.89 | 2.05 | 2.29 | 2.21 | ns |
| LVC MOS25, Slow, 24 mA | 0.51 | 0.57 | 0.66 | 0.70 | 1.68 | 1.82 | 2.02 | 1.98 | 1.68 | 1.82 | 2.02 | 1.98 | ns |
| LVC MOS25, Fast, 2 mA | 0.51 | 0.57 | 0.66 | 0.70 | 5.12 | 5.49 | 6.04 | 5.62 | 5.12 | 5.49 | 6.04 | 5.62 | ns |
| LVC MOS25, Fast, 4 mA | 0.51 | 0.57 | 0.66 | 0.70 | 3.28 | 3.50 | 3.82 | 3.65 | 3.28 | 3.50 | 3.82 | 3.65 | ns |
| LVC MOS25, Fast, 6 mA | 0.51 | 0.57 | 0.66 | 0.70 | 2.56 | 2.73 | 2.99 | 2.88 | 2.56 | 2.73 | 2.99 | 2.88 | ns |
| LVC MOS25, Fast, 8 mA | 0.51 | 0.57 | 0.66 | 0.70 | 2.11 | 2.33 | 2.65 | 2.53 | 2.11 | 2.33 | 2.65 | 2.53 | ns |
| LVC MOS25, Fast, 12 mA | 0.51 | 0.57 | 0.66 | 0.70 | 1.74 | 1.88 | 2.08 | 2.03 | 1.74 | 1.88 | 2.08 | 2.03 | ns |
| LVC MOS25, Fast, 16 mA | 0.51 | 0.57 | 0.66 | 0.70 | 1.77 | 1.92 | 2.13 | 2.08 | 1.77 | 1.92 | 2.13 | 2.08 | ns |

Table 44: IOB Switching Characteristics for the Commercial (XC) Virtex-6 Devices (Cont'd)

| I/O Standard | T _{IOPI} | | | | T _{IOOP} | | | | T _{IOTP} | | | | Units |
|------------------------|-------------------|------|------|------|-------------------|------|------|------|-------------------|------|------|------|-------|
| | Speed Grade | | | | Speed Grade | | | | Speed Grade | | | | |
| | -3 | -2 | -1 | -1L | -3 | -2 | -1 | -1L | -3 | -2 | -1 | -1L | |
| LVC MOS25, Fast, 24 mA | 0.51 | 0.57 | 0.66 | 0.70 | 1.66 | 1.79 | 1.99 | 1.96 | 1.66 | 1.79 | 1.99 | 1.96 | ns |
| LVC MOS18, Slow, 2 mA | 0.55 | 0.61 | 0.71 | 0.73 | 4.21 | 4.47 | 4.87 | 4.30 | 4.21 | 4.47 | 4.87 | 4.30 | ns |
| LVC MOS18, Slow, 4 mA | 0.55 | 0.61 | 0.71 | 0.73 | 2.79 | 2.96 | 3.21 | 2.94 | 2.79 | 2.96 | 3.21 | 2.94 | ns |
| LVC MOS18, Slow, 6 mA | 0.55 | 0.61 | 0.71 | 0.73 | 2.30 | 2.43 | 2.64 | 2.47 | 2.30 | 2.43 | 2.64 | 2.47 | ns |
| LVC MOS18, Slow, 8 mA | 0.55 | 0.61 | 0.71 | 0.73 | 2.01 | 2.11 | 2.27 | 2.24 | 2.01 | 2.11 | 2.27 | 2.24 | ns |
| LVC MOS18, Slow, 12 mA | 0.55 | 0.61 | 0.71 | 0.73 | 1.88 | 1.99 | 2.15 | 2.10 | 1.88 | 1.99 | 2.15 | 2.10 | ns |
| LVC MOS18, Slow, 16 mA | 0.55 | 0.61 | 0.71 | 0.73 | 1.84 | 1.95 | 2.11 | 2.04 | 1.84 | 1.95 | 2.11 | 2.04 | ns |
| LVC MOS18, Fast, 2 mA | 0.55 | 0.61 | 0.71 | 0.73 | 4.00 | 4.23 | 4.57 | 4.08 | 4.00 | 4.23 | 4.57 | 4.08 | ns |
| LVC MOS18, Fast, 4 mA | 0.55 | 0.61 | 0.71 | 0.73 | 2.62 | 2.76 | 2.97 | 2.74 | 2.62 | 2.76 | 2.97 | 2.74 | ns |
| LVC MOS18, Fast, 6 mA | 0.55 | 0.61 | 0.71 | 0.73 | 2.15 | 2.28 | 2.46 | 2.32 | 2.15 | 2.28 | 2.46 | 2.32 | ns |
| LVC MOS18, Fast, 8 mA | 0.55 | 0.61 | 0.71 | 0.73 | 1.90 | 1.99 | 2.13 | 2.14 | 1.90 | 1.99 | 2.13 | 2.14 | ns |
| LVC MOS18, Fast, 12 mA | 0.55 | 0.61 | 0.71 | 0.73 | 1.69 | 1.80 | 1.97 | 1.88 | 1.69 | 1.80 | 1.97 | 1.88 | ns |
| LVC MOS18, Fast, 16 mA | 0.55 | 0.61 | 0.71 | 0.73 | 1.63 | 1.74 | 1.91 | 1.88 | 1.63 | 1.74 | 1.91 | 1.88 | ns |
| LVC MOS15, Slow, 2 mA | 0.64 | 0.73 | 0.85 | 0.85 | 3.43 | 3.77 | 4.29 | 3.91 | 3.43 | 3.77 | 4.29 | 3.91 | ns |
| LVC MOS15, Slow, 4 mA | 0.64 | 0.73 | 0.85 | 0.85 | 2.58 | 2.79 | 3.10 | 2.93 | 2.58 | 2.79 | 3.10 | 2.93 | ns |
| LVC MOS15, Slow, 6 mA | 0.64 | 0.73 | 0.85 | 0.85 | 2.08 | 2.32 | 2.68 | 2.50 | 2.08 | 2.32 | 2.68 | 2.50 | ns |
| LVC MOS15, Slow, 8 mA | 0.64 | 0.73 | 0.85 | 0.85 | 1.81 | 1.98 | 2.23 | 2.24 | 1.81 | 1.98 | 2.23 | 2.24 | ns |
| LVC MOS15, Slow, 12 mA | 0.64 | 0.73 | 0.85 | 0.85 | 1.76 | 1.91 | 2.13 | 2.07 | 1.76 | 1.91 | 2.13 | 2.07 | ns |
| LVC MOS15, Slow, 16 mA | 0.64 | 0.73 | 0.85 | 0.85 | 1.69 | 1.83 | 2.04 | 1.98 | 1.69 | 1.83 | 2.04 | 1.98 | ns |
| LVC MOS15, Fast, 2 mA | 0.64 | 0.73 | 0.85 | 0.85 | 3.44 | 3.77 | 4.28 | 3.91 | 3.44 | 3.77 | 4.28 | 3.91 | ns |
| LVC MOS15, Fast, 4 mA | 0.64 | 0.73 | 0.85 | 0.85 | 2.37 | 2.53 | 2.78 | 2.66 | 2.37 | 2.53 | 2.78 | 2.66 | ns |
| LVC MOS15, Fast, 6 mA | 0.64 | 0.73 | 0.85 | 0.85 | 1.80 | 2.05 | 2.42 | 2.16 | 1.80 | 2.05 | 2.42 | 2.16 | ns |
| LVC MOS15, Fast, 8 mA | 0.64 | 0.73 | 0.85 | 0.85 | 1.76 | 1.90 | 2.11 | 2.04 | 1.76 | 1.90 | 2.11 | 2.04 | ns |
| LVC MOS15, Fast, 12 mA | 0.64 | 0.73 | 0.85 | 0.85 | 1.64 | 1.77 | 1.97 | 1.90 | 1.64 | 1.77 | 1.97 | 1.90 | ns |
| LVC MOS15, Fast, 16 mA | 0.64 | 0.73 | 0.85 | 0.85 | 1.62 | 1.76 | 1.96 | 1.92 | 1.62 | 1.76 | 1.96 | 1.92 | ns |
| LVC MOS12, Slow, 2 mA | 0.72 | 0.81 | 0.93 | 0.95 | 3.14 | 3.39 | 3.75 | 3.54 | 3.14 | 3.39 | 3.75 | 3.54 | ns |
| LVC MOS12, Slow, 4 mA | 0.72 | 0.81 | 0.93 | 0.95 | 2.43 | 2.63 | 2.93 | 2.79 | 2.43 | 2.63 | 2.93 | 2.79 | ns |
| LVC MOS12, Slow, 6 mA | 0.72 | 0.81 | 0.93 | 0.95 | 1.92 | 2.11 | 2.41 | 2.26 | 1.92 | 2.11 | 2.41 | 2.26 | ns |
| LVC MOS12, Slow, 8 mA | 0.72 | 0.81 | 0.93 | 0.95 | 1.87 | 2.02 | 2.25 | 2.17 | 1.87 | 2.02 | 2.25 | 2.17 | ns |
| LVC MOS12, Fast, 2 mA | 0.72 | 0.81 | 0.93 | 0.95 | 2.71 | 2.98 | 3.39 | 3.11 | 2.71 | 2.98 | 3.39 | 3.11 | ns |
| LVC MOS12, Fast, 4 mA | 0.72 | 0.81 | 0.93 | 0.95 | 1.93 | 2.16 | 2.51 | 2.31 | 1.93 | 2.16 | 2.51 | 2.31 | ns |
| LVC MOS12, Fast, 6 mA | 0.72 | 0.81 | 0.93 | 0.95 | 1.75 | 1.89 | 2.11 | 2.05 | 1.75 | 1.89 | 2.11 | 2.05 | ns |
| LVC MOS12, Fast, 8 mA | 0.72 | 0.81 | 0.93 | 0.95 | 1.69 | 1.82 | 2.02 | 1.98 | 1.69 | 1.82 | 2.02 | 1.98 | ns |
| LVDCI_25 | 0.51 | 0.57 | 0.66 | 0.70 | 2.05 | 2.14 | 2.26 | 2.26 | 2.05 | 2.14 | 2.26 | 2.26 | ns |
| LVDCI_18 | 0.55 | 0.61 | 0.71 | 0.73 | 2.07 | 2.23 | 2.47 | 2.38 | 2.07 | 2.23 | 2.47 | 2.38 | ns |
| LVDCI_15 | 0.64 | 0.73 | 0.85 | 0.85 | 1.85 | 2.01 | 2.24 | 2.18 | 1.85 | 2.01 | 2.24 | 2.18 | ns |

Table 44: IOB Switching Characteristics for the Commercial (XC) Virtex-6 Devices (Cont'd)

| I/O Standard | T _{IOPI} | | | | T _{IOOP} | | | | T _{IOTP} | | | | Units |
|-----------------------|-------------------|------|------|------|-------------------|------|------|------|-------------------|------|------|------|-------|
| | Speed Grade | | | | Speed Grade | | | | Speed Grade | | | | |
| | -3 | -2 | -1 | -1L | -3 | -2 | -1 | -1L | -3 | -2 | -1 | -1L | |
| LVDCI_DV2_25 | 0.51 | 0.57 | 0.66 | 0.70 | 1.71 | 1.83 | 2.01 | 2.00 | 1.71 | 1.83 | 2.01 | 2.00 | ns |
| LVDCI_DV2_18 | 0.55 | 0.61 | 0.71 | 0.73 | 1.69 | 1.81 | 2.00 | 1.98 | 1.69 | 1.81 | 2.00 | 1.98 | ns |
| LVDCI_DV2_15 | 0.64 | 0.73 | 0.85 | 0.85 | 1.68 | 1.77 | 1.91 | 1.98 | 1.68 | 1.77 | 1.91 | 1.98 | ns |
| LVPECL_25 | 0.85 | 0.94 | 1.09 | 1.08 | 1.38 | 1.49 | 1.65 | 1.64 | 1.38 | 1.49 | 1.65 | 1.64 | ns |
| HSTL_I_12 | 0.81 | 0.91 | 1.06 | 1.06 | 1.48 | 1.60 | 1.78 | 1.74 | 1.48 | 1.60 | 1.78 | 1.74 | ns |
| HSTL_I_DCI | 0.81 | 0.91 | 1.06 | 1.06 | 1.40 | 1.50 | 1.66 | 1.64 | 1.40 | 1.50 | 1.66 | 1.64 | ns |
| HSTL_II_DCI | 0.81 | 0.91 | 1.06 | 1.06 | 1.37 | 1.49 | 1.68 | 1.66 | 1.37 | 1.49 | 1.68 | 1.66 | ns |
| HSTL_II_T_DCI | 0.81 | 0.91 | 1.06 | 1.06 | 1.40 | 1.50 | 1.66 | 1.64 | 1.40 | 1.50 | 1.66 | 1.64 | ns |
| HSTL_III_DCI | 0.81 | 0.91 | 1.06 | 1.06 | 1.34 | 1.45 | 1.62 | 1.61 | 1.34 | 1.45 | 1.62 | 1.61 | ns |
| HSTL_I_DCI_18 | 0.81 | 0.91 | 1.06 | 1.06 | 1.42 | 1.53 | 1.68 | 1.66 | 1.42 | 1.53 | 1.68 | 1.66 | ns |
| HSTL_II_DCI_18 | 0.81 | 0.91 | 1.06 | 1.06 | 1.36 | 1.46 | 1.62 | 1.59 | 1.36 | 1.46 | 1.62 | 1.59 | ns |
| HSTL_II_T_DCI_18 | 0.81 | 0.91 | 1.06 | 1.06 | 1.42 | 1.53 | 1.68 | 1.66 | 1.42 | 1.53 | 1.68 | 1.66 | ns |
| HSTL_III_DCI_18 | 0.81 | 0.91 | 1.06 | 1.06 | 1.43 | 1.54 | 1.69 | 1.67 | 1.43 | 1.54 | 1.69 | 1.67 | ns |
| DIFF_HSTL_I_18 | 0.85 | 0.94 | 1.09 | 1.08 | 1.47 | 1.58 | 1.75 | 1.72 | 1.47 | 1.58 | 1.75 | 1.72 | ns |
| DIFF_HSTL_I_DCI_18 | 0.85 | 0.94 | 1.09 | 1.08 | 1.42 | 1.53 | 1.68 | 1.66 | 1.42 | 1.53 | 1.68 | 1.66 | ns |
| DIFF_HSTL_I | 0.85 | 0.94 | 1.09 | 1.08 | 1.45 | 1.56 | 1.73 | 1.71 | 1.45 | 1.56 | 1.73 | 1.71 | ns |
| DIFF_HSTL_I_DCI | 0.85 | 0.94 | 1.09 | 1.08 | 1.40 | 1.50 | 1.66 | 1.64 | 1.40 | 1.50 | 1.66 | 1.64 | ns |
| DIFF_HSTL_II_18 | 0.85 | 0.94 | 1.09 | 1.08 | 1.50 | 1.62 | 1.81 | 1.78 | 1.50 | 1.62 | 1.81 | 1.78 | ns |
| DIFF_HSTL_II_DCI_18 | 0.85 | 0.94 | 1.09 | 1.08 | 1.36 | 1.46 | 1.62 | 1.59 | 1.36 | 1.46 | 1.62 | 1.59 | ns |
| DIFF_HSTL_II_T_DCI_18 | 0.85 | 0.94 | 1.09 | 1.08 | 1.42 | 1.53 | 1.68 | 1.66 | 1.42 | 1.53 | 1.68 | 1.66 | ns |
| DIFF_HSTL_II | 0.85 | 0.94 | 1.09 | 1.08 | 1.44 | 1.56 | 1.74 | 1.72 | 1.44 | 1.56 | 1.74 | 1.72 | ns |
| DIFF_HSTL_II_DCI | 0.85 | 0.94 | 1.09 | 1.08 | 1.37 | 1.49 | 1.68 | 1.66 | 1.37 | 1.49 | 1.68 | 1.66 | ns |
| SSTL2_I_DCI | 0.81 | 0.91 | 1.06 | 1.06 | 1.42 | 1.53 | 1.70 | 1.68 | 1.42 | 1.53 | 1.70 | 1.68 | ns |
| SSTL2_II_DCI | 0.81 | 0.91 | 1.06 | 1.06 | 1.39 | 1.50 | 1.67 | 1.69 | 1.39 | 1.50 | 1.67 | 1.69 | ns |
| SSTL2_II_T_DCI | 0.81 | 0.91 | 1.06 | 1.06 | 1.42 | 1.53 | 1.70 | 1.68 | 1.42 | 1.53 | 1.70 | 1.68 | ns |
| SSTL18_I | 0.81 | 0.91 | 1.06 | 1.06 | 1.47 | 1.58 | 1.75 | 1.73 | 1.47 | 1.58 | 1.75 | 1.73 | ns |
| SSTL18_II | 0.81 | 0.91 | 1.06 | 1.06 | 1.39 | 1.50 | 1.67 | 1.66 | 1.39 | 1.50 | 1.67 | 1.66 | ns |
| SSTL18_I_DCI | 0.81 | 0.91 | 1.06 | 1.06 | 1.40 | 1.51 | 1.67 | 1.65 | 1.40 | 1.51 | 1.67 | 1.65 | ns |
| SSTL18_II_DCI | 0.81 | 0.91 | 1.06 | 1.06 | 1.36 | 1.47 | 1.63 | 1.62 | 1.36 | 1.47 | 1.63 | 1.62 | ns |
| SSTL18_II_T_DCI | 0.81 | 0.91 | 1.06 | 1.06 | 1.40 | 1.51 | 1.67 | 1.65 | 1.40 | 1.51 | 1.67 | 1.65 | ns |
| SSTL15_T_DCI | 0.81 | 0.91 | 1.06 | 1.06 | 1.41 | 1.52 | 1.68 | 1.66 | 1.41 | 1.52 | 1.68 | 1.66 | ns |
| SSTL15_DCI | 0.81 | 0.91 | 1.06 | 1.06 | 1.41 | 1.52 | 1.68 | 1.66 | 1.41 | 1.52 | 1.68 | 1.66 | ns |
| DIFF_SSTL2_I | 0.85 | 0.94 | 1.09 | 1.08 | 1.49 | 1.60 | 1.77 | 1.74 | 1.49 | 1.60 | 1.77 | 1.74 | ns |
| DIFF_SSTL2_I_DCI | 0.85 | 0.94 | 1.09 | 1.08 | 1.42 | 1.53 | 1.70 | 1.68 | 1.42 | 1.53 | 1.70 | 1.68 | ns |
| DIFF_SSTL2_II | 0.85 | 0.94 | 1.09 | 1.08 | 1.42 | 1.54 | 1.72 | 1.71 | 1.42 | 1.54 | 1.72 | 1.71 | ns |
| DIFF_SSTL2_II_DCI | 0.85 | 0.94 | 1.09 | 1.08 | 1.39 | 1.50 | 1.67 | 1.69 | 1.39 | 1.50 | 1.67 | 1.69 | ns |
| DIFF_SSTL2_II_T_DCI | 0.85 | 0.94 | 1.09 | 1.08 | 1.42 | 1.53 | 1.70 | 1.68 | 1.42 | 1.53 | 1.70 | 1.68 | ns |

Table 44: IOB Switching Characteristics for the Commercial (XC) Virtex-6 Devices (Cont'd)

| I/O Standard | T _{IOPI} | | | | T _{IOOP} | | | | T _{IOTP} | | | | Units |
|----------------------|-------------------|------|------|------|-------------------|------|------|------|-------------------|------|------|------|-------|
| | Speed Grade | | | | Speed Grade | | | | Speed Grade | | | | |
| | -3 | -2 | -1 | -1L | -3 | -2 | -1 | -1L | -3 | -2 | -1 | -1L | |
| DIFF_SSTL18_I | 0.85 | 0.94 | 1.09 | 1.08 | 1.47 | 1.58 | 1.75 | 1.73 | 1.47 | 1.58 | 1.75 | 1.73 | ns |
| DIFF_SSTL18_I_DCI | 0.85 | 0.94 | 1.09 | 1.08 | 1.40 | 1.51 | 1.67 | 1.65 | 1.40 | 1.51 | 1.67 | 1.65 | ns |
| DIFF_SSTL18_II | 0.85 | 0.94 | 1.09 | 1.08 | 1.39 | 1.50 | 1.67 | 1.66 | 1.39 | 1.50 | 1.67 | 1.66 | ns |
| DIFF_SSTL18_II_DCI | 0.85 | 0.94 | 1.09 | 1.08 | 1.36 | 1.47 | 1.63 | 1.62 | 1.36 | 1.47 | 1.63 | 1.62 | ns |
| DIFF_SSTL18_II_T_DCI | 0.85 | 0.94 | 1.09 | 1.08 | 1.40 | 1.51 | 1.67 | 1.65 | 1.40 | 1.51 | 1.67 | 1.65 | ns |
| DIFF_SSTL15 | 0.81 | 0.91 | 1.06 | 1.06 | 1.42 | 1.54 | 1.71 | 1.69 | 1.42 | 1.54 | 1.71 | 1.69 | ns |
| DIFF_SSTL15_DCI | 0.81 | 0.91 | 1.06 | 1.06 | 1.41 | 1.52 | 1.68 | 1.66 | 1.41 | 1.52 | 1.68 | 1.66 | ns |
| DIFF_SSTL15_T_DCI | 0.81 | 0.91 | 1.06 | 1.06 | 1.41 | 1.52 | 1.68 | 1.66 | 1.41 | 1.52 | 1.68 | 1.66 | ns |

Table 45: IOB Switching Characteristics for the Defense-grade (XQ) Virtex-6 Devices

| I/O Standard | T _{IOPI} | | | T _{IOOP} | | | T _{IOTP} | | | Units |
|--------------------------|-------------------|------|------|-------------------|------|------|-------------------|------|------|-------|
| | Speed Grade | | | Speed Grade | | | Speed Grade | | | |
| | -2 | -1 | -1L | -2 | -1 | -1L | -2 | -1 | -1L | |
| LVDS_25 | 0.94 | 1.09 | 1.08 | 1.54 | 2.16 | 1.62 | 1.54 | 2.16 | 1.62 | ns |
| LVDSEXT_25 | 0.94 | 1.09 | 1.08 | 1.65 | 2.20 | 1.73 | 1.65 | 2.20 | 1.73 | ns |
| HT_25 | 0.94 | 1.09 | 1.08 | 1.62 | 2.20 | 1.69 | 1.62 | 2.20 | 1.69 | ns |
| BLVDS_25 | 0.94 | 1.09 | 1.08 | 1.50 | 3.18 | 1.65 | 1.50 | 3.18 | 1.65 | ns |
| RSDS_25 (point to point) | 0.94 | 1.09 | 1.08 | 1.54 | 2.22 | 1.62 | 1.54 | 2.22 | 1.62 | ns |
| HSTL_I | 0.91 | 1.06 | 1.06 | 1.56 | 2.44 | 1.71 | 1.56 | 2.44 | 1.71 | ns |
| HSTL_II | 0.91 | 1.06 | 1.06 | 1.56 | 2.21 | 1.72 | 1.56 | 2.21 | 1.72 | ns |
| HSTL_III | 0.91 | 1.06 | 1.06 | 1.54 | 2.50 | 1.69 | 1.54 | 2.50 | 1.69 | ns |
| HSTL_I_18 | 0.91 | 1.06 | 1.06 | 1.58 | 2.43 | 1.72 | 1.58 | 2.43 | 1.72 | ns |
| HSTL_II_18 | 0.91 | 1.06 | 1.06 | 1.62 | 2.30 | 1.78 | 1.62 | 2.30 | 1.78 | ns |
| HSTL_III_18 | 0.91 | 1.06 | 1.06 | 1.54 | 2.49 | 1.69 | 1.54 | 2.49 | 1.69 | ns |
| SSTL2_I | 0.91 | 1.06 | 1.06 | 1.60 | 2.50 | 1.74 | 1.60 | 2.50 | 1.74 | ns |
| SSTL2_II | 0.91 | 1.06 | 1.06 | 1.54 | 2.49 | 1.71 | 1.54 | 2.49 | 1.71 | ns |
| SSTL15 | 0.91 | 1.06 | 1.06 | 1.54 | 2.07 | 1.69 | 1.54 | 2.07 | 1.69 | ns |
| LVC MOS25, Slow, 2 mA | 0.57 | 0.66 | 0.70 | 5.46 | 6.01 | 5.63 | 5.46 | 6.01 | 5.63 | ns |
| LVC MOS25, Slow, 4 mA | 0.57 | 0.66 | 0.70 | 3.49 | 3.79 | 3.65 | 3.49 | 3.79 | 3.65 | ns |
| LVC MOS25, Slow, 6 mA | 0.57 | 0.66 | 0.70 | 2.81 | 3.08 | 2.95 | 2.81 | 3.08 | 2.95 | ns |
| LVC MOS25, Slow, 8 mA | 0.57 | 0.66 | 0.70 | 2.41 | 2.72 | 2.59 | 2.41 | 2.72 | 2.59 | ns |
| LVC MOS25, Slow, 12 mA | 0.57 | 0.66 | 0.70 | 1.95 | 2.23 | 2.10 | 1.95 | 2.23 | 2.10 | ns |
| LVC MOS25, Slow, 16 mA | 0.57 | 0.66 | 0.70 | 2.05 | 2.29 | 2.21 | 2.05 | 2.29 | 2.21 | ns |
| LVC MOS25, Slow, 24 mA | 0.57 | 0.66 | 0.70 | 1.82 | 2.24 | 1.98 | 1.82 | 2.24 | 1.98 | ns |
| LVC MOS25, Fast, 2 mA | 0.57 | 0.66 | 0.70 | 5.49 | 6.04 | 5.62 | 5.49 | 6.04 | 5.62 | ns |
| LVC MOS25, Fast, 4 mA | 0.57 | 0.66 | 0.70 | 3.50 | 3.82 | 3.65 | 3.50 | 3.82 | 3.65 | ns |
| LVC MOS25, Fast, 6 mA | 0.57 | 0.66 | 0.70 | 2.73 | 2.99 | 2.88 | 2.73 | 2.99 | 2.88 | ns |
| LVC MOS25, Fast, 8 mA | 0.57 | 0.66 | 0.70 | 2.33 | 2.65 | 2.53 | 2.33 | 2.65 | 2.53 | ns |
| LVC MOS25, Fast, 12 mA | 0.57 | 0.66 | 0.70 | 1.88 | 2.08 | 2.03 | 1.88 | 2.08 | 2.03 | ns |

Table 45: IOB Switching Characteristics for the Defense-grade (XQ) Virtex-6 Devices (Cont'd)

| I/O Standard | T _{IOP1} | | | T _{IOP} | | | T _{IOTP} | | | Units |
|------------------------|-------------------|------|------|------------------|------|------|-------------------|------|------|-------|
| | Speed Grade | | | Speed Grade | | | Speed Grade | | | |
| | -2 | -1 | -1L | -2 | -1 | -1L | -2 | -1 | -1L | |
| LVC MOS25, Fast, 16 mA | 0.57 | 0.66 | 0.70 | 1.92 | 2.15 | 2.08 | 1.92 | 2.15 | 2.08 | ns |
| LVC MOS25, Fast, 24 mA | 0.57 | 0.66 | 0.70 | 1.79 | 2.15 | 1.96 | 1.79 | 2.15 | 1.96 | ns |
| LVC MOS18, Slow, 2 mA | 0.61 | 0.71 | 0.73 | 4.47 | 4.87 | 4.30 | 4.47 | 4.87 | 4.30 | ns |
| LVC MOS18, Slow, 4 mA | 0.61 | 0.71 | 0.73 | 2.96 | 3.21 | 2.94 | 2.96 | 3.21 | 2.94 | ns |
| LVC MOS18, Slow, 6 mA | 0.61 | 0.71 | 0.73 | 2.43 | 2.64 | 2.47 | 2.43 | 2.64 | 2.47 | ns |
| LVC MOS18, Slow, 8 mA | 0.61 | 0.71 | 0.73 | 2.11 | 2.41 | 2.24 | 2.11 | 2.41 | 2.24 | ns |
| LVC MOS18, Slow, 12 mA | 0.61 | 0.71 | 0.73 | 1.99 | 2.30 | 2.10 | 1.99 | 2.30 | 2.10 | ns |
| LVC MOS18, Slow, 16 mA | 0.61 | 0.71 | 0.73 | 1.95 | 2.30 | 2.04 | 1.95 | 2.30 | 2.04 | ns |
| LVC MOS18, Fast, 2 mA | 0.61 | 0.71 | 0.73 | 4.23 | 4.57 | 4.08 | 4.23 | 4.57 | 4.08 | ns |
| LVC MOS18, Fast, 4 mA | 0.61 | 0.71 | 0.73 | 2.76 | 2.97 | 2.74 | 2.76 | 2.97 | 2.74 | ns |
| LVC MOS18, Fast, 6 mA | 0.61 | 0.71 | 0.73 | 2.28 | 2.46 | 2.32 | 2.28 | 2.46 | 2.32 | ns |
| LVC MOS18, Fast, 8 mA | 0.61 | 0.71 | 0.73 | 1.99 | 2.34 | 2.14 | 1.99 | 2.34 | 2.14 | ns |
| LVC MOS18, Fast, 12 mA | 0.61 | 0.71 | 0.73 | 1.80 | 2.19 | 1.88 | 1.80 | 2.19 | 1.88 | ns |
| LVC MOS18, Fast, 16 mA | 0.61 | 0.71 | 0.73 | 1.74 | 2.18 | 1.88 | 1.74 | 2.18 | 1.88 | ns |
| LVC MOS15, Slow, 2 mA | 0.73 | 0.85 | 0.85 | 3.77 | 4.29 | 3.91 | 3.77 | 4.29 | 3.91 | ns |
| LVC MOS15, Slow, 4 mA | 0.73 | 0.85 | 0.85 | 2.79 | 3.10 | 2.93 | 2.79 | 3.10 | 2.93 | ns |
| LVC MOS15, Slow, 6 mA | 0.73 | 0.85 | 0.85 | 2.32 | 2.68 | 2.50 | 2.32 | 2.68 | 2.50 | ns |
| LVC MOS15, Slow, 8 mA | 0.73 | 0.85 | 0.85 | 1.98 | 2.29 | 2.24 | 1.98 | 2.29 | 2.24 | ns |
| LVC MOS15, Slow, 12 mA | 0.73 | 0.85 | 0.85 | 1.91 | 2.23 | 2.07 | 1.91 | 2.23 | 2.07 | ns |
| LVC MOS15, Slow, 16 mA | 0.73 | 0.85 | 0.85 | 1.83 | 2.23 | 1.98 | 1.83 | 2.23 | 1.98 | ns |
| LVC MOS15, Fast, 2 mA | 0.73 | 0.85 | 0.85 | 3.77 | 4.28 | 3.91 | 3.77 | 4.28 | 3.91 | ns |
| LVC MOS15, Fast, 4 mA | 0.73 | 0.85 | 0.85 | 2.53 | 2.78 | 2.66 | 2.53 | 2.78 | 2.66 | ns |
| LVC MOS15, Fast, 6 mA | 0.73 | 0.85 | 0.85 | 2.05 | 2.42 | 2.16 | 2.05 | 2.42 | 2.16 | ns |
| LVC MOS15, Fast, 8 mA | 0.73 | 0.85 | 0.85 | 1.90 | 2.20 | 2.04 | 1.90 | 2.20 | 2.04 | ns |
| LVC MOS15, Fast, 12 mA | 0.73 | 0.85 | 0.85 | 1.77 | 2.11 | 1.90 | 1.77 | 2.11 | 1.90 | ns |
| LVC MOS15, Fast, 16 mA | 0.73 | 0.85 | 0.85 | 1.76 | 2.11 | 1.92 | 1.76 | 2.11 | 1.92 | ns |
| LVC MOS12, Slow, 2 mA | 0.81 | 0.93 | 0.95 | 3.39 | 3.75 | 3.54 | 3.39 | 3.75 | 3.54 | ns |
| LVC MOS12, Slow, 4 mA | 0.81 | 0.93 | 0.95 | 2.63 | 2.93 | 2.79 | 2.63 | 2.93 | 2.79 | ns |
| LVC MOS12, Slow, 6 mA | 0.81 | 0.93 | 0.95 | 2.11 | 2.67 | 2.26 | 2.11 | 2.67 | 2.26 | ns |
| LVC MOS12, Slow, 8 mA | 0.81 | 0.93 | 0.95 | 2.02 | 2.25 | 2.17 | 2.02 | 2.25 | 2.17 | ns |
| LVC MOS12, Fast, 2 mA | 0.81 | 0.93 | 0.95 | 2.98 | 3.39 | 3.11 | 2.98 | 3.39 | 3.11 | ns |
| LVC MOS12, Fast, 4 mA | 0.81 | 0.93 | 0.95 | 2.16 | 2.70 | 2.31 | 2.16 | 2.70 | 2.31 | ns |
| LVC MOS12, Fast, 6 mA | 0.81 | 0.93 | 0.95 | 1.89 | 2.34 | 2.05 | 1.89 | 2.34 | 2.05 | ns |
| LVC MOS12, Fast, 8 mA | 0.81 | 0.93 | 0.95 | 1.82 | 2.10 | 1.98 | 1.82 | 2.10 | 1.98 | ns |
| LVDCI_25 | 0.57 | 0.70 | 0.70 | 2.14 | 2.82 | 2.26 | 2.14 | 2.82 | 2.26 | ns |
| LVDCI_18 | 0.61 | 0.71 | 0.73 | 2.23 | 2.78 | 2.38 | 2.23 | 2.78 | 2.38 | ns |
| LVDCI_15 | 0.73 | 0.85 | 0.85 | 2.01 | 2.75 | 2.18 | 2.01 | 2.75 | 2.18 | ns |
| LVDCI_DV2_25 | 0.57 | 0.70 | 0.70 | 1.83 | 2.37 | 2.00 | 1.83 | 2.37 | 2.00 | ns |

Table 45: IOB Switching Characteristics for the Defense-grade (XQ) Virtex-6 Devices (Cont'd)

| I/O Standard | T _{IOPI} | | | T _{IOOP} | | | T _{IOTP} | | | Units |
|-----------------------|-------------------|------|------|-------------------|------|------|-------------------|------|------|-------|
| | Speed Grade | | | Speed Grade | | | Speed Grade | | | |
| | -2 | -1 | -1L | -2 | -1 | -1L | -2 | -1 | -1L | |
| LVDCI_DV2_18 | 0.61 | 0.72 | 0.73 | 1.81 | 2.36 | 1.98 | 1.81 | 2.36 | 1.98 | ns |
| LVDCI_DV2_15 | 0.73 | 0.85 | 0.85 | 1.77 | 2.30 | 1.98 | 1.77 | 2.30 | 1.98 | ns |
| LVPECL_25 | 0.94 | 1.09 | 1.08 | 1.49 | 2.68 | 1.64 | 1.49 | 2.68 | 1.64 | ns |
| HSTL_I_12 | 0.91 | 1.06 | 1.06 | 1.60 | 2.48 | 1.74 | 1.60 | 2.48 | 1.74 | ns |
| HSTL_I_DCI | 0.91 | 1.06 | 1.06 | 1.50 | 2.43 | 1.64 | 1.50 | 2.43 | 1.64 | ns |
| HSTL_II_DCI | 0.91 | 1.06 | 1.06 | 1.49 | 2.39 | 1.66 | 1.49 | 2.39 | 1.66 | ns |
| HSTL_II_T_DCI | 0.91 | 1.06 | 1.06 | 1.50 | 2.43 | 1.64 | 1.50 | 2.43 | 1.64 | ns |
| HSTL_III_DCI | 0.91 | 1.06 | 1.06 | 1.45 | 2.48 | 1.61 | 1.45 | 2.48 | 1.61 | ns |
| HSTL_I_DCI_18 | 0.91 | 1.06 | 1.06 | 1.53 | 2.44 | 1.66 | 1.53 | 2.44 | 1.66 | ns |
| HSTL_II_DCI_18 | 0.91 | 1.06 | 1.06 | 1.46 | 2.41 | 1.59 | 1.46 | 2.41 | 1.59 | ns |
| HSTL_II_T_DCI_18 | 0.91 | 1.06 | 1.06 | 1.53 | 2.43 | 1.66 | 1.53 | 2.43 | 1.66 | ns |
| HSTL_III_DCI_18 | 0.91 | 1.06 | 1.06 | 1.54 | 2.50 | 1.67 | 1.54 | 2.50 | 1.67 | ns |
| DIFF_HSTL_I_18 | 0.94 | 1.09 | 1.08 | 1.58 | 2.30 | 1.72 | 1.58 | 2.30 | 1.72 | ns |
| DIFF_HSTL_I_DCI_18 | 0.94 | 1.09 | 1.08 | 1.53 | 2.21 | 1.66 | 1.53 | 2.21 | 1.66 | ns |
| DIFF_HSTL_I | 0.94 | 1.09 | 1.08 | 1.56 | 2.28 | 1.71 | 1.56 | 2.28 | 1.71 | ns |
| DIFF_HSTL_I_DCI | 0.94 | 1.09 | 1.08 | 1.50 | 2.28 | 1.64 | 1.50 | 2.28 | 1.64 | ns |
| DIFF_HSTL_II_18 | 0.94 | 1.09 | 1.08 | 1.62 | 2.33 | 1.78 | 1.62 | 2.33 | 1.78 | ns |
| DIFF_HSTL_II_DCI_18 | 0.94 | 1.09 | 1.08 | 1.46 | 2.18 | 1.59 | 1.46 | 2.18 | 1.59 | ns |
| DIFF_HSTL_II_T_DCI_18 | 0.94 | 1.09 | 1.08 | 1.53 | 2.22 | 1.66 | 1.53 | 2.22 | 1.66 | ns |
| DIFF_HSTL_II | 0.94 | 1.09 | 1.08 | 1.56 | 2.29 | 1.72 | 1.56 | 2.29 | 1.72 | ns |
| DIFF_HSTL_II_DCI | 0.94 | 1.09 | 1.08 | 1.49 | 2.26 | 1.66 | 1.49 | 2.26 | 1.66 | ns |
| SSTL2_I_DCI | 0.91 | 1.06 | 1.06 | 1.53 | 2.51 | 1.68 | 1.53 | 2.51 | 1.68 | ns |
| SSTL2_II_DCI | 0.91 | 1.06 | 1.06 | 1.50 | 2.50 | 1.69 | 1.50 | 2.50 | 1.69 | ns |
| SSTL2_II_T_DCI | 0.91 | 1.06 | 1.06 | 1.53 | 2.52 | 1.68 | 1.53 | 2.52 | 1.68 | ns |
| SSTL18_I | 0.91 | 1.06 | 1.06 | 1.58 | 2.48 | 1.73 | 1.58 | 2.48 | 1.73 | ns |
| SSTL18_II | 0.91 | 1.06 | 1.06 | 1.50 | 2.46 | 1.66 | 1.50 | 2.46 | 1.66 | ns |
| SSTL18_I_DCI | 0.91 | 1.06 | 1.06 | 1.51 | 2.49 | 1.65 | 1.51 | 2.49 | 1.65 | ns |
| SSTL18_II_DCI | 0.91 | 1.06 | 1.06 | 1.47 | 2.41 | 1.62 | 1.47 | 2.41 | 1.62 | ns |
| SSTL18_II_T_DCI | 0.91 | 1.06 | 1.06 | 1.51 | 2.49 | 1.65 | 1.51 | 2.49 | 1.65 | ns |
| SSTL15_T_DCI | 0.91 | 1.06 | 1.06 | 1.52 | 2.48 | 1.66 | 1.52 | 2.48 | 1.66 | ns |
| SSTL15_DCI | 0.91 | 1.06 | 1.06 | 1.52 | 2.48 | 1.66 | 1.52 | 2.48 | 1.66 | ns |
| DIFF_SSTL2_I | 0.94 | 1.09 | 1.08 | 1.60 | 2.34 | 1.74 | 1.60 | 2.34 | 1.74 | ns |
| DIFF_SSTL2_I_DCI | 0.94 | 1.09 | 1.08 | 1.53 | 2.25 | 1.68 | 1.53 | 2.25 | 1.68 | ns |
| DIFF_SSTL2_II | 0.94 | 1.09 | 1.08 | 1.54 | 2.29 | 1.71 | 1.54 | 2.29 | 1.71 | ns |
| DIFF_SSTL2_II_DCI | 0.94 | 1.09 | 1.08 | 1.50 | 2.23 | 1.69 | 1.50 | 2.23 | 1.69 | ns |
| DIFF_SSTL2_II_T_DCI | 0.94 | 1.09 | 1.08 | 1.53 | 2.26 | 1.68 | 1.53 | 2.26 | 1.68 | ns |
| DIFF_SSTL18_I | 0.94 | 1.09 | 1.08 | 1.58 | 2.22 | 1.73 | 1.58 | 2.22 | 1.73 | ns |
| DIFF_SSTL18_I_DCI | 0.94 | 1.09 | 1.08 | 1.51 | 2.30 | 1.65 | 1.51 | 2.30 | 1.65 | ns |

Table 45: IOB Switching Characteristics for the Defense-grade (XQ) Virtex-6 Devices (Cont'd)

| I/O Standard | T_{IOPI} | | | T_{IOOP} | | | T_{IOTP} | | | Units |
|----------------------|-------------|------|------|-------------|------|------|-------------|------|------|-------|
| | Speed Grade | | | Speed Grade | | | Speed Grade | | | |
| | -2 | -1 | -1L | -2 | -1 | -1L | -2 | -1 | -1L | |
| DIFF_SSTL18_II | 0.94 | 1.09 | 1.08 | 1.50 | 2.27 | 1.66 | 1.50 | 2.27 | 1.66 | ns |
| DIFF_SSTL18_II_DCI | 0.94 | 1.09 | 1.08 | 1.47 | 2.20 | 1.62 | 1.47 | 2.20 | 1.62 | ns |
| DIFF_SSTL18_II_T_DCI | 0.94 | 1.09 | 1.08 | 1.51 | 2.30 | 1.65 | 1.51 | 2.30 | 1.65 | ns |
| DIFF_SSTL15 | 0.91 | 1.06 | 1.06 | 1.54 | 2.25 | 1.69 | 1.54 | 2.25 | 1.69 | ns |
| DIFF_SSTL15_DCI | 0.91 | 1.06 | 1.06 | 1.52 | 2.25 | 1.66 | 1.52 | 2.25 | 1.66 | ns |
| DIFF_SSTL15_T_DCI | 0.91 | 1.06 | 1.06 | 1.52 | 2.25 | 1.66 | 1.52 | 2.25 | 1.66 | ns |

Table 46: IOB 3-state ON Output Switching Characteristics (T_{IOTPHZ})

| Symbol | Description | Speed Grade | | | | Units |
|--------------|-------------------------------|-------------|------|------|------|-------|
| | | -3 | -2 | -1 | -1L | |
| T_{IOTPHZ} | T input to Pad high-impedance | 0.86 | 0.92 | 0.99 | 0.99 | ns |

I/O Standard Adjustment Measurement Methodology

Input Delay Measurements

Table 47 shows the test setup parameters used for measuring input delay.

Table 47: Input Delay Measurement Methodology

| Description | I/O Standard Attribute | $V_L^{(1)(2)}$ | $V_H^{(1)(2)}$ | $V_{MEAS}^{(1)(4)(5)}$ | $V_{REF}^{(1)(3)(5)}$ |
|--|------------------------|------------------|------------------|------------------------|-----------------------|
| LVC MOS, 2.5V | LVC MOS25 | 0 | 2.5 | 1.25 | – |
| LVC MOS, 1.8V | LVC MOS18 | 0 | 1.8 | 0.9 | – |
| LVC MOS, 1.5V | LVC MOS15 | 0 | 1.5 | 0.75 | – |
| HSTL (High-Speed Transceiver Logic), Class I & II | HSTL_I, HSTL_II | $V_{REF} - 0.5$ | $V_{REF} + 0.5$ | V_{REF} | 0.75 |
| HSTL, Class III | HSTL_III | $V_{REF} - 0.5$ | $V_{REF} + 0.5$ | V_{REF} | 0.90 |
| HSTL, Class I & II, 1.8V | HSTL_I_18, HSTL_II_18 | $V_{REF} - 0.5$ | $V_{REF} + 0.5$ | V_{REF} | 0.90 |
| HSTL, Class III 1.8V | HSTL_III_18 | $V_{REF} - 0.5$ | $V_{REF} + 0.5$ | V_{REF} | 1.08 |
| SSTL (Stub Terminated Transceiver Logic), Class I & II, 3.3V | SSTL3_I, SSTL3_II | $V_{REF} - 1.00$ | $V_{REF} + 1.00$ | V_{REF} | 1.5 |
| SSTL, Class I & II, 2.5V | SSTL2_I, SSTL2_II | $V_{REF} - 0.75$ | $V_{REF} + 0.75$ | V_{REF} | 1.25 |
| SSTL, Class I & II, 1.8V | SSTL18_I, SSTL18_II | $V_{REF} - 0.5$ | $V_{REF} + 0.5$ | V_{REF} | 0.90 |
| LVDS (Low-Voltage Differential Signaling), 2.5V | LVDS_25 | $1.2 - 0.125$ | $1.2 + 0.125$ | $0^{(6)}$ | – |
| LVDS EXT (LVDS Extended Mode), 2.5V | LVDS EXT_25 | $1.2 - 0.125$ | $1.2 + 0.125$ | $0^{(6)}$ | – |
| HT (HyperTransport), 2.5V | LDT_25 | $0.6 - 0.125$ | $0.6 + 0.125$ | $0^{(6)}$ | – |

Notes:

1. The input delay measurement methodology parameters for LVDCI are the same for LVC MOS standards of the same voltage. Input delay measurement methodology parameters for HSLVDCI are the same as for HSTL_II standards of the same voltage. Parameters for all other DCI standards are the same for the corresponding non-DCI standards.
2. Input waveform switches between V_L and V_H .
3. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst case of these measurements. V_{REF} values listed are typical.
4. Input voltage level from which measurement starts.
5. This is an input voltage reference that bears no relation to the V_{REF} / V_{MEAS} parameters found in IBIS models and/or noted in Figure 6.
6. The value given is the differential input voltage.

Output Delay Measurements

Output delays are measured using a Tektronix P6245 TDS500/600 probe (< 1 pF) across approximately 4" of FR4 microstrip trace. Standard termination was used for all testing. The propagation delay of the 4" trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setups shown in Figure 6 and Figure 7.

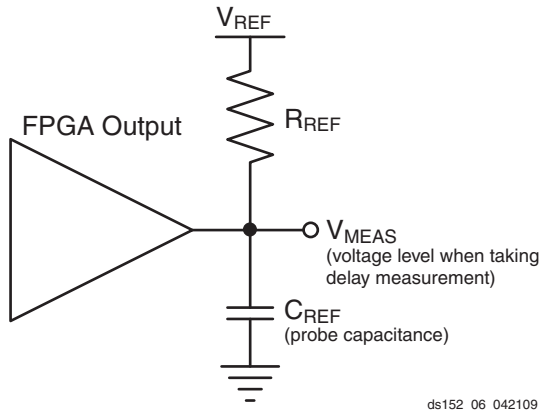


Figure 6: Single Ended Test Setup



ds152_07_042109

Figure 7: Differential Test Setup

Measurements and test conditions are reflected in the IBIS models except where the IBIS format precludes it. Parameters V_{REF} , R_{REF} , C_{REF} , and V_{MEAS} fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using the following method:

1. Simulate the output driver of choice into the generalized test setup, using values from Table 48.
2. Record the time to V_{MEAS} .
3. Simulate the output driver of choice into the actual PCB trace and load, using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS} .
5. Compare the results of steps 2 and 4. The increase or decrease in delay yields the actual propagation delay of the PCB trace.

Table 48: Output Delay Measurement Methodology

| Description | I/O Standard Attribute | R_{REF} (Ω) | $C_{REF}^{(1)}$ (pF) | V_{MEAS} (V) | V_{REF} (V) |
|--|------------------------|------------------------|----------------------|------------------|---------------|
| LVC MOS, 2.5V | LVC MOS25 | 1M | 0 | 1.25 | 0 |
| LVC MOS, 1.8V | LVC MOS18 | 1M | 0 | 0.9 | 0 |
| LVC MOS, 1.5V | LVC MOS15 | 1M | 0 | 0.75 | 0 |
| LVC MOS, 1.2V | LVC MOS12 | 1M | 0 | 0.75 | 0 |
| HSTL (High-Speed Transceiver Logic), Class I | HSTL_I | 50 | 0 | V_{REF} | 0.75 |
| HSTL, Class II | HSTL_II | 25 | 0 | V_{REF} | 0.75 |
| HSTL, Class III | HSTL_III | 50 | 0 | 0.9 | 1.5 |
| HSTL, Class I, 1.8V | HSTL_I_18 | 50 | 0 | V_{REF} | 0.9 |
| HSTL, Class II, 1.8V | HSTL_II_18 | 25 | 0 | V_{REF} | 0.9 |
| HSTL, Class III, 1.8V | HSTL_III_18 | 50 | 0 | 1.1 | 1.8 |
| SSTL (Stub Series Terminated Logic), Class I, 1.8V | SSTL18_I | 50 | 0 | V_{REF} | 0.9 |
| SSTL, Class II, 1.8V | SSTL18_II | 25 | 0 | V_{REF} | 0.9 |
| SSTL, Class I, 2.5V | SSTL2_I | 50 | 0 | V_{REF} | 1.25 |
| SSTL, Class II, 2.5V | SSTL2_II | 25 | 0 | V_{REF} | 1.25 |
| LVDS (Low-Voltage Differential Signaling), 2.5V | LVDS_25 | 100 | 0 | 0 ⁽²⁾ | 1.2 |
| LVDS EXT (LVDS Extended Mode), 2.5V | LVDS_25 | 100 | 0 | 0 ⁽²⁾ | 1.2 |
| BLVDS (Bus LVDS), 2.5V | BLVDS_25 | 100 | 0 | 0 ⁽²⁾ | 0 |

Table 48: Output Delay Measurement Methodology (Cont'd)

| Description | I/O Standard Attribute | R _{REF} (Ω) | C _{REF} ⁽¹⁾ (pF) | V _{MEAS} (V) | V _{REF} (V) |
|--|-------------------------------|----------------------|--------------------------------------|-----------------------|----------------------|
| HT (HyperTransport), 2.5V | LDT_25 | 100 | 0 | 0 ⁽²⁾ | 0.6 |
| LVPECL (Low-Voltage Positive Emitter-Coupled Logic), 2.5V | LVPECL_25 | 100 | 0 | 0 ⁽²⁾ | 0 |
| LVDCI/HSLVDCI, 2.5V | LVDCI_25, HSLVDCI_25 | 1M | 0 | 1.25 | 0 |
| LVDCI/HSLVDCI, 1.8V | LVDCI_18, HSLVDCI_18 | 1M | 0 | 0.9 | 0 |
| LVDCI/HSLVDCI, 1.5V | LVDCI_15, HSLVDCI_15 | 1M | 0 | 0.75 | 0 |
| HSTL (High-Speed Transceiver Logic), Class I & II, with DCI | HSTL_I_DCI, HSTL_II_DCI | 50 | 0 | V _{REF} | 0.75 |
| HSTL, Class III, with DCI | HSTL_III_DCI | 50 | 0 | 0.9 | 1.5 |
| HSTL, Class I & II, 1.8V, with DCI | HSTL_I_DCI_18, HSTL_II_DCI_18 | 50 | 0 | V _{REF} | 0.9 |
| HSTL, Class III, 1.8V, with DCI | HSTL_III_DCI_18 | 50 | 0 | 1.1 | 1.8 |
| SSTL (Stub Series Termi.Logic), Class I & II, 1.8V, with DCI | SSTL18_I_DCI, SSTL18_II_DCI | 50 | 0 | V _{REF} | 0.9 |
| SSTL, Class I & II, 2.5V, with DCI | SSTL2_I_DCI, SSTL2_II_DCI | 50 | 0 | V _{REF} | 1.25 |

Notes:

- C_{REF} is the capacitance of the probe, nominally 0 pF.
- The value given is the differential output voltage.

Input/Output Logic Switching Characteristics

Table 49: ILOGIC Switching Characteristics

| Symbol | Description | Speed Grade | | | | Units |
|--|---|----------------|----------------|----------------|----------------|---------|
| | | -3 | -2 | -1 | -1L | |
| Setup/Hold | | | | | | |
| T _{ICE1CK} /T _{ICKCE1} | CE1 pin Setup/Hold with respect to CLK | 0.21/ 0.03 | 0.25/ 0.04 | 0.27/ 0.04 | 0.31/ 0.05 | ns |
| T _{ISRCK} /T _{ICKSR} | SR pin Setup/Hold with respect to CLK | 0.66/ -0.08 | 0.78/ -0.08 | 0.96/ -0.08 | 1.09/ -0.11 | ns |
| T _{IDOCK} /T _{IOCKD} | D pin Setup/Hold with respect to CLK without Delay | 0.07/ 0.41 | 0.08/ 0.46 | 0.10/ 0.54 | 0.11/ 0.64 | ns |
| T _{IDOCKD} /T _{IOCKDD} | DDLY pin Setup/Hold with respect to CLK (using IODELAY) | 0.10/ 0.32 | 0.12/ 0.36 | 0.14/ 0.42 | 0.16/ 0.50 | ns |
| Combinatorial | | | | | | |
| T _{IDI} | D pin to O pin propagation delay, no Delay | 0.15 | 0.17 | 0.20 | 0.23 | ns |
| T _{IDID} | DDLY pin to O pin propagation delay (using IODELAY) | 0.19 | 0.22 | 0.25 | 0.28 | ns |
| Sequential Delays | | | | | | |
| T _{IDLO} | D pin to Q1 pin using flip-flop as a latch without Delay | 0.48 | 0.54 | 0.64 | 0.73 | ns |
| T _{IDLOD} | DDLY pin to Q1 pin using flip-flop as a latch (using IODELAY) | 0.52 | 0.58 | 0.68 | 0.78 | ns |
| T _{ICKQ} | CLK to Q outputs | 0.54 | 0.61 | 0.70 | 0.93 | ns |
| T _{RQ_ILOGIC} | SR pin to OQ/TQ out | 0.85 | 0.97 | 1.15 | 1.32 | ns |
| T _{GSRQ_ILOGIC} | Global Set/Reset to Q outputs | 7.60 | 7.60 | 10.51 | 10.51 | ns |
| Set/Reset | | | | | | |
| T _{RPW_ILOGIC} | Minimum Pulse Width, SR inputs | 0.78 | 0.95 | 1.20 | 1.30 | ns, Min |

Table 50: OLOGIC Switching Characteristics

| Symbol | Description | Speed Grade | | | | | Units |
|--------------------------|---|----------------|----------------|----------------|----------------|----------------|---------|
| | | -3 | -2 | -1 (XC) | -1 (XQ) | -1L | |
| Setup/Hold | | | | | | | |
| T_{ODCK}/T_{OCKD} | D1/D2 pins Setup/Hold with respect to CLK | 0.45/ -0.08 | 0.50/ -0.08 | 0.54/ -0.08 | 0.54/ -0.08 | 0.69/ -0.11 | ns |
| T_{OOCECK}/T_{OCKOCE} | OCE pin Setup/Hold with respect to CLK | 0.17/ -0.03 | 0.20/ -0.03 | 0.22/ -0.03 | 0.27/ -0.05 | 0.27/ -0.04 | ns |
| T_{OSRCK}/T_{OCKSR} | SR pin Setup/Hold with respect to CLK | 0.59/ -0.24 | 0.62/ -0.24 | 0.54/ -0.08 | 0.54/ -0.08 | 0.79/ -0.35 | ns |
| T_{OTCK}/T_{OCKT} | T1/T2 pins Setup/Hold with respect to CLK | 0.44/ -0.07 | 0.51/ -0.07 | 0.56/ -0.07 | 0.60/ -0.10 | 0.68/ -0.13 | ns |
| T_{OTCECK}/T_{OCKTCE} | TCE pin Setup/Hold with respect to CLK | 0.15/ -0.04 | 0.19/ -0.04 | 0.21/ -0.04 | 0.27/ -0.05 | 0.29/ -0.05 | ns |
| Combinatorial | | | | | | | |
| T_{DOQ} | D1 to OQ out or T1 to TQ out | 0.78 | 0.87 | 1.01 | 1.01 | 1.15 | ns |
| Sequential Delays | | | | | | | |
| T_{OCKQ} | CLK to OQ/TQ out | 0.54 | 0.61 | 0.71 | 0.71 | 0.80 | ns |
| T_{RQ} | SR pin to OQ/TQ out | 0.80 | 0.90 | 1.05 | 1.05 | 1.19 | ns |
| T_{GSRQ} | Global Set/Reset to Q outputs | 7.60 | 7.60 | 10.51 | 10.51 | 10.51 | ns |
| Set/Reset | | | | | | | |
| T_{RPW} | Minimum Pulse Width, SR inputs | 0.78 | 0.95 | 1.20 | 1.20 | 1.30 | ns, Min |

Input Serializer/Deserializer Switching Characteristics

Table 51: ISERDES Switching Characteristics

| Symbol | Description | Speed Grade | | | | | Units |
|---|---|---------------|---------------|---------------|---------------|----------------|-------|
| | | -3 | -2 | -1 (XC) | -1 (XQ) | -1L | |
| Setup/Hold for Control Lines | | | | | | | |
| $T_{ISCK_BITSLIP} / T_{ISCKC_BITSLIP}$ | BITSLIP pin Setup/Hold with respect to CLKDIV | 0.07/ 0.15 | 0.08/ 0.16 | 0.09/ 0.17 | 0.09/ 0.17 | 0.14/ 0.17 | ns |
| $T_{ISCK_CE} / T_{ISCKC_CE}^{(2)}$ | CE pin Setup/Hold with respect to CLK (for CE1) | 0.20/ 0.03 | 0.25/ 0.04 | 0.27/ 0.04 | 0.27/ 0.04 | 0.31/ 0.05 | ns |
| $T_{ISCK_CE2} / T_{ISCKC_CE2}^{(2)}$ | CE pin Setup/Hold with respect to CLKDIV (for CE2) | 0.01/ 0.27 | 0.01/ 0.29 | 0.01/ 0.31 | 0.01/ 0.31 | -0.05/ 0.35 | ns |
| Setup/Hold for Data Lines | | | | | | | |
| $T_{ISDCK_D} / T_{ISCKD_D}$ | D pin Setup/Hold with respect to CLK | 0.07/ 0.08 | 0.08/ 0.09 | 0.09/ 0.11 | 0.09/ 0.11 | 0.11/ 0.19 | ns |
| $T_{ISDCK_DDLY} / T_{ISCKD_DDLY}$ | DDLY pin Setup/Hold with respect to CLK (using IODELAY) ⁽¹⁾ | 0.10/ 0.05 | 0.12/ 0.06 | 0.14/ 0.07 | 0.14/ 0.07 | 0.16/ 0.15 | ns |
| $T_{ISDCK_D_DDR} / T_{ISCKD_D_DDR}$ | D pin Setup/Hold with respect to CLK at DDR mode | 0.07/ 0.08 | 0.08/ 0.09 | 0.09/ 0.11 | 0.09/ 0.11 | 0.11/ 0.19 | ns |
| $T_{ISDCK_DDLY_DDR} / T_{ISCKD_DDLY_DDR}$ | D pin Setup/Hold with respect to CLK at DDR mode (using IODELAY) ⁽¹⁾ | 0.10/ 0.05 | 0.12/ 0.06 | 0.14/ 0.07 | 0.14/ 0.07 | 0.16/ 0.15 | ns |
| Sequential Delays | | | | | | | |
| T_{ISCKO_Q} | CLKDIV to out at Q pin | 0.57 | 0.66 | 0.75 | 0.80 | 0.88 | ns |
| Propagation Delays | | | | | | | |
| T_{ISDO_DO} | D input to DO output pin | 0.19 | 0.22 | 0.25 | 0.25 | 0.28 | ns |

Notes:

- Recorded at 0 tap value.
- T_{ISCK_CE2} and T_{ISCKC_CE2} are reported as $T_{ISCK_CE} / T_{ISCKC_CE}$ in TRACE report.

Output Serializer/Deserializer Switching Characteristics

Table 52: OSERDES Switching Characteristics

| Symbol | Description | Speed Grade | | | | | Units |
|-------------------------------------|---|----------------|----------------|----------------|----------------|----------------|-------|
| | | -3 | -2 | -1 (XC) | -1 (XQ) | -1L | |
| Setup/Hold | | | | | | | |
| T_{OSDCK_D}/T_{OSCKD_D} | D input Setup/Hold with respect to CLKDIV | 0.23/ -0.10 | 0.28/ -0.10 | 0.31/ -0.10 | 0.35/ -0.10 | 0.36/ -0.15 | ns |
| $T_{OSDCK_T}/T_{OSCKD_T}^{(1)}$ | T input Setup/Hold with respect to CLK | 0.44/ -0.10 | 0.51/ -0.09 | 0.56/ -0.08 | 0.60/ -0.08 | 0.68/ -0.15 | ns |
| $T_{OSDCK_T2}/T_{OSCKD_T2}^{(1)}$ | T input Setup/Hold with respect to CLKDIV | 0.25/ -0.10 | 0.27/ -0.09 | 0.31/ -0.08 | 0.31/ -0.08 | 0.47/ -0.15 | ns |
| $T_{OSCKK_OCE}/T_{OSCKC_OCE}$ | OCE input Setup/Hold with respect to CLK | 0.17/ -0.03 | 0.20/ -0.03 | 0.22/ -0.03 | 0.27/ -0.03 | 0.27/ -0.04 | ns |
| T_{OSCKK_S} | SR (Reset) input Setup with respect to CLKDIV | 0.07 | 0.07 | 0.07 | 0.07 | 0.08 | ns |
| $T_{OSCKK_TCE}/T_{OSCKC_TCE}$ | TCE input Setup/Hold with respect to CLK | 0.15/ -0.04 | 0.19/ -0.04 | 0.21/ -0.04 | 0.27/ -0.04 | 0.29/ -0.05 | ns |
| Sequential Delays | | | | | | | |
| T_{OSCKO_OQ} | Clock to out from CLK to OQ | 0.63 | 0.71 | 0.82 | 0.82 | 0.93 | ns |
| T_{OSCKO_TQ} | Clock to out from CLK to TQ | 0.63 | 0.71 | 0.82 | 0.82 | 0.93 | ns |
| Combinatorial | | | | | | | |
| T_{OSDO_TQ} | T input to TQ Out | 0.76 | 0.84 | 0.97 | 0.97 | 1.11 | ns |

Notes:

- T_{OSDCK_T2} and T_{OSCKD_T2} are reported as T_{OSDCK_T}/T_{OSCKD_T} in TRACE report.

Input/Output Delay Switching Characteristics

Table 53: Input/Output Delay Switching Characteristics

| Symbol | Description | Speed Grade | | | | Units |
|---|--|--------------------------------|----------------|----------------|----------------|------------|
| | | -3 | -2 | -1 | -1L | |
| IDELAYCTRL | | | | | | |
| T _{DLYCCO_RDY} | Reset to Ready for IDELAYCTRL | 3.00 | 3.00 | 3.00 | 3.25 | µs |
| F _{IDELAYCTRL_REF} | REFCLK frequency = 200.0 ⁽¹⁾ | 200 | 200 | 200 | 200 | MHz |
| | REFCLK frequency = 300.0 ⁽¹⁾ | 300 | 300 | – | – | MHz |
| IDELAYCTRL_REF_PRECISION | REFCLK precision | ±10 | ±10 | ±10 | ±10 | MHz |
| T _{IDELAYCTRL_RPW} | Minimum Reset pulse width | 50.00 | 50.00 | 50.00 | 52.50 | ns |
| IODELAY | | | | | | |
| T _{IDELAYRESOLUTION} | IODELAY Chain Delay Resolution | 1/(32 x 2 x F _{REF}) | | | | ps |
| T _{IDELAYPAT_JIT} | Pattern dependent period jitter in delay chain for clock pattern. ⁽²⁾ | 0 | 0 | 0 | 0 | ps per tap |
| | Pattern dependent period jitter in delay chain for random data pattern (PRBS 23). ⁽³⁾ | ±5 | ±5 | ±5 | ±5 | ps per tap |
| | Pattern dependent period jitter in delay chain for random data pattern (PRBS 23). ⁽⁴⁾ | ±9 | ±9 | ±9 | ±9 | ps per tap |
| T _{IODELAY_CLK_MAX} | Maximum frequency of CLK input to IODELAY | 500.00 | 420.00 | 300.00 | 300.00 | MHz |
| T _{IODCKC_CE} / T _{IODCKC_CE} | CE pin Setup/Hold with respect to CK | 0.45/ –0.09 | 0.53/ –0.09 | 0.65/ –0.09 | 0.84/ –0.14 | ns |
| T _{IODCK_INC} / T _{IODCKC_INC} | INC pin Setup/Hold with respect to CK | 0.23/ –0.02 | 0.27/ –0.01 | 0.31/ 0.00 | 0.27/ –0.04 | ns |
| T _{IODCKC_RST} / T _{IODCKC_RST} | RST pin Setup/Hold with respect to CK | 0.57/ –0.08 | 0.62/ –0.08 | 0.69/ –0.08 | 0.74/ –0.13 | ns |
| T _{IODDO_T} | TSCONTROL delay to MUXE/MUXF switching and through IODELAY | Note 5 | Note 5 | Note 5 | Note 5 | ps |
| T _{IODDO_IDATAIN} | Propagation delay through IODELAY | Note 5 | Note 5 | Note 5 | Note 5 | ps |
| T _{IODDO_ODATAIN} | Propagation delay through IODELAY | Note 5 | Note 5 | Note 5 | Note 5 | ps |

Notes:

1. Average Tap Delay at 200 MHz = 78 ps, at 300 MHz = 52 ps.
2. When HIGH_PERFORMANCE mode is set to TRUE or FALSE.
3. When HIGH_PERFORMANCE mode is set to TRUE
4. When HIGH_PERFORMANCE mode is set to FALSE.
5. Delay depends on IODELAY tap setting. See TRACE report for actual values.

CLB Switching Characteristics

Table 54: CLB Switching Characteristics

| Symbol | Description | Speed Grade | | | | Units |
|-----------------------------|----------------------------------|-------------|------|------|------|---------|
| | | -3 | -2 | -1 | -1L | |
| Combinatorial Delays | | | | | | |
| T _{ILO} | An – Dn LUT address to A | 0.06 | 0.07 | 0.07 | 0.09 | ns, Max |
| | An – Dn LUT address to AMUX/CMUX | 0.18 | 0.20 | 0.22 | 0.25 | ns, Max |
| | An – Dn LUT address to BMUX_A | 0.28 | 0.31 | 0.36 | 0.40 | ns, Max |

Table 54: CLB Switching Characteristics (Cont'd)

| Symbol | Description | Speed Grade | | | | Units |
|--|---|-------------|------------|------------|------------|---------|
| | | -3 | -2 | -1 | -1L | |
| T _{ITO} | An – Dn inputs to A – D Q outputs | 0.59 | 0.67 | 0.79 | 0.85 | ns, Max |
| T _{AXA} | AX inputs to AMUX output | 0.31 | 0.35 | 0.42 | 0.44 | ns, Max |
| T _{AXB} | AX inputs to BMUX output | 0.35 | 0.39 | 0.47 | 0.50 | ns, Max |
| T _{AXC} | AX inputs to CMUX output | 0.39 | 0.44 | 0.52 | 0.56 | ns, Max |
| T _{AXD} | AX inputs to DMUX output | 0.42 | 0.47 | 0.55 | 0.60 | ns, Max |
| T _{BXB} | BX inputs to BMUX output | 0.30 | 0.34 | 0.39 | 0.44 | ns, Max |
| T _{BXD} | BX inputs to DMUX output | 0.38 | 0.43 | 0.50 | 0.55 | ns, Max |
| T _{CXC} | CX inputs to CMUX output | 0.26 | 0.29 | 0.34 | 0.37 | ns, Max |
| T _{CXD} | CX inputs to DMUX output | 0.30 | 0.34 | 0.40 | 0.44 | ns, Max |
| T _{DXD} | DX inputs to DMUX output | 0.30 | 0.33 | 0.38 | 0.43 | ns, Max |
| T _{OPCYA} | An input to COUT output | 0.32 | 0.36 | 0.41 | 0.47 | ns, Max |
| T _{OPCYB} | Bn input to COUT output | 0.32 | 0.36 | 0.41 | 0.47 | ns, Max |
| T _{OPCYC} | Cn input to COUT output | 0.27 | 0.30 | 0.34 | 0.40 | ns, Max |
| T _{OPCYD} | Dn input to COUT output | 0.25 | 0.28 | 0.32 | 0.37 | ns, Max |
| T _{AXCY} | AX input to COUT output | 0.25 | 0.28 | 0.33 | 0.36 | ns, Max |
| T _{BXCY} | BX input to COUT output | 0.22 | 0.24 | 0.28 | 0.31 | ns, Max |
| T _{CXCY} | CX input to COUT output | 0.15 | 0.17 | 0.20 | 0.22 | ns, Max |
| T _{DXCY} | DX input to COUT output | 0.14 | 0.16 | 0.19 | 0.21 | ns, Max |
| T _{BYP} | CIN input to COUT output | 0.06 | 0.07 | 0.08 | 0.09 | ns, Max |
| T _{CINA} | CIN input to AMUX output | 0.21 | 0.24 | 0.28 | 0.30 | ns, Max |
| T _{CINB} | CIN input to BMUX output | 0.23 | 0.25 | 0.29 | 0.31 | ns, Max |
| T _{CINC} | CIN input to CMUX output | 0.23 | 0.26 | 0.30 | 0.33 | ns, Max |
| T _{CIND} | CIN input to DMUX output | 0.25 | 0.29 | 0.33 | 0.36 | ns, Max |
| Sequential Delays | | | | | | |
| T _{CKO} | Clock to AQ – DQ outputs | 0.29 | 0.33 | 0.39 | 0.44 | ns, Max |
| T _{SHCKO} | Clock to AMUX – DMUX outputs | 0.36 | 0.40 | 0.47 | 0.53 | ns, Max |
| Setup and Hold Times of CLB Flip-Flops Before/After Clock CLK | | | | | | |
| T _{DICK} /T _{CKDI} | A – D input to CLK on A – D Flip Flops | 0.30/0.17 | 0.36/0.18 | 0.43/0.20 | 0.44/0.25 | ns, Min |
| T _{CECK_CLB} / T _{CKCE_CLB} | CE input to CLK on A – D Flip Flops | 0.20/0.00 | 0.25/0.00 | 0.32/0.00 | 0.32/0.01 | ns, Min |
| T _{SRCK} /T _{CKSR} | SR input to CLK on A – D Flip Flops | 0.39/–0.07 | 0.44/–0.07 | 0.52/–0.07 | 0.58/–0.08 | ns, Min |
| T _{CINCK} /T _{CKCIN} | CIN input to CLK on A – D Flip Flops | 0.16/0.12 | 0.19/0.14 | 0.24/0.16 | 0.23/0.22 | ns, Min |
| Set/Reset | | | | | | |
| T _{SRMIN} | SR input minimum pulse width | 0.90 | 0.90 | 0.97 | 0.80 | ns, Min |
| T _{RQ} | Delay from SR input to AQ – DQ flip-flops | 0.52 | 0.58 | 0.68 | 0.77 | ns, Max |
| T _{CEO} | Delay from CE input to AQ – DQ flip-flops | 0.41 | 0.48 | 0.59 | 0.61 | ns, Max |
| F _{TOG} | Toggle frequency (for export control) | 1412.00 | 1286.40 | 1098.00 | 1098.00 | MHz |

Notes:

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.
2. These items are of interest for Carry Chain applications.

CLB Distributed RAM Switching Characteristics (SLICEM Only)

Table 55: CLB Distributed RAM Switching Characteristics

| Symbol | Description | Speed Grade | | | | Units |
|--|------------------------------|-------------|------------|------------|------------|---------|
| | | -3 | -2 | -1 | -1L | |
| Sequential Delays | | | | | | |
| T_{SHCKO} | Clock to A – B outputs | 0.92 | 1.10 | 1.36 | 1.49 | ns, Max |
| T_{SHCKO_1} | Clock to AMUX – BMUX outputs | 1.19 | 1.40 | 1.71 | 1.87 | ns, Max |
| Setup and Hold Times Before/After Clock CLK | | | | | | |
| T_{DS}/T_{DH} | A – D inputs to CLK | 0.62/0.18 | 0.72/0.20 | 0.88/0.22 | 0.98/0.23 | ns, Min |
| T_{AS}/T_{AH} | Address An inputs to clock | 0.19/0.52 | 0.22/0.59 | 0.27/0.66 | 0.30/0.75 | ns, Min |
| T_{WS}/T_{WH} | WE input to clock | 0.27/0.00 | 0.32/0.00 | 0.40/0.00 | 0.47/–0.03 | ns, Min |
| T_{CECK}/T_{CKCE} | CE input to CLK | 0.28/–0.01 | 0.34/–0.01 | 0.41/–0.01 | 0.48/–0.05 | ns, Min |
| Clock CLK | | | | | | |
| T_{MPW} | Minimum pulse width | 0.70 | 0.82 | 1.00 | 1.04 | ns, Min |
| T_{MCP} | Minimum clock period | 1.40 | 1.64 | 2.00 | 2.08 | ns, Min |

Notes:

1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values cannot be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.
2. T_{SHCKO} also represents the CLK to XMUX output. Refer to TRACE report for the CLK to XMUX path.

CLB Shift Register Switching Characteristics (SLICEM Only)

Table 56: CLB Shift Register Switching Characteristics

| Symbol | Description | Speed Grade | | | | Units |
|--|-------------------------------------|-------------|------------|------------|-----------|---------|
| | | -3 | -2 | -1 | -1L | |
| Sequential Delays | | | | | | |
| T_{REG} | Clock to A – D outputs | 1.11 | 1.30 | 1.58 | 1.74 | ns, Max |
| T_{REG_MUX} | Clock to AMUX – DMUX output | 1.37 | 1.60 | 1.93 | 2.12 | ns, Max |
| T_{REG_M31} | Clock to DMUX output via M31 output | 1.08 | 1.27 | 1.55 | 1.74 | ns, Max |
| Setup and Hold Times Before/After Clock CLK | | | | | | |
| T_{WS}/T_{WH} | WE input | 0.05/0.00 | 0.07/0.00 | 0.09/0.00 | 0.11/0.03 | ns, Min |
| T_{CECK}/T_{CKCE} | CE input to CLK | 0.06/–0.01 | 0.08/–0.01 | 0.10/–0.01 | 0.12/0.02 | ns, Min |
| T_{DS}/T_{DH} | A – D inputs to CLK | 0.64/0.18 | 0.76/0.21 | 0.94/0.24 | 1.07/0.23 | ns, Min |
| Clock CLK | | | | | | |
| T_{MPW} | Minimum pulse width | 0.60 | 0.70 | 0.85 | 0.89 | ns, Min |

Notes:

1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values cannot be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

Block RAM and FIFO Switching Characteristics

Table 57: Block RAM and FIFO Switching Characteristics

| Symbol | Description | Speed Grade | | | | Units |
|--|--|---------------|---------------|---------------|---------------|---------|
| | | -3 | -2 | -1 | -1L | |
| Block RAM and FIFO Clock-to-Out Delays | | | | | | |
| T_{RCKO_DO} and $T_{RCKO_DO_REG}$ ⁽¹⁾ | Clock CLK to DOUT output (without output register) ⁽²⁾⁽³⁾ | 1.60 | 1.79 | 2.08 | 2.36 | ns, Max |
| | Clock CLK to DOUT output (with output register) ⁽⁴⁾⁽⁵⁾ | 0.60 | 0.66 | 0.75 | 0.83 | ns, Max |
| $T_{RCKO_DO_ECC}$ and $T_{RCKO_DO_ECC_REG}$ | Clock CLK to DOUT output with ECC (without output register) ⁽²⁾⁽³⁾ | 2.62 | 2.89 | 3.30 | 3.73 | ns, Max |
| | Clock CLK to DOUT output with ECC (with output register) ⁽⁴⁾⁽⁵⁾ | 0.71 | 0.77 | 0.86 | 0.94 | ns, Max |
| T_{RCKO_CASC} and $T_{RCKO_CASC_REG}$ | Clock CLK to DOUT output with Cascade (without output register) ⁽²⁾ | 2.49 | 2.77 | 3.18 | 3.61 | ns, Max |
| | Clock CLK to DOUT output with Cascade (with output register) ⁽⁴⁾ | 1.29 | 1.41 | 1.58 | 1.79 | ns, Max |
| T_{RCKO_FLAGS} | Clock CLK to FIFO flags outputs ⁽⁶⁾ | 0.74 | 0.81 | 0.91 | 0.98 | ns, Max |
| $T_{RCKO_POINTERS}$ | Clock CLK to FIFO pointers outputs ⁽⁷⁾ | 0.90 | 0.98 | 1.09 | 1.21 | ns, Max |
| $T_{RCKO_SDBIT_ECC}$ and $T_{RCKO_SDBIT_ECC_REG}$ | Clock CLK to BITERR (with output register) | 0.62 | 0.68 | 0.76 | 0.82 | ns, Max |
| | Clock CLK to BITERR (without output register) | 2.21 | 2.46 | 2.84 | 3.23 | ns, Max |
| $T_{RCKO_PARITY_ECC}$ | Clock CLK to ECCPARITY in ECC encode only mode | 0.86 | 0.94 | 1.06 | 1.18 | ns, Max |
| $T_{RCKO_RDADDR_ECC}$ and $T_{RCKO_RDADDR_ECC_REG}$ | Clock CLK to RDADDR output with ECC (without output register) | 0.73 | 0.79 | 0.90 | 1.00 | ns, Max |
| | Clock CLK to RDADDR output with ECC (with output register) | 0.76 | 0.82 | 0.92 | 1.02 | ns, Max |
| Setup and Hold Times Before/After Clock CLK | | | | | | |
| $T_{RCKK_ADDR}/T_{RCKC_ADDR}$ | ADDR inputs ⁽⁸⁾ | 0.47/ 0.27 | 0.53/ 0.29 | 0.62/ 0.32 | 0.66/ 0.34 | ns, Min |
| T_{RDCK_DI}/T_{RCKD_DI} | DIN inputs ⁽⁹⁾ | 0.84/ 0.30 | 0.95/ 0.32 | 1.11/ 0.34 | 1.26/ 0.36 | ns, Min |
| $T_{RDCK_DI_ECC}/T_{RCKD_DI_ECC}$ | DIN inputs with block RAM ECC in standard mode ⁽⁹⁾ | 0.47/ 0.30 | 0.52/ 0.32 | 0.59/ 0.34 | 0.68/ 0.36 | ns, Min |
| | DIN inputs with block RAM ECC encode only ⁽⁹⁾ | 0.68/ 0.30 | 0.75/ 0.32 | 0.85/ 0.34 | 0.97/ 0.36 | ns, Min |
| | DIN inputs with FIFO ECC in standard mode ⁽⁹⁾ | 0.77/ 0.30 | 0.87/ 0.32 | 1.02/ 0.34 | 1.16/ 0.36 | ns, Min |
| $T_{RCKK_CLK}/T_{RCKC_CLK}$ | Inject single/double bit error in ECC mode | 0.90/ 0.27 | 1.02/ 0.28 | 1.20/ 0.29 | 1.56/ 0.29 | ns, Min |
| $T_{RCKK_RDEN}/T_{RCKC_RDEN}$ | Block RAM Enable (EN) input | 0.31/ 0.26 | 0.35/ 0.27 | 0.41/ 0.30 | 0.44/ 0.31 | ns, Min |
| $T_{RCKK_REGCE}/T_{RCKC_REGCE}$ | CE input of output register | 0.18/ 0.25 | 0.19/ 0.27 | 0.22/ 0.31 | 0.24/ 0.33 | ns, Min |
| $T_{RCKK_RSTREG}/T_{RCKC_RSTREG}$ | Synchronous RSTREG input | 0.22/ 0.23 | 0.24/ 0.24 | 0.28/ 0.26 | 0.31/ 0.27 | ns, Min |
| $T_{RCKK_RSTRAM}/T_{RCKC_RSTRAM}$ | Synchronous RSTRAM input | 0.32/ 0.23 | 0.36/ 0.24 | 0.41/ 0.27 | 0.46/ 0.29 | ns, Min |

Table 57: Block RAM and FIFO Switching Characteristics (Cont'd)

| Symbol | Description | Speed Grade | | | | Units |
|-------------------------------------|--|---------------|---------------|---------------|---------------|---------|
| | | -3 | -2 | -1 | -1L | |
| T_{RCKK_WE}/T_{RCKC_WE} | Write Enable (WE) input (Block RAM only) | 0.44/ 0.19 | 0.47/ 0.25 | 0.52/ 0.35 | 0.67/ 0.24 | ns, Min |
| $T_{RCKK_WREN}/T_{RCKC_WREN}$ | WREN FIFO inputs | 0.47/ 0.26 | 0.50/ 0.27 | 0.55/ 0.30 | 0.68/ 0.31 | ns, Min |
| $T_{RCKK_RDEN}/T_{RCKC_RDEN}$ | RDEN FIFO inputs | 0.46/ 0.26 | 0.50/ 0.27 | 0.55/ 0.30 | 0.67/ 0.31 | ns, Min |
| Reset Delays | | | | | | |
| T_{RCO_FLAGS} | Reset RST to FIFO Flags/Pointers ⁽¹⁰⁾ | 0.90 | 0.98 | 1.10 | 1.23 | ns, Max |
| $T_{RCKK_RSTREG}/T_{RCKC_RSTREG}$ | FIFO reset timing ⁽¹¹⁾ | 0.22/ 0.23 | 0.24/ 0.24 | 0.28/ 0.26 | 0.31/ 0.27 | ns, Min |
| Maximum Frequency | | | | | | |
| F_{MAX} | Block RAM in TDP and SDP modes (Write First and No Change modes) | 600 | 540 | 450 | 340 | MHz |
| | Block RAM (Read First mode) | 525 | 475 | 400 | 275 | MHz |
| | Block RAM (SDP mode) ⁽¹²⁾ | 525 | 475 | 400 | 275 | MHz |
| $F_{MAX_CASCADE}$ | Block RAM Cascade (Write First and No Change modes) | 550 | 490 | 400 | 300 | MHz |
| | Block RAM Cascade (Read First mode) | 475 | 425 | 350 | 235 | MHz |
| F_{MAX_FIFO} | FIFO in all modes | 600 | 540 | 450 | 340 | MHz |
| F_{MAX_ECC} | Block RAM and FIFO in ECC configuration | 450 | 400 | 325 | 250 | MHz |

Notes:

- TRACE will report all of these parameters as T_{RCKO_DO} .
- T_{RCKO_DOR} includes T_{RCKO_DOW} , T_{RCKO_DOPR} , and T_{RCKO_DOPW} as well as the B port equivalent timing parameters.
- These parameters also apply to synchronous FIFO with $DO_REG = 0$.
- T_{RCKO_DO} includes T_{RCKO_DOP} as well as the B port equivalent timing parameters.
- These parameters also apply to multirate (asynchronous) and synchronous FIFO with $DO_REG = 1$.
- T_{RCKO_FLAGS} includes the following parameters: T_{RCKO_AEMPTY} , T_{RCKO_AFULL} , T_{RCKO_EMPTY} , T_{RCKO_FULL} , T_{RCKO_RDERR} , T_{RCKO_WRERR} .
- $T_{RCKO_POINTERS}$ includes both $T_{RCKO_RDCOUNT}$ and $T_{RCKO_WRCOUNT}$.
- The ADDR setup and hold must be met when EN is asserted (even when WE is deasserted). Otherwise, block RAM data corruption is possible.
- T_{RCKO_DI} includes both A and B inputs as well as the parity inputs of A and B.
- T_{RCO_FLAGS} includes the following flags: AEMPTY, AFULL, EMPTY, FULL, RDERR, WRERR, RDCOUNT, and WRCOUNT.
- The FIFO reset must be asserted for at least three positive clock edges.
- When using ISE software v12.4 or later, if the RDADDR_COLLISION_HWCONFIG attribute is set to PERFORMANCE or the block RAM is in single-port operation, then the faster F_{MAX} for WRITE_FIRST/NO_CHANGE modes apply.

DSP48E1 Switching Characteristics

Table 58: DSP48E1 Switching Characteristics

| Symbol | Description | Speed Grade | | | | | Units |
|---|---|----------------|----------------|----------------|----------------|----------------|-------|
| | | -3 | -2 | -1 (XC) | -1 (XQ) | -1L | |
| Setup and Hold Times of Data/Control Pins to the Input Register Clock | | | | | | | |
| $T_{\text{DSPDCK}}\{A, ACIN; B, BCIN\}_{\text{AREG}; \text{BREG}} / T_{\text{DSPCKD}}\{A, ACIN; B, BCIN\}_{\text{AREG}; \text{BREG}}$ | {A, ACIN, B, BCIN} input to {A, B} register CLK | 0.25/ 0.27 | 0.29/ 0.30 | 0.35/ 0.34 | 0.36/ 0.34 | 0.46/ 0.39 | ns |
| $T_{\text{DSPDCK_C_CREG}} / T_{\text{DSPCKD_C_CREG}}$ | C input to C register CLK | 0.16/ 0.20 | 0.19/ 0.22 | 0.22/ 0.24 | 0.25/ 0.24 | 0.33/ 0.30 | ns |
| $T_{\text{DSPDCK_D_DREG}} / T_{\text{DSPCKD_D_DREG}}$ | D input to D register CLK | 0.07/ 0.31 | 0.10/ 0.34 | 0.15/ 0.39 | 0.16/ 0.39 | 0.24/ 0.45 | ns |
| Setup and Hold Times of Data Pins to the Pipeline Register Clock | | | | | | | |
| $T_{\text{DSPDCK}}\{A, ACIN, B, BCIN\}_{\text{MREG_MULT}} / T_{\text{DSPCKD}}\{A, ACIN, B, BCIN\}_{\text{MREG_MULT}}$ | {A, ACIN, B, BCIN} input to M register CLK | 2.36/ 0.04 | 2.70/ 0.04 | 3.21/ 0.04 | 3.21/ 0.04 | 3.66/ 0.02 | ns |
| $T_{\text{DSPDCK}}\{A, D\}_{\text{ADREG}} / T_{\text{DSPCKD}}\{A, D\}_{\text{ADREG}}$ | {A, D} input to AD register CLK | 1.24/ 0.10 | 1.42/ 0.12 | 1.69/ 0.13 | 1.69/ 0.13 | 1.91/ 0.16 | ns |
| Setup and Hold Times of Data/Control Pins to the Output Register Clock | | | | | | | |
| $T_{\text{DSPDCK}}\{A, ACIN, B, BCIN\}_{\text{PREG_MULT}} / T_{\text{DSPCKD}}\{A, ACIN, B, BCIN\}_{\text{PREG_MULT}}$ | {A, ACIN, B, BCIN} input to P register CLK using multiplier | 3.83/ -0.13 | 4.37/ -0.13 | 5.20/ -0.13 | 5.20/ -0.13 | 5.94/ -0.24 | ns |
| $T_{\text{DSPDCK_D_PREG_MULT}} / T_{\text{DSPCKD_D_PREG_MULT}}$ | D input to P register CLK | 3.62/ -0.47 | 4.13/ -0.47 | 4.90/ -0.47 | 4.90/ -0.47 | 5.61/ -0.77 | ns |
| $T_{\text{DSPDCK}}\{A, ACIN, B, BCIN\}_{\text{PREG}} / T_{\text{DSPCKD}}\{A, ACIN, B, BCIN\}_{\text{PREG}}$ | {A, ACIN, B, BCIN} input to P register CLK not using multiplier | 1.59/ -0.13 | 1.81/ -0.13 | 2.15/ -0.13 | 2.15/ -0.13 | 2.44/ -0.24 | ns |
| $T_{\text{DSPDCK_C_PREG}} / T_{\text{DSPCKD_C_PREG}}$ | C input to P register CLK | 1.42/ -0.10 | 1.61/ -0.10 | 1.91/ -0.10 | 1.91/ -0.10 | 2.16/ -0.19 | ns |
| $T_{\text{DSPDCK}}\{\text{PCIN}, \text{CARRYCASCIN}, \text{MULTSIGNIN}\}_{\text{PREG}} / T_{\text{DSPCKD}}\{\text{PCIN}, \text{CARRYCASCIN}, \text{MULTSIGNIN}\}_{\text{PREG}}$ | {PCIN, CARRYCASCIN, MULTSIGNIN} input to P register CLK | 1.23/ -0.02 | 1.41/ -0.02 | 1.67/ -0.02 | 1.67/ -0.02 | 1.91/ -0.07 | ns |
| Setup and Hold Times of the CE Pins | | | | | | | |
| $T_{\text{DSPDCK}}\{\text{CEA}; \text{CEB}\}_{\text{AREG}; \text{BREG}} / T_{\text{DSPCKD}}\{\text{CEA}; \text{CEB}\}_{\text{AREG}; \text{BREG}}$ | {CEA; CEB} input to {A; B} register CLK | 0.14/ 0.19 | 0.17/ 0.22 | 0.22/ 0.25 | 0.22/ 0.25 | 0.30/ 0.28 | ns |
| $T_{\text{DSPDCK_CEC_CREG}} / T_{\text{DSPCKD_CEC_CREG}}$ | CEC input to C register CLK | 0.15/ 0.18 | 0.18/ 0.20 | 0.24/ 0.23 | 0.24/ 0.23 | 0.31/ 0.26 | ns |
| $T_{\text{DSPDCK_CED_DREG}} / T_{\text{DSPCKD_CED_DREG}}$ | CED input to D register CLK | 0.20/ 0.12 | 0.24/ 0.13 | 0.31/ 0.14 | 0.31/ 0.14 | 0.43/ 0.16 | ns |
| $T_{\text{DSPDCK_CEM_MREG}} / T_{\text{DSPCKD_CEM_MREG}}$ | CEM input to M register CLK | 0.16/ 0.19 | 0.20/ 0.21 | 0.26/ 0.25 | 0.26/ 0.25 | 0.32/ 0.28 | ns |
| $T_{\text{DSPDCK_CEP_PREG}} / T_{\text{DSPCKD_CEP_PREG}}$ | CEP input to P register CLK | 0.32/ 0.02 | 0.38/ 0.02 | 0.46/ 0.03 | 0.46/ 0.03 | 0.54/ 0.04 | ns |
| Setup and Hold Times of the RST Pins | | | | | | | |
| $T_{\text{DSPDCK}}\{\text{RSTA}; \text{RSTB}\}_{\text{AREG}; \text{BREG}} / T_{\text{DSPCKD}}\{\text{RSTA}; \text{RSTB}\}_{\text{AREG}; \text{BREG}}$ | {RSTA, RSTB} input to {A, B} register CLK | 0.27/ 0.17 | 0.31/ 0.19 | 0.38/ 0.22 | 0.38/ 0.22 | 0.41/ 0.25 | ns |
| $T_{\text{DSPDCK_RSTC_CREG}} / T_{\text{DSPCKD_RSTC_CREG}}$ | RSTC input to C register CLK | 0.18/ 0.08 | 0.20/ 0.08 | 0.23/ 0.09 | 0.23/ 0.09 | 0.27/ 0.11 | ns |
| $T_{\text{DSPDCK_RSTD_DREG}} / T_{\text{DSPCKD_RSTD_DREG}}$ | RSTD input to D register CLK | 0.28/ 0.15 | 0.32/ 0.16 | 0.38/ 0.19 | 0.38/ 0.19 | 0.45/ 0.21 | ns |
| $T_{\text{DSPDCK_RSTM_MREG}} / T_{\text{DSPCKD_RSTM_MREG}}$ | RSTM input to M register CLK | 0.20/ 0.24 | 0.23/ 0.26 | 0.26/ 0.30 | 0.26/ 0.30 | 0.29/ 0.34 | ns |

Table 58: DSP48E1 Switching Characteristics (Cont'd)

| Symbol | Description | Speed Grade | | | | | Units |
|--|--|---------------|---------------|---------------|---------------|---------------|-------|
| | | -3 | -2 | -1 (XC) | -1 (XQ) | -1L | |
| $T_{\text{DSPDCK_RSTP_PREG}} / T_{\text{DSPCKD_RSTP_PREG}}$ | RSTP input to P register CLK | 0.26/ 0.04 | 0.30/ 0.04 | 0.35/ 0.05 | 0.35/ 0.05 | 0.43/ 0.06 | ns |
| Combinatorial Delays from Input Pins to Output Pins | | | | | | | |
| $T_{\text{DSPDO_}\{A, B\}_{\{P, \text{CARRYOUT}\}}_{\text{MULT}}}$ | {A, B} input to {P, CARRYOUT} output using multiplier | 3.76 | 4.29 | 5.08 | 5.08 | 5.87 | ns |
| $T_{\text{DSPDO_D_}\{P, \text{CARRYOUT}\}}_{\text{MULT}}$ | D input to {P, CARRYOUT} output using multiplier | 3.57 | 4.07 | 4.82 | 4.82 | 5.57 | ns |
| $T_{\text{DSPDO_}\{A, B\}_{\{P, \text{CARRYOUT}\}}}$ | {A, B} input to {P, CARRYOUT} output not using multiplier | 1.55 | 1.76 | 2.07 | 2.07 | 2.41 | ns |
| $T_{\text{DSPDO_}\{C, \text{CARRYIN}\}_{\{P, \text{CARRYOUT}\}}}$ | {C, CARRYIN} input to {P, CARRYOUT} output | 1.38 | 1.56 | 1.83 | 1.83 | 2.13 | ns |
| Combinatorial Delays from Input Pins to Cascading Output Pins | | | | | | | |
| $T_{\text{DSPDO_}\{A, B\}_{\{\text{ACOUT}; \text{BCOUT}\}}}$ | {A, B} input to {ACOUT, BCOUT} output | 0.49 | 0.56 | 0.65 | 0.65 | 0.73 | ns |
| $T_{\text{DSPDO_}\{A, B\}_{\{\text{PCOUT}, \text{CARRYCASCOUT}, \text{MULTSIGNOUT}\}}_{\text{MULT}}}$ | {A, B} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier | 3.87 | 4.42 | 5.24 | 5.24 | 6.09 | ns |
| $T_{\text{DSPDO_D_}\{\text{PCOUT}, \text{CARRYCASCOUT}, \text{MULTSIGNOUT}\}}_{\text{MULT}}$ | D input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier | 3.66 | 4.17 | 4.94 | 4.94 | 5.76 | ns |
| $T_{\text{DSPDO_}\{A, B\}_{\{\text{PCOUT}, \text{CARRYCASCOUT}, \text{MULTSIGNOUT}\}}}$ | {A, B} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output not using multiplier | 1.64 | 1.86 | 2.19 | 2.19 | 2.60 | ns |
| $T_{\text{DSPDO_}\{C, \text{CARRYIN}\}_{\{\text{PCOUT}, \text{CARRYCASCOUT}, \text{MULTSIGNOUT}\}}}$ | {C, CARRYIN} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output | 1.46 | 1.66 | 1.95 | 1.95 | 2.32 | ns |
| Combinatorial Delays from Cascading Input Pins to All Output Pins | | | | | | | |
| $T_{\text{DSPDO_}\{\text{ACIN}, \text{BCIN}\}_{\{P, \text{CARRYOUT}\}}_{\text{MULT}}}$ | {ACIN, BCIN} input to {P, CARRYOUT} output using multiplier | 3.67 | 4.19 | 4.97 | 4.97 | 5.75 | ns |
| $T_{\text{DSPDO_}\{\text{ACIN}, \text{BCIN}\}_{\{P, \text{CARRYOUT}\}}}$ | {ACIN, BCIN} input to {P, CARRYOUT} output not using multiplier | 1.43 | 1.63 | 1.92 | 1.92 | 2.25 | ns |
| $T_{\text{DSPDO_}\{\text{ACIN}; \text{BCIN}\}_{\{\text{ACOUT}; \text{BCOUT}\}}}$ | {ACIN, BCIN} input to {ACOUT, BCOUT} output | 0.36 | 0.42 | 0.49 | 0.49 | 0.56 | ns |
| $T_{\text{DSPDO_}\{\text{ACIN}, \text{BCIN}\}_{\{\text{PCOUT}, \text{CARRYCASCOUT}, \text{MULTSIGNOUT}\}}_{\text{MULT}}}$ | {ACIN, BCIN} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier | 3.76 | 4.29 | 5.10 | 5.10 | 5.94 | ns |
| $T_{\text{DSPDO_}\{\text{ACIN}, \text{BCIN}\}_{\{\text{PCOUT}, \text{CARRYCASCOUT}, \text{MULTSIGNOUT}\}}}$ | {ACIN, BCIN} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output not using multiplier | 1.52 | 1.73 | 2.05 | 2.05 | 2.44 | ns |
| $T_{\text{DSPDO_}\{\text{PCIN}, \text{CARRYCASCIN}, \text{MULTSIGNIN}\}_{\{P, \text{CARRYOUT}\}}}$ | {PCIN, CARRYCASCIN, MULTSIGNIN} input to {P, CARRYOUT} output | 1.19 | 1.35 | 1.60 | 1.60 | 1.87 | ns |

Table 58: DSP48E1 Switching Characteristics (Cont'd)

| Symbol | Description | Speed Grade | | | | | Units |
|---|---|-------------|------|---------|---------|------|-------|
| | | -3 | -2 | -1 (XC) | -1 (XQ) | -1L | |
| $T_{\text{DSPDO}}_{\{\text{PCIN}, \text{CARRYCASCIN}, \text{MULTSIGNIN}\}_{\{\text{PCOUT}, \text{CARRYCASCOU}, \text{MULTSIGNOUT}\}}$ | {PCIN, CARRYCASCIN, MULTSIGNIN} input to {PCOUT, CARRYCASCOU, MULTSIGNOUT} output | 1.28 | 1.46 | 1.72 | 1.72 | 2.06 | ns |
| Clock to Outs from Output Register Clock to Output Pins | | | | | | | |
| $T_{\text{DSPCKO}}_{\{\text{P}, \text{CARRYOUT}\}_{\text{PREG}}}$ | CLK (PREG) to {P, CARRYOUT} output | 0.38 | 0.43 | 0.50 | 0.50 | 0.57 | ns |
| $T_{\text{DSPCKO}}_{\{\text{PCOUT}, \text{CARRYCASCOU}, \text{MULTSIGNOUT}\}_{\text{PREG}}}$ | CLK (PREG) to {CARRYCASCOU, PCOUT, MULTSIGNOUT} output | 0.50 | 0.56 | 0.66 | 0.66 | 0.76 | ns |
| Clock to Outs from Pipeline Register Clock to Output Pins | | | | | | | |
| $T_{\text{DSPCKO}}_{\{\text{P}, \text{CARRYOUT}\}_{\text{MREG}}}$ | CLK (MREG) to {P, CARRYOUT} output | 1.72 | 1.96 | 2.30 | 2.30 | 2.69 | ns |
| $T_{\text{DSPCKO}}_{\{\text{PCOUT}, \text{CARRYCASCOU}, \text{MULTSIGNOUT}\}_{\text{MREG}}}$ | CLK (MREG) to {PCOUT, CARRYCASCOU, MULTSIGNOUT} output | 1.81 | 2.06 | 2.43 | 2.43 | 2.88 | ns |
| $T_{\text{DSPCKO}}_{\{\text{P}, \text{CARRYOUT}\}_{\text{ADREG_MULT}}}$ | CLK (ADREG) to {P, CARRYOUT} output | 2.79 | 3.16 | 3.72 | 3.72 | 4.32 | ns |
| $T_{\text{DSPCKO}}_{\{\text{PCOUT}, \text{CARRYCASCOU}, \text{MULTSIGNOUT}\}_{\text{ADREG_MULT}}}$ | CLK (ADREG) to {PCOUT, CARRYCASCOU, MULTSIGNOUT} output | 2.87 | 3.26 | 3.84 | 3.84 | 4.51 | ns |
| Clock to Outs from Input Register Clock to Output Pins | | | | | | | |
| $T_{\text{DSPCKO}}_{\{\text{P}, \text{CARRYOUT}\}_{\{\text{AREG}, \text{BREG}\}_{\text{MULT}}}}$ | CLK (AREG, BREG) to {P, CARRYOUT} output using multiplier | 3.97 | 4.52 | 5.36 | 5.36 | 6.20 | ns |
| $T_{\text{DSPCKO}}_{\{\text{P}, \text{CARRYOUT}\}_{\{\text{AREG}, \text{BREG}\}}}$ | CLK (AREG, BREG) to {P, CARRYOUT} output not using multiplier | 1.70 | 1.93 | 2.27 | 2.27 | 2.65 | ns |
| $T_{\text{DSPCKO}}_{\{\text{P}, \text{CARRYOUT}\}_{\text{CREG}}}$ | CLK (CREG) to {P, CARRYOUT} output | 1.70 | 1.93 | 2.27 | 2.27 | 2.80 | ns |
| $T_{\text{DSPCKO}}_{\{\text{P}, \text{CARRYOUT}\}_{\text{DREG_MULT}}}$ | CLK (DREG) to {P, CARRYOUT} output | 3.89 | 4.44 | 5.25 | 5.25 | 6.07 | ns |
| Clock to Outs from Input Register Clock to Cascading Output Pins | | | | | | | |
| $T_{\text{DSPCKO}}_{\{\text{ACOUT}; \text{BCOUT}\}_{\{\text{AREG}; \text{BREG}\}}}$ | CLK (AREG, BREG) to {P, CARRYOUT} output | 0.66 | 0.76 | 0.89 | 0.89 | 1.01 | ns |
| $T_{\text{DSPCKO}}_{\{\text{PCOUT}, \text{CARRYCASCOU}, \text{MULTSIGNOUT}\}_{\{\text{AREG}, \text{BREG}\}_{\text{MULT}}}}$ | CLK (AREG, BREG) to {PCOUT, CARRYCASCOU, MULTSIGNOUT} output using multiplier | 4.05 | 4.63 | 5.49 | 5.49 | 6.39 | ns |
| $T_{\text{DSPCKO}}_{\{\text{PCOUT}, \text{CARRYCASCOU}, \text{MULTSIGNOUT}\}_{\{\text{AREG}, \text{BREG}\}}}$ | CLK (AREG, BREG) to {PCOUT, CARRYCASCOU, MULTSIGNOUT} output not using multiplier | 1.79 | 2.03 | 2.40 | 2.40 | 2.84 | ns |
| $T_{\text{DSPCKO}}_{\{\text{PCOUT}, \text{CARRYCASCOU}, \text{MULTSIGNOUT}\}_{\text{DREG_MULT}}}$ | CLK (DREG) to {PCOUT, CARRYCASCOU, MULTSIGNOUT} output using multiplier | 3.98 | 4.54 | 5.38 | 5.38 | 6.26 | ns |
| $T_{\text{DSPCKO}}_{\{\text{PCOUT}, \text{CARRYCASCOU}, \text{MULTSIGNOUT}\}_{\text{CREG}}}$ | CLK (CREG) to {PCOUT, CARRYCASCOU, MULTSIGNOUT} output | 1.78 | 2.03 | 2.40 | 2.40 | 2.99 | ns |

Table 58: DSP48E1 Switching Characteristics (Cont'd)

| Symbol | Description | Speed Grade | | | | | Units |
|--|--|-------------|-----|---------|---------|-----|-------|
| | | -3 | -2 | -1 (XC) | -1 (XQ) | -1L | |
| Maximum Frequency | | | | | | | |
| F_{MAX} | With all registers used | 600 | 540 | 450 | 450 | 410 | MHz |
| F_{MAX_PATDET} | With pattern detector | 551 | 483 | 408 | 408 | 356 | MHz |
| $F_{MAX_MULT_NOMREG}$ | Two register multiply without MREG | 356 | 311 | 262 | 262 | 224 | MHz |
| $F_{MAX_MULT_NOMREG_PATDET}$ | Two register multiply without MREG with pattern detect | 327 | 286 | 241 | 241 | 211 | MHz |
| $F_{MAX_PREADD_MULT_NOADREG}$ | Without ADREG | 398 | 347 | 292 | 292 | 254 | MHz |
| $F_{MAX_PREADD_MULT_NOADREG_PATDET}$ | Without ADREG with pattern detect | 398 | 347 | 292 | 292 | 254 | MHz |
| $F_{MAX_NOPIPELINEREG}$ | Without pipeline registers (MREG, ADREG) | 266 | 233 | 196 | 196 | 171 | MHz |
| $F_{MAX_NOPIPELINEREG_PATDET}$ | Without pipeline registers (MREG, ADREG) with pattern detect | 250 | 219 | 184 | 184 | 160 | MHz |

Configuration Switching Characteristics

Table 59: Configuration Switching Characteristics

| Symbol | Description | Speed Grade | | | | Units |
|---|--|-------------|----------|----------|----------|-------------|
| | | -3 | -2 | -1 | -1L | |
| Power-up Timing Characteristics | | | | | | |
| $T_{PL}^{(1)}$ | Program Latency | 5 | 5 | 5 | 5 | ms, Max |
| $T_{POR}^{(1)}$ | Power-on-Reset | 15/55 | 15/55 | 15/55 | 15/60 | ms, Min/Max |
| T_{ICCK} | CCLK (output) delay | 400 | 400 | 400 | 400 | ns, Min |
| $T_{PROGRAM}$ | Program Pulse Width | 250 | 250 | 250 | 250 | ns, Min |
| Master/Slave Serial Mode Programming Switching | | | | | | |
| T_{DCCK}/T_{CCKD} | DIN Setup/Hold, slave mode | 4.0/0.0 | 4.0/0.0 | 4.0/0.0 | 4.5/0.0 | ns, Min |
| T_{DSCCK}/T_{SCCKD} | DIN Setup/Hold, master mode | 4.0/0.0 | 4.0/0.0 | 4.0/0.0 | 5.0/0.0 | ns, Min |
| T_{CCO} | DOU at 2.5V | 6 | 6 | 6 | 7 | ns, Max |
| | DOU at 1.8V | 6 | 6 | 6 | 7 | ns, Max |
| F_{MCCK} | Maximum CCLK frequency, serial modes | 105 | 105 | 105 | 70 | MHz, Max |
| $F_{MCCKTOL}$ | Frequency Tolerance, master mode with respect to nominal CCLK. | 55 | 55 | 55 | 60 | % |
| F_{MSCCK} | Slave mode external CCLK | 100 | 100 | 100 | 100 | MHz |
| SelectMAP Mode Programming Switching | | | | | | |
| T_{SMDCCK}/T_{SMCCKD} | SelectMAP Data Setup/Hold | 4.0/0.0 | 4.0/0.0 | 4.0/0.0 | 5.5/0.0 | ns, Min |
| $T_{SMCSCCK}/T_{SMCCKCS}$ | CSI_B Setup/Hold | 4.0/0.0 | 4.0/0.0 | 4.0/0.0 | 5.5/0.0 | ns, Min |
| T_{SMCCKW}/T_{SMWCKK} | RDWR_B Setup/Hold | 10.0/0.0 | 10.0/0.0 | 10.0/0.0 | 16.0/0.0 | ns, Min |
| $T_{SMCKCSO}$ | CSO_B clock to out (330 Ω pull-up resistor required) | 6 | 6 | 6 | 7 | ns, Max |
| T_{SMCO} | CCLK to DATA out in readback at 2.5V | 6 | 6 | 6 | 7 | ns, Max |
| | CCLK to DATA out in readback at 1.8V | 6 | 6 | 6 | 7 | ns, Max |

Table 59: Configuration Switching Characteristics (Cont'd)

| Symbol | Description | Speed Grade | | | | Units |
|--|---|---------------|---------------|---------------|---------------|-------------|
| | | -3 | -2 | -1 | -1L | |
| T _{SMCKBY} | CCLK to BUSY out in readback at 2.5V | 6 | 6 | 6 | 7 | ns, Max |
| | CCLK to BUSY out in readback at 1.8V | 6 | 6 | 6 | 7 | ns, Max |
| F _{SMCK} | Maximum Frequency with respect to nominal CCLK | 100 | 100 | 100 | 70 | MHz, Max |
| F _{RBCK} | Maximum Readback Frequency with respect to nominal CCLK | 100 | 100 | 100 | 60 | MHz, Max |
| F _{MCCKTOL} | Frequency tolerance, master mode with respect to nominal CCLK | 55 | 55 | 55 | 60 | % |
| Boundary-Scan Port Timing Specifications | | | | | | |
| T _{TAPTCK} /T _{TCKTAP} | TMS and TDI Setup time before TCK/ Hold time after TCK | 3.0/2.0 | 3.0/2.0 | 3.0/2.0 | 4.0/2.0 | ns, Min |
| T _{TCKTDO} | TCK falling edge to TDO output valid at 2.5V | 6 | 6 | 6 | 7 | ns, Max |
| | TCK falling edge to TDO output valid at 1.8V | 6 | 6 | 6 | 7 | ns, Max |
| F _{TCK} | Maximum configuration TCK clock frequency | 66 | 66 | 66 | 33 | MHz, Max |
| F _{TCKB_MIN} | Minimum boundary-scan TCK clock frequency when using IEEE Std 1149.6 (AC-JTAG). Minimum operating temperature for IEEE Std 1149.6 is 0°C. | 15 | 15 | 15 | 15 | MHz, Min |
| F _{TCKB} | Maximum boundary-scan TCK clock frequency | 66 | 66 | 66 | 33 | MHz, Max |
| BPI Master Flash Mode Programming Switching | | | | | | |
| T _{BPICCO} ⁽²⁾ | ADDR[25:0], RS[1:0], FCS_B, FOE_B, FWE_B outputs valid after CCLK rising edge at 2.5V | 6 | 6 | 6 | 7 | ns |
| | ADDR[25:0], RS[1:0], FCS_B, FOE_B, FWE_B outputs valid after CCLK rising edge at 1.8V | 6 | 6 | 6 | 7 | ns |
| T _{BPIDCC} /T _{BPICCD} | Setup/Hold on D[15:0] data input pins | 4.0/0.0 | 4.0/0.0 | 4.0/0.0 | 5.0/0.0 | ns |
| T _{INITADDR} | Minimum period of initial ADDR[25:0] address cycles | 3 | 3 | 3 | 3 | CCLK cycles |
| SPI Master Flash Mode Programming Switching | | | | | | |
| T _{SPIDCC} /T _{SPIDCCD} | DIN Setup/Hold before/after the rising CCLK edge | 3.0/0.0 | 3.0/0.0 | 3.0/0.0 | 3.5/0.0 | ns |
| T _{SPICCM} | MOSI clock to out at 2.5V | 6 | 6 | 6 | 7 | ns |
| | MOSI clock to out at 1.8V | 6 | 6 | 6 | 7 | ns |
| T _{SPICFC} | FCS_B clock to out at 2.5V | 6 | 6 | 6 | 7 | ns |
| | FCS_B clock to out at 1.8V | 6 | 6 | 6 | 7 | ns |
| T _{FSINIT} /T _{FSINITH} | FS[2:0] to INIT_B rising edge Setup and Hold | 2 | 2 | 2 | 2 | µs |
| CCLK Output (Master Modes) | | | | | | |
| T _{MCCKL} | Master CCLK clock Low time duty cycle | 45/55 | 45/55 | 45/55 | 40/60 | %, Min/Max |
| T _{MCCKH} | Master CCLK clock High time duty cycle | 45/55 | 45/55 | 45/55 | 40/60 | %, Min/Max |
| CCLK Input (Slave Modes) | | | | | | |
| T _{SCCKL} | Slave CCLK clock minimum Low time | 2.5 | 2.5 | 2.5 | 2.5 | ns, Min |
| T _{SCCKH} | Slave CCLK clock minimum High time | 2.5 | 2.5 | 2.5 | 2.5 | ns, Min |
| Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK | | | | | | |
| F _{DCK} | Maximum frequency for DCLK | 200 | 200 | 200 | 200 | MHz |
| T _{MMCMDCK_DADDR} / T _{MMCMCKD_DADDR} | DADDR Setup/Hold | 1.25/ 0.00 | 1.40/ 0.00 | 1.63/ 0.00 | 1.64/ 0.00 | ns |

Table 59: Configuration Switching Characteristics (Cont'd)

| Symbol | Description | Speed Grade | | | | Units |
|---|---------------------------------|---------------|---------------|---------------|---------------|-------|
| | | -3 | -2 | -1 | -1L | |
| $T_{MMCMCKD_DI}/$ $T_{MMCMCKD_DI}$ | DI Setup/Hold | 1.25/ 0.00 | 1.40/ 0.00 | 1.63/ 0.00 | 1.64/ 0.00 | ns |
| $T_{MMCMCKD_DEN}/$ $T_{MMCMCKD_DEN}$ | DEN Setup/Hold time | 1.25/ 0.00 | 1.40/ 0.00 | 1.63/ 0.00 | 1.64/ 0.00 | ns |
| $T_{MMCMCKD_DWE}/$ $T_{MMCMCKD_DWE}$ | DWE Setup/Hold time | 1.25/ 0.00 | 1.40/ 0.00 | 1.63/ 0.00 | 1.64/ 0.00 | ns |
| $T_{MMCMCKO_DO}$ | CLK to out of DO ⁽³⁾ | 2.60 | 3.02 | 3.64 | 3.68 | ns |
| $T_{MMCMCKO_DRDY}$ | CLK to out of DRDY | 0.32 | 0.34 | 0.38 | 0.38 | ns |

Notes:

1. To support longer delays in configuration, use the design solutions described in [UG360: Virtex-6 FPGA Configuration User Guide](#).
2. Only during configuration, the last edge is determined by a weak pull-up/pull-down resistor in the I/O.
3. DO will hold until next DRP operation.

Clock Buffers and Networks

Table 60: Global Clock Switching Characteristics (Including BUFCTRL)

| Symbol | Description | Devices | Speed Grade | | | | Units |
|--|-------------------------------|------------------|---------------|---------------|---------------|---------------|-------|
| | | | -3 | -2 | -1 | -1L | |
| $T_{BCCCK_CE}/T_{BCCCK_CE}$ ⁽¹⁾ | CE pins Setup/Hold | All | 0.11/ 0.00 | 0.13/ 0.00 | 0.16/ 0.00 | 0.13/ 0.00 | ns |
| T_{BCCCK_S}/T_{BCCCK_S} ⁽¹⁾ | S pins Setup/Hold | All | 0.11/ 0.00 | 0.13/ 0.00 | 0.16/ 0.00 | 0.13/ 0.00 | ns |
| T_{BCKO_O} ⁽²⁾ | BUFCTRL delay from I0/I1 to O | All | 0.07 | 0.08 | 0.10 | 0.10 | ns |
| Maximum Frequency | | | | | | | |
| F_{MAX} | Global clock tree (BUFCTRL) | All except LX760 | 800 | 750 | 700 | 667 | MHz |
| | | LX760 | N/A | 700 | 700 | 667 | MHz |

Notes:

1. T_{BCCCK_CE} and T_{BCCCK_S} must be satisfied to assure glitch-free operation of the global clock when switching between clocks. These parameters do not apply to the BUFCTRL_VIRTEX4 primitive that assures glitch-free operation. The other global clock setup and hold times are optional; only needing to be satisfied if device operation requires simulation matches on a cycle-for-cycle basis when switching between clocks.
2. T_{BCKO_O} (BUFCTRL delay from I0 to O) values are the same as T_{BCKO_O} values.

Table 61: Input/Output Clock Switching Characteristics (BUFIO)

| Symbol | Description | Speed Grade | | | | Units |
|--------------------------|--------------------------------|-------------|------|------|------|-------|
| | | -3 | -2 | -1 | -1L | |
| T_{BIOCKO_O} | Clock to out delay from I to O | 0.14 | 0.16 | 0.18 | 0.21 | ns |
| Maximum Frequency | | | | | | |
| F_{MAX} | I/O clock tree (BUFIO) | 800 | 800 | 710 | 710 | MHz |

Table 62: Regional Clock Switching Characteristics (BUFR)

| Symbol | Description | Speed Grade | | | | Units |
|---------------------|---|-------------|------|------|------|-------|
| | | -3 | -2 | -1 | -1L | |
| T_{BRCKO_O} | Clock to out delay from I to O | 0.56 | 0.62 | 0.73 | 0.82 | ns |
| $T_{BRCKO_O_BYP}$ | Clock to out delay from I to O with Divide Bypass attribute set | 0.28 | 0.31 | 0.36 | 0.41 | ns |

Table 62: Regional Clock Switching Characteristics (BUFR) (Cont'd)

| Symbol | Description | Speed Grade | | | | Units |
|---------------------------------|---------------------------------|-------------|------|------|------|-------|
| | | -3 | -2 | -1 | -1L | |
| T _{BRDO_O} | Propagation delay from CLR to O | 0.69 | 0.74 | 0.80 | 1.12 | ns |
| Maximum Frequency | | | | | | |
| F _{MAX} ⁽¹⁾ | Regional clock tree (BUFR) | 500 | 420 | 300 | 300 | MHz |

Notes:

1. The maximum input frequency to the BUFR is the BUFIO F_{MAX} frequency.

Table 63: Horizontal Clock Buffer Switching Characteristics (BUFH)

| Symbol | Description | Speed Grade | | | | Units |
|---|--------------------------------|---------------|---------------|---------------|---------------|-------|
| | | -3 | -2 | -1 | -1L | |
| T _{BHCKO_O} | BUFH delay from I to O | 0.10 | 0.11 | 0.13 | 0.15 | ns |
| T _{BHCK_CE} /T _{BHCKC_CE} | CE pin Setup and Hold | 0.04/ 0.04 | 0.04/ 0.04 | 0.05/ 0.05 | 0.04/ 0.04 | ns |
| Maximum Frequency | | | | | | |
| F _{MAX} | Horizontal clock buffer (BUFH) | 800 | 750 | 700 | 667 | MHz |

MMCM Switching Characteristics

Table 64: MMCM Specification

| Symbol | Description | Speed Grade | | | | Units |
|------------------------------------|--|---|------|------|------|-------|
| | | -3 | -2 | -1 | -1L | |
| F _{INMAX} | Maximum Input Clock Frequency ⁽¹⁾ | 800 | 750 | 700 | 700 | MHz |
| F _{INMIN} | Minimum Input Clock Frequency | 10 | 10 | 10 | 10 | MHz |
| F _{INJITTER} | Maximum Input Clock Period Jitter | < 20% of clock input period or 1 ns Max | | | | |
| F _{INDUTY} ⁽²⁾ | Allowable Input Duty Cycle: 10—49 MHz | 25/75 | | | | % |
| | Allowable Input Duty Cycle: 50—199 MHz | 30/70 | | | | % |
| | Allowable Input Duty Cycle: 200—399 MHz | 35/65 | | | | % |
| | Allowable Input Duty Cycle: 400—499 MHz | 40/60 | | | | % |
| | Allowable Input Duty Cycle: >500 MHz | 45/55 | | | | % |
| F _{MIN_PSCLK} | Minimum Dynamic Phase Shift Clock Frequency | 0.01 | 0.01 | 0.01 | 0.01 | MHz |
| F _{MAX_PSCLK} | Maximum Dynamic Phase Shift Clock Frequency | 550 | 500 | 450 | 450 | MHz |
| F _{VCOMIN} | Minimum MMCM VCO Frequency | 600 | 600 | 600 | 600 | MHz |
| F _{VCOMAX} | Maximum MMCM VCO Frequency | 1600 | 1440 | 1200 | 1200 | MHz |
| F _{BANDWIDTH} | Low MMCM Bandwidth at Typical ⁽³⁾ | 1.00 | 1.00 | 1.00 | 1.00 | MHz |
| | High MMCM Bandwidth at Typical ⁽³⁾ | 4.00 | 4.00 | 4.00 | 4.00 | MHz |
| T _{STATPHAOFFSET} | Static Phase Offset of the MMCM Outputs ⁽⁴⁾ | 0.12 | 0.12 | 0.12 | 0.12 | ns |
| T _{OUTJITTER} | MMCM Output Jitter ⁽⁵⁾ | Note 3 | | | | |
| T _{OUTDUTY} | MMCM Output Clock Duty Cycle Precision ⁽⁶⁾ | 0.15 | 0.20 | 0.20 | 0.20 | ns |
| T _{LOCKMAX} | MMCM Maximum Lock Time | 100 | 100 | 100 | 100 | µs |
| F _{OUTMAX} | MMCM Maximum Output Frequency | 800 | 750 | 700 | 700 | MHz |
| F _{OUTMIN} | MMCM Minimum Output Frequency ⁽⁷⁾⁽⁸⁾ | 4.69 | 4.69 | 4.69 | 4.69 | MHz |
| T _{EXTFDVAR} | External Clock Feedback Variation | < 20% of clock input period or 1 ns Max | | | | |

Table 64: MMCM Specification (Cont'd)

| Symbol | Description | Speed Grade | | | | Units |
|---|--|-----------------------------|--------------|--------------|--------------|-------|
| | | -3 | -2 | -1 | -1L | |
| $RST_{MINPULSE}$ | Minimum Reset Pulse Width | 1.5 | 1.5 | 1.5 | 1.5 | ns |
| F_{PFDMAX} | Maximum Frequency at the Phase Frequency Detector with Bandwidth Set to High or Optimized ⁽⁹⁾ | 550 | 500 | 450 | 450 | MHz |
| | Maximum Frequency at the Phase Frequency Detector with Bandwidth Set to Low | 300 | 300 | 300 | 300 | MHz |
| F_{PFDMIN} | Minimum Frequency at the Phase Frequency Detector with Bandwidth Set to High or Optimized | 135 | 135 | 135 | 135 | MHz |
| | Minimum Frequency at the Phase Frequency Detector with Bandwidth Set to Low | 10 | 10 | 10 | 10 | MHz |
| $T_{FBDELAY}$ | Maximum Delay in the Feedback Path | 3 ns Max or one CLKIN cycle | | | | |
| $T_{MMCMCKD_PSEN}/$ $T_{MMCMCKD_PSEN}$ | Setup and Hold of Phase Shift Enable | 1.04 0.00 | 1.04 0.00 | 1.04 0.00 | 1.04 0.00 | ns |
| $T_{MMCMCKD_PSINCDEC}/$ $T_{MMCMCKD_PSINCDEC}$ | Setup and Hold of Phase Shift Increment/Decrement | 1.04 0.00 | 1.04 0.00 | 1.04 0.00 | 1.04 0.00 | ns |
| $T_{MMCMCKO_PSDONE}$ | Phase Shift Clock-to-Out of PSDONE | 0.32 | 0.34 | 0.38 | 0.38 | ns |

Notes:

- When $DIVCLK_DIVIDE = 3$ or 4 , F_{INMAX} is 315 MHz.
- This duty cycle specification does not apply to the GTH_QUAD (GTH) to MMCM connection. The GTH transceivers drive the MMCMs at the following maximum frequencies: 323 MHz for -1 speed grade devices, 350 MHz for -2 speed grade devices, or 350 MHz for -3 speed grade devices.
- The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
- The static offset is measured between any MMCM outputs with identical phase.
- Values for this parameter are available in the Clocking Wizard.
See http://www.xilinx.com/products/intellectual-property/clocking_wizard.htm.
- Includes global clock buffer.
- Calculated as $F_{VCO}/128$ assuming output duty cycle is 50%.
- When $CLKOUT4_CASCADE = TRUE$, F_{OUTMIN} is 0.036 MHz.
- In ISE software 12.3 (or earlier versions supporting the Virtex-6 family), the phase frequency detector Optimized bandwidth setting is equivalent to the High bandwidth setting. Starting with ISE software 12.4, the Optimized bandwidth setting is automatically adjusted to Low when the software can determine that the phase frequency detector input is less than 135 MHz.

Virtex-6 Device Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. The representative values for typical pin locations and normal clock loading are listed in Table 65. Values are expressed in nanoseconds unless otherwise noted.

Table 65: Global Clock Input to Output Delay Without MMCM

| Symbol | Description | Device | Speed Grade | | | | Units |
|--|--|------------|-------------|------|------|------|-------|
| | | | -3 | -2 | -1 | -1L | |
| LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, <i>without</i> MMCM. | | | | | | | |
| T _{ICKOF} | Global Clock input and OUTFF <i>without</i> MMCM | XC6VLX75T | 4.91 | 5.32 | 5.88 | 6.02 | ns |
| | | XC6VLX130T | 4.89 | 5.33 | 6.00 | 6.13 | ns |
| | | XC6VLX195T | 5.02 | 5.46 | 6.13 | 6.27 | ns |
| | | XC6VLX240T | 5.02 | 5.46 | 6.13 | 6.27 | ns |
| | | XC6VLX365T | 5.30 | 5.75 | 6.43 | 6.37 | ns |
| | | XC6VLX550T | N/A | 6.02 | 6.72 | 6.60 | ns |
| | | XC6VLX760 | N/A | 6.26 | 6.97 | 6.87 | ns |
| | | XC6VSX315T | 5.40 | 5.85 | 6.54 | 6.49 | ns |
| | | XC6VSX475T | N/A | 6.01 | 6.71 | 6.61 | ns |
| | | XC6VHX250T | 5.18 | 5.63 | 6.30 | N/A | ns |
| | | XC6VHX255T | 5.20 | 5.66 | 6.34 | N/A | ns |
| | | XC6VHX380T | 5.38 | 5.84 | 6.53 | N/A | ns |
| | | XC6VHX565T | N/A | 6.03 | 6.71 | N/A | ns |
| | | XQ6VLX130T | N/A | 5.33 | 6.00 | 6.13 | ns |
| | | XQ6VLX240T | N/A | 5.46 | 6.13 | 6.27 | ns |
| | | XQ6VLX550T | N/A | N/A | 6.72 | 6.60 | ns |
| | | XQ6VSX315T | N/A | 5.85 | 6.54 | 6.49 | ns |
| XQ6VSX475T | N/A | N/A | 6.71 | 6.61 | ns | | |

Notes:

- Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

Table 66: Global Clock Input to Output Delay With MMCM

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|------------|-------------|------|------|------|-------|
| | | | -3 | -2 | -1 | -1L | |
| LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, <i>with</i> MMCM. | | | | | | | |
| T _{ICKOFMMCMGC} | Global Clock Input and OUTFF <i>with</i> MMCM | XC6VLX75T | 2.34 | 2.50 | 2.77 | 2.85 | ns |
| | | XC6VLX130T | 2.35 | 2.51 | 2.78 | 2.87 | ns |
| | | XC6VLX195T | 2.36 | 2.52 | 2.79 | 2.88 | ns |
| | | XC6VLX240T | 2.36 | 2.52 | 2.79 | 2.88 | ns |
| | | XC6VLX365T | 2.37 | 2.53 | 2.79 | 2.89 | ns |
| | | XC6VLX550T | N/A | 2.55 | 2.82 | 2.93 | ns |
| | | XC6VLX760 | N/A | 2.54 | 2.82 | 2.92 | ns |
| | | XC6VSX315T | 2.35 | 2.51 | 2.79 | 2.87 | ns |
| | | XC6VSX475T | N/A | 2.43 | 2.70 | 2.79 | ns |
| | | XC6VHX250T | 2.36 | 2.53 | 2.80 | N/A | ns |
| | | XC6VHX255T | 2.46 | 2.63 | 2.91 | N/A | ns |
| | | XC6VHX380T | 2.39 | 2.59 | 2.83 | N/A | ns |
| | | XC6VHX565T | N/A | 2.54 | 2.81 | N/A | ns |
| | | XQ6VLX130T | N/A | 2.51 | 2.78 | 2.87 | ns |
| | | XQ6VLX240T | N/A | 2.52 | 2.79 | 2.88 | ns |
| | | XQ6VLX550T | N/A | N/A | 2.82 | 2.93 | ns |
| | | XQ6VSX315T | N/A | 2.51 | 2.79 | 2.87 | ns |
| | | XQ6VSX475T | N/A | N/A | 2.70 | 2.79 | ns |

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

Table 67: Clock-Capable Clock Input to Output Delay With MMCM

| Symbol | Description | Device | Speed Grade | | | | Units |
|--|--|------------|-------------|------|------|------|-------|
| | | | -3 | -2 | -1 | -1L | |
| LVCMOS25 Clock-capable Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, <i>with</i> MMCM. | | | | | | | |
| T _{ICKOFMMCMCC} | Clock-capable Clock Input and OUTFF <i>with</i> MMCM | XC6VLX75T | 2.22 | 2.38 | 2.63 | 2.72 | ns |
| | | XC6VLX130T | 2.24 | 2.39 | 2.65 | 2.74 | ns |
| | | XC6VLX195T | 2.24 | 2.40 | 2.65 | 2.75 | ns |
| | | XC6VLX240T | 2.24 | 2.40 | 2.65 | 2.75 | ns |
| | | XC6VLX365T | 2.25 | 2.42 | 2.65 | 2.76 | ns |
| | | XC6VLX550T | N/A | 2.43 | 2.68 | 2.80 | ns |
| | | XC6VLX760 | N/A | 2.42 | 2.69 | 2.79 | ns |
| | | XC6VSX315T | 2.23 | 2.38 | 2.65 | 2.73 | ns |
| | | XC6VSX475T | N/A | 2.30 | 2.57 | 2.66 | ns |
| | | XC6VHX250T | 2.25 | 2.41 | 2.67 | N/A | ns |
| | | XC6VHX255T | 2.35 | 2.51 | 2.78 | N/A | ns |
| | | XC6VHX380T | 2.27 | 2.43 | 2.69 | N/A | ns |
| | | XC6VHX565T | N/A | 2.41 | 2.68 | N/A | ns |
| | | XQ6VLX130T | N/A | 2.39 | 2.65 | 2.74 | ns |
| | | XQ6VLX240T | N/A | 2.40 | 2.65 | 2.75 | ns |
| | | XQ6VLX550T | N/A | N/A | 2.68 | 2.80 | ns |
| | | XQ6VSX315T | N/A | 2.38 | 2.65 | 2.73 | ns |
| | | XQ6VSX475T | N/A | N/A | 2.57 | 2.66 | ns |

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

Virtex-6 Device Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. The representative values for typical pin locations and normal clock loading are listed in Table 68. Values are expressed in nanoseconds unless otherwise noted.

Table 68: Global Clock Input Setup and Hold Without MMCM

| Symbol | Description | Device | Speed Grade | | | | Units |
|--|---|------------|----------------|----------------|----------------|----------------|-------|
| | | | -3 | -2 | -1 | -1L | |
| Input Setup and Hold Time Relative to Global Clock Input Signal for LVC MOS25 Standard.⁽¹⁾ | | | | | | | |
| T _{PSFD} / T _{PHFD} | Full Delay (Legacy Delay or Default Delay) Global Clock Input and IFF ⁽²⁾ without MMCM | XC6VLX75T | 1.33/ 0.03 | 1.44/ 0.03 | 1.75/ 0.03 | 2.18/ -0.22 | ns |
| | | XC6VLX130T | 1.31/ -0.08 | 1.54/ -0.08 | 1.88/ -0.08 | 2.31/ -0.12 | ns |
| | | XC6VLX195T | 1.36/ -0.11 | 1.60/ -0.11 | 1.97/ -0.11 | 2.40/ -0.25 | ns |
| | | XC6VLX240T | 1.36/ -0.11 | 1.60/ -0.11 | 1.97/ -0.11 | 2.40/ -0.25 | ns |
| | | XC6VLX365T | 1.79/ -0.28 | 1.87/ -0.28 | 2.17/ -0.28 | 2.48/ -0.24 | ns |
| | | XC6VLX550T | N/A | 2.22/ -0.12 | 2.36/ -0.12 | 2.77/ -0.26 | ns |
| | | XC6VLX760 | N/A | 2.19/ -0.24 | 2.35/ -0.24 | 2.71/ -0.21 | ns |
| | | XC6VSX315T | 1.75/ -0.09 | 1.85/ -0.09 | 2.06/ -0.09 | 2.47/ -0.24 | ns |
| | | XC6VSX475T | N/A | 2.14/ -0.14 | 2.31/ -0.14 | 2.71/ -0.30 | ns |
| | | XC6VHX250T | 1.93/ -0.22 | 2.04/ -0.22 | 2.25/ -0.22 | N/A | ns |
| | | XC6VHX255T | 1.81/ -0.33 | 2.11/ -0.33 | 2.56/ -0.33 | N/A | ns |
| | | XC6VHX380T | 1.93/ -0.11 | 2.04/ -0.11 | 2.25/ -0.11 | N/A | ns |
| | | XC6VHX565T | N/A | 2.20/ -0.12 | 2.39/ -0.12 | N/A | ns |
| | | XQ6VLX130T | N/A | 1.54/ -0.08 | 1.88/ -0.08 | 2.31/ -0.12 | ns |
| | | XQ6VLX240T | N/A | 1.60/ -0.11 | 1.97/ -0.11 | 2.40/ -0.25 | ns |
| | | XQ6VLX550T | N/A | N/A | 2.36/ -0.12 | 2.77/ -0.26 | ns |
| | | XQ6VSX315T | N/A | 1.85/ -0.09 | 2.06/ -0.09 | 2.47/ -0.24 | ns |
| | | XQ6VSX475T | N/A | N/A | 2.31/ -0.14 | 2.71/ -0.30 | ns |

Notes:

- Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
- IFF = Input Flip-Flop or Latch
- A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

Table 69: Global Clock Input Setup and Hold With MMCM

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|--|------------|----------------|----------------|----------------|----------------|-------|
| | | | -3 | -2 | -1 | -1L | |
| Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.⁽¹⁾ | | | | | | | |
| T _{PSMMCMGC} / T _{PHMMCMGC} | No Delay Global Clock Input and IFF ⁽²⁾ with MMCM | XC6VLX75T | 1.45/ -0.18 | 1.57/ -0.18 | 1.72/ -0.18 | 1.78/ -0.08 | ns |
| | | XC6VLX130T | 1.53/ -0.18 | 1.65/ -0.18 | 1.81/ -0.18 | 1.87/ -0.07 | ns |
| | | XC6VLX195T | 1.54/ -0.17 | 1.66/ -0.17 | 1.82/ -0.17 | 1.87/ -0.08 | ns |
| | | XC6VLX240T | 1.54/ -0.17 | 1.66/ -0.17 | 1.82/ -0.17 | 1.87/ -0.08 | ns |
| | | XC6VLX365T | 1.55/ -0.18 | 1.67/ -0.18 | 1.83/ -0.18 | 1.87/ -0.07 | ns |
| | | XC6VLX550T | N/A | 1.84/ -0.17 | 2.02/ -0.17 | 2.06/ -0.06 | ns |
| | | XC6VLX760 | N/A | 2.26/ -0.13 | 2.49/ -0.13 | 2.06/ -0.03 | ns |
| | | XC6VSX315T | 1.56/ -0.18 | 1.68/ -0.18 | 1.84/ -0.18 | 1.89/ -0.08 | ns |
| | | XC6VSX475T | N/A | 1.85/ -0.23 | 2.03/ -0.23 | 2.07/ -0.13 | ns |
| | | XC6VHX250T | 1.52/ -0.17 | 1.64/ -0.17 | 1.80/ -0.17 | N/A | ns |
| | | XC6VHX255T | 1.52/ -0.12 | 1.64/ -0.12 | 1.85/ -0.12 | N/A | ns |
| | | XC6VHX380T | 1.68/ -0.16 | 1.81/ -0.16 | 1.99/ -0.16 | N/A | ns |
| | | XC6VHX565T | N/A | 1.81/ -0.01 | 1.99/ -0.01 | N/A | ns |
| | | XQ6VLX130T | N/A | 1.65/ -0.18 | 1.81/ -0.18 | 1.87/ -0.07 | ns |
| | | XQ6VLX240T | N/A | 1.66/ -0.17 | 1.82/ -0.17 | 1.87/ -0.08 | ns |
| | | XQ6VLX550T | N/A | N/A | 2.02/ -0.17 | 2.06/ -0.06 | ns |
| | | XQ6VSX315T | N/A | 1.68/ -0.18 | 1.84/ -0.18 | 1.89/ -0.08 | ns |
| | | XQ6VSX475T | N/A | N/A | 2.03/ -0.23 | 2.07/ -0.13 | ns |

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 70: Clock-Capable Clock Input Setup and Hold With MMCM

| Symbol | Description | Device | Speed Grade | | | | Units |
|--|---|------------|----------------|----------------|----------------|----------------|-------|
| | | | -3 | -2 | -1 | -1L | |
| Input Setup and Hold Time Relative to Clock-capable Clock Input Signal for LVCMOS25 Standard.⁽¹⁾ | | | | | | | |
| T _{PSMMCMCC} / T _{PHMMCMCC} | No Delay Clock-capable Clock Input and IFF ⁽²⁾ with MMCM | XC6VLX75T | 1.56/ -0.25 | 1.69/ -0.25 | 1.86/ -0.25 | 1.91/ -0.15 | ns |
| | | XC6VLX130T | 1.64/ -0.25 | 1.78/ -0.25 | 1.95/ -0.25 | 2.00/ -0.14 | ns |
| | | XC6VLX195T | 1.65/ -0.24 | 1.79/ -0.24 | 1.96/ -0.24 | 2.01/ -0.15 | ns |
| | | XC6VLX240T | 1.65/ -0.24 | 1.79/ -0.24 | 1.96/ -0.24 | 2.01/ -0.15 | ns |
| | | XC6VLX365T | 1.66/ -0.25 | 1.79/ -0.25 | 1.97/ -0.25 | 2.02/ -0.15 | ns |
| | | XC6VLX550T | N/A | 1.97/ -0.24 | 2.16/ -0.24 | 2.19/ -0.14 | ns |
| | | XC6VLX760 | N/A | 2.39/ -0.20 | 2.63/ -0.20 | 2.21/ -0.10 | ns |
| | | XC6VSX315T | 1.67/ -0.25 | 1.80/ -0.25 | 1.98/ -0.25 | 2.03/ -0.16 | ns |
| | | XC6VSX475T | N/A | 1.98/ -0.29 | 2.17/ -0.29 | 2.21/ -0.20 | ns |
| | | XC6VHX250T | 1.63/ -0.24 | 1.76/ -0.24 | 1.94/ -0.24 | N/A | ns |
| | | XC6VHX255T | 1.63/ -0.19 | 1.76/ -0.19 | 1.99/ -0.19 | N/A | ns |
| | | XC6VHX380T | 1.80/ -0.23 | 1.94/ -0.23 | 2.13/ -0.23 | N/A | ns |
| | | XC6VHX565T | N/A | 1.94/ -0.08 | 2.13/ -0.08 | N/A | ns |
| | | XQ6VLX130T | N/A | 1.78/ -0.25 | 1.95/ -0.25 | 2.00/ -0.14 | ns |
| | | XQ6VLX240T | N/A | 1.79/ -0.24 | 1.96/ -0.24 | 2.01/ -0.15 | ns |
| | | XQ6VLX550T | N/A | N/A | 2.16/ -0.24 | 2.19/ -0.14 | ns |
| | | XQ6VSX315T | N/A | 1.80/ -0.25 | 1.98/ -0.25 | 2.03/ -0.16 | ns |
| | | XQ6VSX475T | N/A | N/A | 2.17/ -0.29 | 2.21/ -0.20 | ns |

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Clock Switching Characteristics

The parameters in this section provide the necessary values for calculating timing budgets for Virtex-6 FPGA clock transmitter and receiver data-valid windows.

Table 71: Duty Cycle Distortion and Clock-Tree Skew

| Symbol | Description | Device | Speed Grade | | | | Units |
|--------------------|--|------------|-------------|------|------|------|-------|
| | | | -3 | -2 | -1 | -1L | |
| T_{DCD_CLK} | Global Clock Tree Duty Cycle Distortion ⁽¹⁾ | All | 0.12 | 0.12 | 0.12 | 0.12 | ns |
| T_{CKSKEW} | Global Clock Tree Skew ⁽²⁾ | XC6VLX75T | 0.15 | 0.16 | 0.18 | 0.17 | ns |
| | | XC6VLX130T | 0.25 | 0.26 | 0.29 | 0.28 | ns |
| | | XC6VLX195T | 0.26 | 0.27 | 0.31 | 0.30 | ns |
| | | XC6VLX240T | 0.26 | 0.27 | 0.31 | 0.30 | ns |
| | | XC6VLX365T | 0.28 | 0.29 | 0.31 | 0.31 | ns |
| | | XC6VLX550T | N/A | 0.50 | 0.54 | 0.54 | ns |
| | | XC6VLX760 | N/A | 0.51 | 0.56 | 0.56 | ns |
| | | XC6VSX315T | 0.27 | 0.28 | 0.32 | 0.30 | ns |
| | | XC6VSX475T | N/A | 0.39 | 0.44 | 0.42 | ns |
| | | XC6VHX250T | 0.25 | 0.26 | 0.29 | N/A | ns |
| | | XC6VHX255T | 0.35 | 0.37 | 0.41 | N/A | ns |
| | | XC6VHX380T | 0.45 | 0.47 | 0.52 | N/A | ns |
| | | XC6VHX565T | N/A | 0.46 | 0.51 | N/A | ns |
| | | XQ6VLX130T | N/A | 0.26 | 0.29 | 0.28 | ns |
| | | XQ6VLX240T | N/A | 0.27 | 0.31 | 0.30 | ns |
| | | XQ6VLX550T | N/A | N/A | 0.54 | 0.54 | ns |
| XQ6VSX315T | N/A | 0.28 | 0.32 | 0.30 | ns | | |
| XQ6VSX475T | N/A | N/A | 0.44 | 0.42 | ns | | |
| T_{DCD_BUFIO} | I/O clock tree duty cycle distortion | All | 0.08 | 0.08 | 0.08 | 0.08 | ns |
| T_{BUFIO_SKEW} | I/O clock tree skew across one clock region | All | 0.03 | 0.03 | 0.03 | 0.02 | ns |
| T_{BUFIO_SKEW2} | I/O clock tree skew across three clock regions | All | 0.10 | 0.12 | 0.23 | 0.12 | ns |
| T_{DCD_BUFR} | Regional clock tree duty cycle distortion | All | 0.15 | 0.15 | 0.15 | 0.15 | ns |

Notes:

1. These parameters represent the worst-case duty cycle distortion observable at the pins of the device using LVDS output buffers. For cases where other I/O standards are used, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
2. The T_{CKSKEW} value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA_Editor and Timing Analyzer tools to evaluate clock skew specific to your application.

Table 72: Package Skew

| Symbol | Description | Device | Package | Value | Units |
|----------------------|-----------------------------|------------|---------|-------|-------|
| T _{PKGSKEW} | Package Skew ⁽¹⁾ | XC6VLX75T | FF484 | 95 | ps |
| | | | FF784 | 146 | ps |
| | | XC6VLX130T | FF484 | 95 | ps |
| | | | FF784 | 146 | ps |
| | | | FF1156 | 165 | ps |
| | | XC6VLX195T | FF784 | 145 | ps |
| | | | FF1156 | 182 | ps |
| | | XC6VLX240T | FF784 | 146 | ps |
| | | | FF1156 | 182 | ps |
| | | | FF1759 | 187 | ps |
| | | XC6VLX365T | FF1156 | 189 | ps |
| | | | FF1759 | 184 | ps |
| | | XC6VLX550T | FF1759 | 196 | ps |
| | | | FF1760 | 249 | ps |
| | | XC6VLX760 | FF1760 | 236 | ps |
| | | | FF1156 | 168 | ps |
| | | XC6VSX315T | FF1759 | 190 | ps |
| | | | FF1156 | 168 | ps |
| | | XC6VSX475T | FF1156 | 168 | ps |
| | | | FF1759 | 204 | ps |
| | | XC6VHX250T | FF1154 | 166 | ps |
| | | XC6VHX255T | FF1155 | 168 | ps |
| | | | FF1923 | 228 | ps |
| | | XC6VHX380T | FF1154 | 159 | ps |
| | | | FF1155 | 172 | ps |
| | | | FF1923 | 227 | ps |
| | | | FF1924 | 220 | ps |
| | | XC6VHX565T | FF1923 | 232 | ps |
| | | | FF1924 | 197 | ps |
| | | XQ6VLX130T | RF784 | 146 | ps |
| | | | RF1156 | 165 | ps |
| | | | FFG1156 | 165 | ps |
| | | XQ6VLX240T | RF784 | 146 | ps |
| | | | RF1156 | 182 | ps |
| | | | FFG1156 | 182 | ps |
| | | | RF1759 | 187 | ps |
| | | XQ6VLX550T | RF1759 | 196 | ps |
| | | XQ6VSX315T | RF1156 | 168 | ps |
| | | | FFG1156 | 168 | ps |
| | | | RF1759 | 190 | ps |
| XQ6VSX475T | RF1156 | 168 | ps | | |
| | FFG1156 | 168 | ps | | |
| | RF1759 | 204 | ps | | |

Notes:

1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest flight time to longest flight time from Pad to Ball (7.0 ps per mm).
2. Package trace length information is available for these device/package combinations. This information can be used to deskew the package.

Table 73: Sample Window

| Symbol | Description | Device | Speed Grade | | | | Units |
|-------------------|--|--------|-------------|-----|-----|-----|-------|
| | | | -3 | -2 | -1 | -1L | |
| T_{SAMP} | Sampling Error at Receiver Pins ⁽¹⁾ | All | 510 | 560 | 610 | 670 | ps |
| T_{SAMP_BUFIO} | Sampling Error at Receiver Pins using BUFIO ⁽²⁾ | All | 300 | 350 | 400 | 440 | ps |

Notes:

- This parameter indicates the total sampling error of Virtex-6 FPGA DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include:
 - CLK0 MMCM jitter
 - MMCM accuracy (phase offset)
 - MMCM phase shift resolution
 These measurements do not include package or clock tree skew.
- This parameter indicates the total sampling error of Virtex-6 FPGA DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO clock network and IODELAY to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

Table 74: Pin-to-Pin Setup/Hold and Clock-to-Out

| Symbol | Description | Speed Grade | | | | Units |
|--|---------------------------|-------------|------------|------------|------------|-------|
| | | -3 | -2 | -1 | -1L | |
| Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin Using BUFIO | | | | | | |
| T_{PSCS}/T_{PHCS} | Setup/Hold of I/O clock | -0.28/1.09 | -0.28/1.16 | -0.28/1.33 | -0.18/1.79 | ns |
| Pin-to-Pin Clock-to-Out Using BUFIO | | | | | | |
| $T_{ICKOFCS}$ | Clock-to-Out of I/O clock | 4.22 | 4.59 | 5.22 | 5.63 | ns |

Revision History

The following table shows the revision history for this document:

| Date | Version | Description of Revisions |
|------------|---------|--|
| 06/24/2009 | 1.0 | Initial Xilinx release. |
| 07/16/2009 | 1.1 | Revised the maximum V_{CCAUX} and V_{IN} numbers in Table 2, page 2 . Removed empty column from Table 3, page 3 . Revised specifications on Table 20, page 13 . Updated Table 38, page 22 and added notes 1 and 2. Revised T_{DLYCCO_RDY} , $T_{IDELAYCTRL_RPW}$, and $T_{IDELAYPAT_JIT}$ in Table 53, page 41 . Updated Table 58, page 46 to more closely match the DSP48E1 speed specifications. Updated T_{TAPTCK}/T_{TCKTAP} in Table 59, page 49 . Updated XC6VLX130T parameters in Table 68 through Table 70, page 59 . |
| 08/19/2009 | 1.2 | Added values for -1L voltages and speed grade in all pertinent tables. Added V_{FS} and notes to Table 1 and Table 2 . Removed DV_{PPIN} from the example in Figure 2 . Added networking applications to Table 41, page 25 . Changed and added to the block RAM F_{MAX} section in Table 57, page 44 including removing Note 12. Changed F_{PFDMAX} values and corrected units for $T_{STATPHAOFFSET}$ and $T_{OUTDUTY}$ in Table 64, page 52 . Updated Table 71, page 60 . |
| 09/16/2009 | 2.0 | Added Virtex-6 HXT devices to entire document including GTH Transceiver Specifications . Updated speed specifications as described in Switching Characteristics , includes changes in Table 51 , Table 57 , Table 58 , and Table 66 through Table 70 . Comprehensive changes to Table 14 , Table 15 , and Table 16 . Added conditions to DV_{PPOUT} and revised description of T_{OSKEW} in Table 17 . Removed V_{ISE} specification and note from Table 18 . Added note 3 to Table 23 . Updated note 3 in Table 24 . Updated LVCMOS25 delays in Table 44 . Updated specification for T_{IOTPHZ} in Table 46 . Removed $T_{BUFHSKEW}$ from Table 71, page 60 and added values for $T_{BUFIOSKEW}$. Added values in Table 74 . |

| Date | Version | Description of Revisions |
|------------|---------|---|
| 01/18/2010 | 2.1 | Changed absolute maximum ratings for both V_{IN} and V_{TS} in Table 1 . Added data to Table 3 . Added data to Table 5 . Updated SSTL15 in Table 7 . Updated V_{OCM} and V_{OD} values in Table 8 . Added eFUSE endurance Table 12 . Added values to $V_{MGTREFCLK}$ and V_{IN} in Table 13 , page 11 . Added values and updated tables in the GTX Transceiver Specifications and GTH Transceiver Specifications sections. Added Table 27 and Figure 4 . Revised parameters and values in Table 39 . Updated Table 40 , page 23 . Added data to Table 41 . Updated speed specification to v1.04 with appropriate changes to Table 42 and Table 43 including production release of the XC6VLX240T for -1 and -2 speed grades. Speed specification changes and numerous updates also made to Table 44 , and Table 49 through Table 71 . Added data to Table 73 and Table 74 . |
| 02/09/2010 | 2.2 | Revised description of C_{IN} in Table 3 . Clarified values in Table 5 . Fixed SDR LVDS unit error in Table 41 . |
| 04/12/2010 | 2.3 | Added note 3 and update value of n in Table 3 . Clarified simultaneous power-down in Power-On Power Supply Requirements . Updated external reference junction temperatures in Table 40 , Analog-to-Digital Specifications . Updated speed specification to v1.05 with appropriate changes to Table 42 and Table 43 including production release of the XC6VLX130T for -1 and -2 speed grades. Fixed note 4 in Table 48 . Increased the -2 specification for $F_{IDELAYCTRL_REF}$ and clarified units for $T_{IDELAYPAT_JIT}$ in Table 53 . Added note 1 to Table 62 . |
| 05/11/2010 | 2.4 | Updated F_{RXREC} in Table 22 . Revised $F_{IDELAYCTRL_REF}$ in Table 53 . Removed $T_{RCKO_PARITY_ECC}$: Clock CLK to ECCPARITY in standard ECC mode row in Table 57 . Added XC6VLX130T values to Table 72 . |
| 05/26/2010 | 2.5 | Added XC6VLX195T data to Table 5 . Updated values in Table 22 including adding note 2 and note 3. Updated speed specification to v1.06 with appropriate changes to Table 42 and Table 43 including production release of the XC6VLX195T for -1 and -2 speed grades. Added XC6VLX195T values to Table 72 . |
| 07/16/2010 | 2.6 | Changed Table 42 and Table 43 to production status on the -3 speed grade XC6VLX130T, XC6VLX195T, and XC6VLX240T devices. Added XC6VHX250T data to Table 4 and Table 72 . Added Note 6 to Table 64 . |
| 07/23/2010 | 2.7 | Changed Table 42 and Table 43 to production status on the XC6VLX75T, XC6VLX365T, XC6VLX550T, XC6VLX760, XC6VVSX315T, and XC6VVSX475T devices using ISE 12.2 software with speed specification v1.08. Updated $V_{CMOUTDC}$ equation to $MGTAVTT - D_{VPP_OUT}/4$ in Table 17 . Updated some -3, -2, -1 specifications in Table 65 through Table 72 . Added and updated -1L specifications to Table 41 and for most switching characteristics tables. |
| 07/30/2010 | 2.8 | Changed Table 42 and Table 43 to production status on the -1L speed grade for the XC6VLX130T, XC6VLX195T, XC6VLX240T, XC6VLX365T, and XC6VLX550T devices using ISE 12.2 software with current speed specifications. Also updated the speed specifications for XC6VLX75T, XC6VLX550T, and XC6VVSX315T. Updated V_{CCINT} specifications for -1L speed grade industrial temperature range devices in Table 2 . |
| 09/20/2010 | 2.9 | In Table 32 , changed $F_{GPLLMAX}$ specification in -3 column from 5.951 to 5.591. In Table 40 , changed F_{MAX} for the DCLK from 250 MHz to 80 MHz. |
| 10/18/2010 | 2.10 | The specification change in version 2.9, Table 40 is described in XCN10032 , <i>Virtex-6 FPGA: GTX Transceiver User Guide, Family Data Sheet (SYSMON DCLK), and JTAG ID Changes</i> In this version (2.10), -1L(I) data is added to Table 4 and clarified in Note 2. Changed Table 42 and Table 43 to production status on the -1L speed grade XC6VLX75T, XC6VLX760, XC6VVSX315T, and XC6VVSX475T devices using ISE 12.3 software with current speed specifications. Revised the XC6VLX760 -1L speed specification for $T_{PHMMCMGC}$ in Table 69 and $T_{PHMMCMCC}$ in Table 70 . |
| 01/17/2011 | 2.11 | Changed in Table 42 and Table 43 to production status on the XC6VHX250T devices using ISE 12.4 software with current speed specifications. Added industrial temperature range (T_I) recommended specifications to Table 2 ; including specific ranges for the -2I XC6VVSX475T, XC6VLX550T, XC6VLX760, and XC6VHX565T devices. Added note 3 to Table 36 and maximum total jitter values. Added note 4 to Table 37 and maximum sinusoidal jitter values. Added note 2 to Table 43 . Revised F_{MAX} descriptions in Table 57 and added note 12. Added note 8 to F_{PFDMIN} in Table 64 . The following revisions are due to specification changes as described in XCN11009 , <i>Virtex-6 FPGA: Data Sheet, User Guides, and JTAG ID Updates</i> . In Table 59: Configuration Switching Characteristics , page 49 , revised -1L specifications for T_{POR} , F_{MCCCK} , $F_{MCCCKTOL}$, T_{SMCCKW} , T_{SMCCKW} , F_{RBCKK} , F_{TCK} , F_{TCKB} , T_{MCCCKL} , and T_{MCCCKH} . In Table 64: MMCM Specification , added bandwidth settings to F_{PFDMIN} and added note 1. |

| Date | Version | Description of Revisions |
|------------|---------|---|
| 02/08/2011 | 2.12 | Removed note 1 from Table 4 as the larger devices (XC6VLX550T, XC6VLX760, XC6VSX475T, and XC6VHX565T) are now offered in -2I. Updated Table 4 and Table 5 with data for the XC6VHX380T in the FF(G)1154 package. In Table 41 , updated -1L specification for DDR3. Added Note 1 to Table 42 . Moved the XC6VHX380T devices in the FF(G)1154 package to production release in Table 43 using ISE 12.4 software with current speed specifications. Updated description for F_{INDUTY} in Table 64 . |
| 02/25/2011 | 3.0 | Designated the data sheet as Preliminary for all devices not already labeled production in Table 42 . Changed the XC6VHX380T devices in all packages to production status in Table 42 and Table 43 . Removed note 1 from Table 42 . Added maximum specifications to Table 25 . Updated $T_{HAVCC2HAVCCR}$ in Table 27 . Updated the typical values and notes in Table 28 and Table 29 . Added values to Table 30 and Table 31 . In Table 34 , added values for T_{LOCK} and T_{PHASE} . Updated the values in Table 36 and added note 3. Updated Table 37 and added note 4. |
| 03/21/2011 | 3.1 | Updated Table 2 including Note 7 . In Table 4 , added Note 3 and -2E, extended temperature range to the XC6VLX550T, XC6VLX760, XC6VSX475T, and XC6VHX380T devices, and added Note 5 for the XC6VHX565T. Updated Table 28 typical values. Updated the description for $F_{IDELAYCTRL_REF}$ in Table 53 . Updated F_{MCCK} in Table 59 . |
| 04/01/2011 | 3.2 | Added T_j values for C, E, and I temperature ranges to Table 2 . Updated the I_{CCQ} values in Table 4 . Updated F_{GCLK} in Table 34 . Designated the data sheet as Production for all devices not already labeled production in Table 42 . Changed the XC6VHX255T and XC6VHX565T devices in all packages to production status in Table 42 and Table 43 . This included updates to the Virtex-6 Device Pin-to-Pin Output Parameter Guidelines and Virtex-6 Device Pin-to-Pin Input Parameter Guidelines for these devices. Production speed specifications for these devices are available using the speed specification v1.14 in the ISE 13.1 software update. Updated and added package skew values to Table 72 ; these values are correct with regards to previous production released speed specifications in software. Updated copyright page 1 and Notice of Disclaimer . |
| 12/08/2011 | 3.3 | Production release of the Defense-grade XQ devices in Table 42 and Table 43 using ISE v13.3 v1.17 Patch for -2 and -1 speed specifications; and v1.10 for -1L speed specifications. Added the XQ6VLX130T, XQ6VLX240T, XQ6VLX550T, XQ6VSX315T, and XQ6VSX475T to the data sheet which included adding Table 45 . Updated T_j in Table 2 . In Table 40 , updated T_j for most specifications and added Note 4 . Added Note 4 to Table 41 . Added -1(XQ) speed specification columns only to Table 50 , Table 51 , Table 52 , and Table 58 . Updated V_{OD} in Table 8 , V_{OCM} in Table 9 , and V_{OCM} and V_{DIFF} in Table 10 . Updated the Power-On Power Supply Requirements section. In Table 27 , updated maximum specification for $T_{HAVCC2HAVCCR}$ and added Note 3 . Updated T_j in Table 40 . In Table 41 , increased the DDR LVDS receiver (SPI-4.2) -1 speed grade performance value from 1.0 Gb/s to 1.1 Gb/s. In Table 60 , updated the F_{MAX} to add a separate row for the LX760 device values. The speed specifications in the software tools have always matched these values for the LX760, the data sheet is now correct. Updated the notes for $T_{OUTJITTER}$ in Table 64 . |
| 01/12/2012 | 3.4 | Added the temperature range -2E to Note 5 in Table 4 . |
| 05/17/2013 | 3.5 | Added the DIFF_SSTL15 I/O standard to Table 7 . Added Note 1 to Table 18 . |
| 03/18/2014 | 3.6 | Updated Note 8 in Table 64 . Updated Notice of Disclaimer . |

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| Business Type | Trading Company, Distributor/Wholesaler |
| Main Products | Electronic Integrated Circuit |
| Certifications | ISO9001 |
| Total Annual Revenue | US\$2.5 Million - US\$5 Million |
| Country / Region | Hongkong, China |
| Total Employees | 100 - 200 People |
| Year Established | 2018 |
| Main Markets | North America South Asia Western Europe |