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Intel® Cyclone® 10 GX Device Datasheet

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Intel® Cyclone® 10 GX Device Datasheet

This datasheet describes the electrical characteristics, switching characteristics, configuration specifications, and I/O timing for Intel® Cyclone® 10 GX devices.

Intel Cyclone 10 GX devices are offered in extended and industrial grades. Extended devices are offered in –E5 (fastest) and –E6 speed grades. Industrial grade devices are offered in the –I5 and –I6 speed grades.

Related Information

Intel Cyclone 10 GX Device Overview
Provides more information about the densities and packages in the Intel Cyclone 10 GX devices.

Electrical Characteristics

The following sections describe the operating conditions and power consumption of Intel Cyclone 10 GX devices.

Operating Conditions

Intel Cyclone 10 GX devices are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of the Intel Cyclone 10 GX devices, you must consider the operating requirements described in this section.

Absolute Maximum Ratings

This section defines the maximum operating conditions for Intel Cyclone 10 GX devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied for these conditions.

Caution: Conditions outside the range listed in the following table may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

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Table 1. Absolute Maximum Ratings for Intel Cyclone 10 GX Devices

Symbol	Description	Condition	Minimum	Maximum	Unit
V_{CC}	Core voltage power supply	—	–0.50	1.21	V
V_{CCP}	Periphery circuitry and transceiver fabric interface power supply	—	–0.50	1.21	V
V_{CCERAM}	Embedded memory power supply	—	–0.50	1.36	V
V_{CCPT}	Power supply for programmable power technology and I/O pre-driver	—	–0.50	2.46	V
V_{CCBAT}	Battery back-up power supply for design security volatile key register	—	–0.50	2.46	V
V_{CCPGM}	Configuration pins power supply	(1)	–0.50	2.46	V
V_{CCIO}	I/O buffers power supply	3 V I/O	–0.50	4.10	V
		LVDS I/O	–0.50	2.46	V
V_{CCA_PLL}	Phase-locked loop (PLL) analog power supply	—	–0.50	2.46	V
V_{CCT_GXB}	Transmitter power supply	—	–0.50	1.34	V
V_{CCR_GXB}	Receiver power supply	—	–0.50	1.34	V
V_{CCH_GXB}	Transceiver output buffer power supply	—	–0.50	2.46	V

continued...

(1) The LVDS I/O values are applicable to all dedicated and dual-function configuration I/Os.

Symbol	Description	Condition	Minimum	Maximum	Unit
I_{OUT}	DC output current per pin	—	–25 (2)(3)(4)(5)(6)	25	mA
T_J	Operating junction temperature	—	–55	125	°C
T_{STG}	Storage temperature (no bias)	—	–65	150	°C

Related Information

- AN 692: Power Sequencing Considerations for Intel Cyclone 10 GX, Intel Arria 10, and Intel Stratix 10 Devices
  Provides the power sequencing requirements for Intel Cyclone 10 GX devices.
- Power-Up and Power-Down Sequences, Power Management in Intel Cyclone 10 GX Devices chapter
  Provides the power sequencing requirements for Intel Cyclone 10 GX devices.

Maximum Allowed Overshoot and Undershoot Voltage

During transitions, input signals may overshoot to the voltage listed in the following table and undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% duty cycle.

For example, a signal that overshoots to 2.70 V for LVDS I/O can only be at 2.70 V for ~4% over the lifetime of the device.

---

(2) The maximum current allowed through any LVDS I/O bank pin when the device is not turned on or during power-up/power-down conditions is 10 mA.

(3) Total current per LVDS I/O bank must not exceed 100 mA.

(4) Voltage level must not exceed 1.89 V.

(5) Applies to all I/O standards and settings supported by LVDS I/O banks, including single-ended and differential I/Os.

(6) Applies only to LVDS I/O banks. 3 V I/O banks are not covered under this specification and must be implemented as per the power sequencing requirement. For more details, refer to *AN 692: Power Sequencing Considerations for Intel Cyclone 10 GX, Intel Arria® 10, and Intel Stratix® 10 Devices* and *Power Management in Intel Cyclone 10 GX Devices chapter*.

Table 2. Maximum Allowed Overshoot During Transitions for Intel Cyclone 10 GX Devices

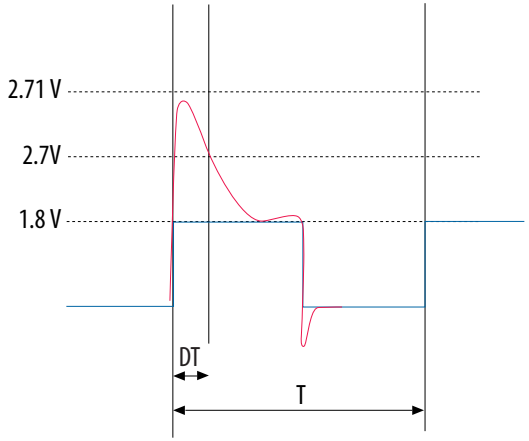
This table lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime. The LVDS I/O values are applicable to the VREFP_ADC and VREFN_ADC I/O pins.

Symbol	Description	Condition (V)		Overshoot Duration as % at T_J = 100°C	Unit
		LVDS I/O [7]	3 V I/O		
V_i (AC)	AC input voltage	2.50	3.80	100	%
		2.55	3.85	42	%
		2.60	3.90	18	%
		2.65	3.95	9	%
		2.70	4.00	4	%
		> 2.70	> 4.00	No overshoot allowed	%

For an overshoot of 2.5 V, the percentage of high time for the overshoot can be as high as 100% over a 10-year period. Percentage of high time is calculated as ([delta T]/T) × 100. This 10-year period assumes that the device is always turned on with 100% I/O toggle rate and 50% duty cycle signal.

(7) The LVDS I/O values are applicable to all dedicated and dual-function configuration I/Os.

Figure 1. Intel Cyclone 10 GX Devices Overshoot Duration



Recommended Operating Conditions

This section lists the functional operation limits for the AC and DC parameters for Intel Cyclone 10 GX devices.

Recommended Operating Conditions

Table 3. Recommended Operating Conditions for Intel Cyclone 10 GX Devices

This table lists the steady-state voltage values expected from Intel Cyclone 10 GX devices. Power supply ramps must all be strictly monotonic, without plateaus.

Symbol	Description	Condition	Minimum [8]	Typical	Maximum [8]	Unit
V_{CC}	Core voltage power supply	—	0.87	0.9	0.93	V
V_{CCP}	Periphery circuitry and transceiver fabric interface power supply	—	0.87	0.9	0.93	V
V_{CCPGM}	Configuration pins power supply	1.8 V	1.71	1.8	1.89	V
		1.5 V	1.425	1.5	1.575	V

continued...

(8) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

Symbol	Description	Condition	Minimum [8]	Typical	Maximum [8]	Unit
		1.2 V	1.14	1.2	1.26	V
V_{CCERAM}	Embedded memory power supply	0.9 V	0.87	0.9	0.93	V
V_{CCBAT} [9]	Battery back-up power supply (For design security volatile key register)	1.8 V	1.71	1.8	1.89	V
		1.2 V	1.14	1.2	1.26	V
V_{CCPT}	Power supply for programmable power technology and I/O pre-driver	1.8 V	1.71	1.8	1.89	V
V_{CCIO}	I/O buffers power supply	3.0 V (for 3 V I/O only)	2.85	3.0	3.15	V
		2.5 V (for 3 V I/O only)	2.375	2.5	2.625	V
		1.8 V	1.71	1.8	1.89	V
		1.5 V	1.425	1.5	1.575	V
		1.35 V	[10]	1.35	[10]	V
		1.25 V	1.19	1.25	1.31	V
		1.2 V	[10]	1.2	[10]	V
V_{CCA_PLL}	PLL analog voltage regulator power supply	—	1.71	1.8	1.89	V
V_{REFP_ADC}	Precision voltage reference for voltage sensor	—	1.2475	1.25	1.2525	V

continued...

(8) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

(9) If you do not use the design security feature in Intel Cyclone 10 GX devices, connect V_{CCBAT} to a 1.5-V to 1.8-V power supply. Intel Cyclone 10 GX power-on reset (POR) circuitry monitors V_{CCBAT}. Intel Cyclone 10 GX devices do not exit POR if V_{CCBAT} is not powered up.

(10) For minimum and maximum voltage values, refer to the I/O Standard Specifications section.

Symbol	Description	Condition	Minimum [8]	Typical	Maximum [8]	Unit
V_I [11][12]	DC input voltage	3 V I/O	–0.3	—	3.3	V
		LVDS I/O	–0.3	—	2.19	V
V_O	Output voltage	—	0	—	V_{CCIO}	V
T_J	Operating junction temperature	Extended	0	—	100	°C
		Industrial	–40	—	100	°C
t_{RAMP} [13]	Power supply ramp time	Standard POR	200 µs	—	100 ms	—
		Fast POR	200 µs	—	4 ms	—

Related Information

I/O Standard Specifications on page 15

Transceiver Power Supply Operating Conditions

Table 4. Transceiver Power Supply Operating Conditions for Intel Cyclone 10 GX Devices

Symbol	Description	Condition	Minimum [14]	Typical	Maximum [14]	Unit
$V_{CCT_GXB[L1][C,D]}$	Transmitter power supply	Chip-to-chip ≤ 12.5 Gbps Or	1.0	1.03	1.06	V

continued...

(8) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

(11) The LVDS I/O values are applicable to all dedicated and dual-function configuration I/Os.

(12) This value applies to both input and tri-stated output configuration. Pin voltage should not be externally pulled higher than the maximum value.

(13) t_{ramp} is the ramp time of each individual power supply, not the ramp time of all combined power supplies.

(14) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

Symbol	Description	Condition	Minimum (14)	Typical	Maximum (14)	Unit
		Backplane ≤ 6.6 Gbps				
		Chip-to-chip ≤ 11.3 Gbps	0.92	0.95	0.98	V
$V_{CCR_GXB[L1][C,D]}$	Receiver power supply	Chip-to-chip ≤ 12.5 Gbps Or Backplane ≤ 6.6 Gbps	1.0	1.03	1.06	V
		Chip-to-chip ≤ 11.3 Gbps	0.92	0.95	0.98	V
V_{CCH_GXBL}	Transceiver output buffer power supply	—	1.710	1.8	1.890	V

Related Information

- Transceiver Performance for Intel Cyclone 10 GX Devices on page 21
- Intel Cyclone 10 GX Pin Connection Guidelines

DC Characteristics

Supply Current and Power Consumption

Intel offers two ways to estimate power for your design—the Excel-based Early Power Estimator (EPE) and the Intel Quartus® Prime Power Analyzer feature.

Use the Excel-based EPE before you start your design to estimate the supply current for your design. The EPE provides a magnitude estimate of the device power because these currents vary greatly with the usage of the resources.

The Intel Quartus Prime Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yield very accurate power estimates.

(14) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

Related Information

- Early Power Estimator User Guide
  Provides more information about power estimation tools.
- Power Analysis and Optimization User Guide: Intel Quartus Prime Pro Edition
  Provides more information about power estimation tools.

I/O Pin Leakage Current

Table 5. I/O Pin Leakage Current for Intel Cyclone 10 GX Devices

If $V_O = V_{CCIO}$ to $V_{CCIOMAX}$, 300 µA of leakage current per I/O is expected.

Symbol	Description	Condition	Min	Max	Unit
I_I	Input pin	V_I = 0 V to $V_{CCIOMAX}$	–80	80	µA
I_{OZ}	Tri-stated I/O pin	V_O = 0 V to $V_{CCIOMAX}$	–80	80	µA

Bus Hold Specifications

The bus-hold trip points are based on calculated input voltages from the JEDEC standard.

Table 6. Bus Hold Parameters for Intel Cyclone 10 GX Devices

Parameter	Symbol	Condition	V_{CCIO} (V)										Unit
			1.2		1.5		1.8		2.5		3.0		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Bus-hold, low, sustaining current	I_{SUSL}	$V_{IN} > V_{IL}$ (max)	8 [15], 26 [16]	—	12 [15], 32 [16]	—	30 [15], 55 [16]	—	60	—	70	—	µA
Bus-hold, high, sustaining current	I_{SUSH}	$V_{IN} < V_{IH}$ (min)	–8 [15], –26 [16]	—	–12 [15], –32 [16]	—	–30 [15], –55 [16]	—	–60	—	–70	—	µA

continued...

(15) This value is only applicable for LVDS I/O bank.

(16) This value is only applicable for 3 V I/O bank.

Parameter	Symbol	Condition	V_{CCIO} (V)										Unit
			1.2		1.5		1.8		2.5		3.0		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Bus-hold, low, overdrive current	I_{ODL}	0 V < V_{IN} < V_{CCIO}	—	125	—	175	—	200	—	300	—	500	µA
Bus-hold, high, overdrive current	I_{ODH}	0 V < V_{IN} < V_{CCIO}	—	–125	—	–175	—	–200	—	–300	—	–500	µA
Bus-hold trip point	V_{TRIP}	—	0.3	0.9	0.38	1.13	0.68	1.07	0.70	1.7	0.8	2	V

OCT Calibration Accuracy Specifications

If you enable on-chip termination (OCT) calibration, calibration is automatically performed at power up for I/Os connected to the calibration block.

Table 7. OCT Calibration Accuracy Specifications for Intel Cyclone 10 GX Devices

Calibration accuracy for the calibrated on-chip series termination (R_S OCT) and on-chip parallel termination (R_T OCT) are applicable at the moment of calibration. When process, voltage, and temperature (PVT) conditions change after calibration, the tolerance may change.

Symbol	Description	Condition (V)	Resistance Tolerance		Unit
			–E5, –I5	–E6, –I6	
25-Ω and 50-Ω R_S	Internal series termination with calibration (25-Ω and 50-Ω setting)	V_{CCIO} = 1.8, 1.5, 1.2	± 15	± 15	%
34-Ω and 40-Ω R_S	Internal series termination with calibration (34-Ω and 40-Ω setting)	V_{CCIO} = 1.5, 1.25, 1.2	± 15	± 15	%
		V_{CCIO} = 1.35	± 20	± 20	%
48-Ω, 60-Ω, 80-Ω, and 120-Ω R_S	Internal series termination with calibration (48-Ω, 60-Ω, 80-Ω, and 120-Ω setting)	V_{CCIO} = 1.2	± 15	± 15	%
240-Ω R_S	Internal series termination with calibration (240-Ω setting)	V_{CCIO} = 1.2	± 20	± 20	%
30-Ω R_T	Internal parallel termination with calibration (30-Ω setting)	V_{CCIO} = 1.5, 1.35, 1.25	–10 to +40	–10 to +40	%
34-Ω, 48-Ω, 80-Ω, and 240-Ω R_T	Internal parallel termination with calibration (34-Ω, 48-Ω, 80-Ω, and 240-Ω setting)	V_{CCIO} = 1.2	± 15	± 15	%

continued...

Symbol	Description	Condition (V)	Resistance Tolerance		Unit
			–E5, –I5	–E6, –I6	
40-Ω, 60-Ω, and 120-Ω R_T	Internal parallel termination with calibration (40-Ω, 60-Ω, and 120-Ω setting)	V_{CCIO} = 1.5, 1.35, 1.25, 1.2	–10 to +40	–10 to +40	%
		V_{CCIO} = 1.2 [17]	± 15	± 15	%
80-Ω R_T	Internal parallel termination with calibration (80-Ω setting)	V_{CCIO} = 1.2	± 15	± 15	%

Related Information

I/O Standards Support in Intel Cyclone 10 GX Devices

OCT Without Calibration Resistance Tolerance Specifications

Table 8. OCT Without Calibration Resistance Tolerance Specifications for Intel Cyclone 10 GX Devices

This table lists the Intel Cyclone 10 GX OCT without calibration resistance tolerance to PVT changes.

Symbol	Description	Condition (V)	Resistance Tolerance		Unit
			–E5, –I5	–E6, –I6	
25-Ω and 50-Ω R_S	Internal series termination without calibration (25-Ω and 50-Ω setting)	V_{CCIO} = 3.0, 2.5	± 40	± 40	%
		V_{CCIO} = 1.8, 1.5, 1.2	± 50	± 50	%
34-Ω and 40-Ω R_S	Internal series termination without calibration (34-Ω and 40-Ω setting)	V_{CCIO} = 1.5, 1.35, 1.25, 1.2	± 50	± 50	%
48-Ω and 60-Ω R_S	Internal series termination without calibration (48-Ω and 60-Ω setting)	V_{CCIO} = 1.2	± 50	± 50	%
120-Ω R_s	Internal series termination without calibration (120-Ω setting)	V_{CCIO} = 1.2	± 50	± 50	%
100-Ω R_D	Internal differential termination (100-Ω setting)	V_{CCIO} = 1.8	± 35	± 40	%

(17) Only applicable to POD12 I/O standard.

Pin Capacitance

Table 9. Pin Capacitance for Intel Cyclone 10 GX Devices

Symbol	Description	Maximum	Unit
C_{IO_COLUMN}	Input capacitance on column I/O pins	2.5	pF
C_{OUTFB}	Input capacitance on dual-purpose clock output/feedback pins	2.5	pF

Internal Weak Pull-Up and Weak Pull-Down Resistor

All I/O pins, except configuration, test, and JTAG pins, have an option to enable weak pull-up. The weak pull-down feature is only available for the pins as described in the Internal Weak Pull-Down Resistor Values for Intel Cyclone 10 GX Devices table.

Table 10. Internal Weak Pull-Up Resistor Values for Intel Cyclone 10 GX Devices

Symbol	Description	Condition (V) [18]	Value [19]	Unit
R_{PU}	Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if you have enabled the programmable pull-up resistor option.	V_{CCIO} = 3.0 ±5%	25	kΩ
		V_{CCIO} = 2.5 ±5%	25	kΩ
		V_{CCIO} = 1.8 ±5%	25	kΩ
		V_{CCIO} = 1.5 ±5%	25	kΩ
		V_{CCIO} = 1.35 ±5%	25	kΩ
		V_{CCIO} = 1.25 ±5%	25	kΩ
		V_{CCIO} = 1.2 ±5%	25	kΩ

(18) Pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO}.

(19) Valid with ±25% tolerances to cover changes over PVT.

Table 11. Internal Weak Pull-Down Resistor Values for Intel Cyclone 10 GX Devices

Pin Name	Description	Condition (V)	Value (19)	Unit
nIO_PULLUP	Dedicated input pin that determines the internal pull-ups on user I/O pins and dual-purpose I/O pins.	V_{CC} = 0.9 ±3.33%	25	kΩ
TCK	Dedicated JTAG test clock input pin.	V_{CCPGM} = 1.8 ±5 %	25	kΩ
		V_{CCPGM} = 1.5 ±5%	25	kΩ
		V_{CCPGM} = 1.2 ±5%	25	kΩ
MSEL[0:2]	Configuration input pins that set the configuration scheme for the FPGA device.	V_{CCPGM} = 1.8 ±5%	25	kΩ
		V_{CCPGM} = 1.5 ±5%	25	kΩ
		V_{CCPGM} = 1.2 ±5%	25	kΩ

Related Information

Intel Cyclone 10 GX Device Family Pin Connection Guidelines
Provides more information about the pins that support internal weak pull-up and internal weak pull-down features.

I/O Standard Specifications

Tables in this section list the input voltage (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}) for various I/O standards supported by Intel Cyclone 10 GX devices.

For minimum voltage values, use the minimum V_{CCIO} values. For maximum voltage values, use the maximum V_{CCIO} values.

You must perform timing closure analysis to determine the maximum achievable frequency for general purpose I/O standards.

Related Information

Recommended Operating Conditions on page 7

Single-Ended I/O Standards Specifications

Table 12. Single-Ended I/O Standards Specifications for Intel Cyclone 10 GX Devices

I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (20) (mA)	I_{OH} (20) (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
3.0-V LVTTL	2.85	3	3.15	–0.3	0.8	1.7	3.3	0.4	2.4	2	–2
3.0-V LVCMOS	2.85	3	3.15	–0.3	0.8	1.7	3.3	0.2	V_{CCIO} – 0.2	0.1	–0.1
2.5 V	2.375	2.5	2.625	–0.3	0.7	1.7	3.3	0.4	2	1	–1
1.8 V	1.71	1.8	1.89	–0.3	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.3	0.45	V_{CCIO} – 0.45	2	–2
1.5 V	1.425	1.5	1.575	–0.3	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.3	0.25 × V_{CCIO}	0.75 × V_{CCIO}	2	–2
1.2 V	1.14	1.2	1.26	–0.3	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.3	0.25 × V_{CCIO}	0.75 × V_{CCIO}	2	–2

Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications

Table 13. Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Intel Cyclone 10 GX Devices

I/O Standard	V_{CCIO} (V)			V_{REF} (V)			V_{TT} (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-18 Class I, II	1.71	1.8	1.89	0.833	0.9	0.969	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04
SSTL-15 Class I, II	1.425	1.5	1.575	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}
SSTL-135/ SSTL-135 Class I, II	1.283	1.35	1.418	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}
SSTL-125/ SSTL-125 Class I, II	1.19	1.25	1.31	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}
SSTL-12/ SSTL-12 Class I, II	1.14	1.2	1.26	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}

continued...

(20) To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the 3.0-V LVTTL specification (2 mA), you should set the current strength settings to 2 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the datasheet.

I/O Standard	V_{CCIO} (V)			V_{REF} (V)			V_{TT} (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	—	$V_{CCIO}/2$	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.68	0.75	0.9	—	$V_{CCIO}/2$	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.47 × V_{CCIO}	0.5 × V_{CCIO}	0.53 × V_{CCIO}	—	$V_{CCIO}/2$	—
HSUL-12	1.14	1.2	1.3	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	—	—	—
POD12	1.16	1.2	1.24	0.69 × V_{CCIO}	0.7 × V_{CCIO}	0.71 × V_{CCIO}	—	V_{CCIO}	—

Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications

Table 14. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Intel Cyclone 10 GX Devices

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)	V_{OL} (V)	V_{OH} (V)	I_{OL} [21] (mA)	I_{OH} [21] (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
SSTL-18 Class I	–0.3	V_{REF} –0.125	V_{REF} + 0.125	V_{CCIO} + 0.3	V_{REF} – 0.25	V_{REF} + 0.25	V_{TT} – 0.603	V_{TT} + 0.603	6.7	–6.7
SSTL-18 Class II	–0.3	V_{REF} –0.125	V_{REF} + 0.125	V_{CCIO} + 0.3	V_{REF} – 0.25	V_{REF} + 0.25	0.28	V_{CCIO} –0.28	13.4	–13.4
SSTL-15 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.175	V_{REF} + 0.175	0.2 × V_{CCIO}	0.8 × V_{CCIO}	8	–8
SSTL-15 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.175	V_{REF} + 0.175	0.2 × V_{CCIO}	0.8 × V_{CCIO}	16	–16
SSTL-135/ SSTL-135 Class I, II	—	V_{REF} – 0.09	V_{REF} + 0.09	—	V_{REF} – 0.16	V_{REF} + 0.16	0.2 × V_{CCIO}	0.8 × V_{CCIO}	—	—
SSTL-125/ SSTL-125 Class I, II	—	V_{REF} – 0.09	V_{REF} + 0.09	—	V_{REF} – 0.15	V_{REF} + 0.15	0.2 × V_{CCIO}	0.8 × V_{CCIO}	—	—

continued...

(21) To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the SSTL15CI specification (8 mA), you should set the current strength settings to 8 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the datasheet.

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)	V_{OL} (V)	V_{OH} (V)	I_{OL} [21] (mA)	I_{OH} [21] (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
SSTL-12/ SSTL-12 Class I, II	—	V_{REF} – 0.10	V_{REF} + 0.10	—	V_{REF} – 0.15	V_{REF} + 0.15	0.2 × V_{CCIO}	0.8 × V_{CCIO}	—	—
HSTL-18 Class I	—	V_{REF} –0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	8	–8
HSTL-18 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	16	–16
HSTL-15 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	8	–8
HSTL-15 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} –0.4	16	–16
HSTL-12 Class I	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	V_{REF} – 0.15	V_{REF} + 0.15	0.25 × V_{CCIO}	0.75 × V_{CCIO}	8	–8
HSTL-12 Class II	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	V_{REF} – 0.15	V_{REF} + 0.15	0.25 × V_{CCIO}	0.75 × V_{CCIO}	16	–16
HSUL-12	—	V_{REF} – 0.13	V_{REF} + 0.13	—	V_{REF} – 0.22	V_{REF} + 0.22	0.1 × V_{CCIO}	0.9 × V_{CCIO}	—	—
POD12	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	V_{REF} – 0.15	V_{REF} + 0.15	(0.7 – 0.15) × V_{CCIO}	(0.7 + 0.15) × V_{CCIO}	—	—

Differential SSTL I/O Standards Specifications

Table 15. Differential SSTL I/O Standards Specifications for Intel Cyclone 10 GX Devices

I/O Standard	V_{CCIO} (V)			$V_{SWING(DC)}$ (V)		$V_{SWING(AC)}$ (V)		$V_{IX(AC)}$ (V)		
	Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max
SSTL-18 Class I, II	1.71	1.8	1.89	0.25	V_{CCIO} + 0.6	0.5	V_{CCIO} + 0.6	$V_{CCIO}/2$ – 0.175	—	$V_{CCIO}/2$ + 0.175
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	[22]	2($V_{IH(AC)}$ – V_{REF})	2(V_{REF} – $V_{IL(AC)}$)	$V_{CCIO}/2$ – 0.15	—	$V_{CCIO}/2$ + 0.15

continued...

(21) To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the SSTL15CI specification (8 mA), you should set the current strength settings to 8 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the datasheet.

I/O Standard	V_{CCIO} (V)			$V_{SWING(DC)}$ (V)		$V_{SWING(AC)}$ (V)		$V_{IX(AC)}$ (V)		
	Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max
SSTL-135/ SSTL-135 Class I, II	1.283	1.35	1.45	0.18	(22)	$2(V_{IH(AC)} - V_{REF})$	$2(V_{IL(AC)} - V_{REF})$	$V_{CCIO}/2 - 0.15$	$V_{CCIO}/2$	$V_{CCIO}/2 + 0.15$
SSTL-125/ SSTL-125 Class I, II	1.19	1.25	1.31	0.18	(22)	$2(V_{IH(AC)} - V_{REF})$	$2(V_{IL(AC)} - V_{REF})$	$V_{CCIO}/2 - 0.15$	$V_{CCIO}/2$	$V_{CCIO}/2 + 0.15$
SSTL-12/ SSTL-12 Class I, II	1.14	1.2	1.26	0.16	(22)	$2(V_{IH(AC)} - V_{REF})$	$2(V_{IL(AC)} - V_{REF})$	$V_{REF} - 0.15$	$V_{CCIO}/2$	$V_{REF} + 0.15$
POD12	1.16	1.2	1.24	0.16	—	0.3	—	$V_{REF} - 0.08$	—	$V_{REF} + 0.08$

Differential HSTL and HSUL I/O Standards Specifications

Table 16. Differential HSTL and HSUL I/O Standards Specifications for Intel Cyclone 10 GX Devices

I/O Standard	V_{CCIO} (V)			$V_{DIF(DC)}$ (V)		$V_{DIF(AC)}$ (V)		$V_{IX(AC)}$ (V)			$V_{CM(DC)}$ (V)		
	Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max	Min	Typ	Max
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	—	0.4	—	0.78	—	1.12	0.78	—	1.12
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.4	—	0.68	—	0.9	0.68	—	0.9
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	$V_{CCIO} + 0.3$	0.3	$V_{CCIO} + 0.48$	—	$0.5 \times V_{CCIO}$	—	$0.4 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.6 \times V_{CCIO}$
HSUL-12	1.14	1.2	1.3	$2(V_{IH(DC)} - V_{REF})$	$2(V_{REF} - V_{IH(DC)})$	$2(V_{IH(AC)} - V_{REF})$	$2(V_{REF} - V_{IH(AC)})$	$0.5 \times V_{CCIO} - 0.12$	$0.5 \times V_{CCIO}$	$0.5 \times V_{CCIO} + 0.12$	$0.4 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.6 \times V_{CCIO}$

(22) The maximum value for $V_{SWING(DC)}$ is not defined. However, each single-ended signal needs to be within the respective single-ended limits ($V_{IH(DC)}$ and $V_{IL(DC)}$).

Differential I/O Standards Specifications

Table 17. Differential I/O Standards Specifications for Intel Cyclone 10 GX Devices

Differential inputs are powered by V_{CCPT} which requires 1.8 V.

I/O Standard	V_{CCIO} (V)			V_{ID} (mV) (23)			$V_{ICM(DC)}$ (V)			V_{OD} (V) (24)			V_{OCM} (V) (24)		
	Min	Typ	Max	Min	Condition	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
LVDS (25)	1.71	1.8	1.89	100	V_{CM} = 1.25 V	—	0	D_{MAX} ≤700 Mbps	1.85	0.247	—	0.6	1.125	1.25	1.375
							1	D_{MAX} >700 Mbps	1.6						
RSDS (HIO) (26)	1.71	1.8	1.89	100	V_{CM} = 1.25 V	—	0.3	—	1.4	0.1	0.2	0.6	0.5	1.2	1.4
Mini-LVDS (HIO) (27)	1.71	1.8	1.89	200	—	600	0.4	—	1.325	0.25	—	0.6	1	1.2	1.4
LVPECL (28)	1.71	1.8	1.89	300	—	—	0.6	D_{MAX} ≤700 Mbps	1.7	—	—	—	—	—	—
							1	D_{MAX} >700 Mbps	1.6						

Related Information

Transceiver Specifications for Intel Cyclone 10 GX Devices on page 22
Provides the specifications for transmitter, receiver, and reference clock I/O pin.

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(23) The minimum V_{ID} value is applicable over the entire common mode range, V_{CM}.

(24) R_L range: $90 \leq R_L \leq 110\ \Omega$.

(25) For optimized LVDS receiver performance, the receiver voltage input range must be within 1.0 V to 1.6 V for data rates above 700 Mbps and 0 V to 1.85 V for data rates below 700 Mbps.

(26) For optimized RSDS receiver performance, the receiver voltage input range must be within 0.25 V to 1.45 V.

(27) For optimized Mini-LVDS receiver performance, the receiver voltage input range must be within 0.3 V to 1.425 V.

(28) For optimized LVPECL receiver performance, the receiver voltage input range must be within 0.85 V to 1.75 V for data rates above 700 Mbps and 0.45 V to 1.95 V for data rates below 700 Mbps.

Switching Characteristics

This section provides the performance characteristics of Intel Cyclone 10 GX core and periphery blocks for extended grade devices.

Transceiver Performance Specifications

Transceiver Performance for Intel Cyclone 10 GX Devices

Table 18. Transmitter and Receiver Data Rate Performance

Symbol/Description	Condition	Datarate	Unit
Chip-to-Chip [29]	Maximum data rate $V_{CCR_GXB} = V_{CCT_GXB} = 1.03$ V	12.5	Gbps
	Maximum data rate $V_{CCR_GXB} = V_{CCT_GXB} = 0.95$ V	11.3	Gbps
	Minimum Data Rate	1.0 [30]	Gbps
Backplane	Maximum data rate $V_{CCR_GXB} = V_{CCT_GXB} = 1.03$ V	6.6	Gbps
	Minimum Data Rate	1.0 [30]	Gbps

Table 19. ATX PLL and Fractional PLL (fPLL) Performance

Symbol/Description	Condition	Frequency	Unit
Supported Output Frequency	Maximum Frequency	6.25	GHz
	Minimum Frequency	500	MHz

(29) Chip-to-chip links are applications with short reach channels.

(30) Intel Cyclone 10 GX transceivers can support data rates down to 125 Mbps with over sampling. You must create your own over sampling logic.

Table 20. CMU PLL Performance

Symbol/Description	Condition	Frequency	Unit
Supported Output Frequency	Maximum Frequency	5.15625	GHz
	Minimum Frequency	2450	MHz

Related Information

Transceiver Power Supply Operating Conditions on page 9

High-Speed Serial Transceiver-Fabric Interface Performance for Intel Cyclone 10 GX Devices

Table 21. High-Speed Serial Transceiver-Fabric Interface Performance for Intel Cyclone 10 GX Devices

The frequencies listed are the maximum frequencies.

Symbol/Description	Condition (V)	Core Speed Grade		Unit
		-5	-6	
20-bit interface - FIFO	V_{CC} = 0.9	400	400	MHz
20-bit interface - Registered	V_{CC} = 0.9	400	400	MHz
32-bit interface - FIFO	V_{CC} = 0.9	404	335	MHz
32-bit interface - Registered	V_{CC} = 0.9	404	335	MHz
64-bit interface - FIFO	V_{CC} = 0.9	234	222	MHz
64-bit interface - Registered	V_{CC} = 0.9	234	222	MHz

Transceiver Specifications for Intel Cyclone 10 GX Devices

Table 22. Reference Clock Specifications

Symbol/Description	Condition	Min	Typ	Max	Unit
Supported I/O Standards	Dedicated reference clock pin	CML, Differential LVPECL, LVDS, and HCSL [31]			
	RX pin as a reference clock	CML, Differential LVPECL, and LVDS			

continued...

[31] HCSL is only supported for PCIe.

Symbol/Description	Condition	Min	Typ	Max	Unit
Input Reference Clock Frequency (CMU PLL)		61	—	800	MHz
Input Reference Clock Frequency (ATX PLL)		100	—	800	MHz
Input Reference Clock Frequency (fPLL PLL)		25 [32] / 50	—	800	MHz
Rise time	20% to 80%	—	—	400	ps
Fall time	80% to 20%	—	—	400	ps
Duty cycle	—	45	—	55	%
Spread-spectrum modulating clock frequency	PCIe	30	—	33	kHz
Spread-spectrum downspread	PCIe	—	0 to –0.5	—	%
On-chip termination resistors	—	—	100	—	Ω
Absolute V_{MAX}	Dedicated reference clock pin	—	—	1.6	V
	RX pin as a reference clock	—	—	1.2	V
Absolute V_{MIN}	—	–0.4	—	—	V
Peak-to-peak differential input voltage	—	200	—	1600	mV
V_{ICM} (AC coupled)	V_{CCR_GXB} = 0.95 V	—	0.95	—	V
	V_{CCR_GXB} = 1.03 V	—	1.03	—	V
V_{ICM} (DC coupled)	HCSL I/O standard for PCIe reference clock	250	—	550	mV
Transmitter REFCLK Phase Noise (622 MHz) [33]	100 Hz	—	—	–70	dBc/Hz
	1 kHz	—	—	–90	dBc/Hz

continued...

(32) 25 MHz is for HDMI applications only.

(33) To calculate the REFCLK phase noise requirement at frequencies other than 622 MHz, use the following formula: REFCLK phase noise at f (MHz) = REFCLK phase noise at 622 MHz + 20*log(f/622).

Symbol/Description	Condition	Min	Typ	Max	Unit
	10 kHz	—	—	–100	dBc/Hz
	100 kHz	—	—	–110	dBc/Hz
	≥ 1 MHz	—	—	–120	dBc/Hz
Transmitter REFCLK Phase Jitter (100 MHz)	1.5 MHz to 100 MHz (PCIe)	—	—	4.2	ps (rms)
R_{REF}	—	—	2.0 k ±1%	—	Ω
Maximum rate of change of the reference clock frequency $T_{SSC\text{-}MAX\text{-}PERIOD\text{-}SLEW}$ (34)	Max SSC df/dt			0.75	ps/UI

Table 23. Transceiver Clocks Specifications

Symbol/Description	Condition	Min	Typ	Max	Unit
CLKUSR pin for transceiver calibration	Transceiver Calibration	100	—	125	MHz
`reconfig_clk`	Reconfiguration interface	100	—	125	MHz

Table 24. Transceiver Clock Network Maximum Data Rate Specifications

Clock Network	Maximum Performance			Channel Span	Unit
	ATX	fPLL	CMU		
x1	12.5	12.5	10.3125	6 channels in a single bank	Gbps
x6	12.5	12.5	N/A	6 channels in a single bank	Gbps
PLL feedback compensation mode	12.5	12.5	N/A	Side-wide	Gbps
xN at 1.03 V V_{CCR_GXB}/ V_{CCT_GXB}	12.5	12.5	N/A	Side-wide	Gbps
xN at 0.95 V V_{CCR_GXB}/ V_{CCT_GXB}	10.5	10.5	N/A	Side-wide	Gbps

(34) Defined for worst case spread spectrum clock (SSC) modulation profile, such as Lexmark.

Table 25. Receiver Specifications

Symbol/Description	Condition	Min	Typ	Max	Unit
Supported I/O Standards	—	High Speed Differential I/O, CML , Differential LVPECL , and LVDS[35]			
Absolute V_{MAX} for a receiver pin [36]	—	—	—	1.2	V
Absolute V_{MIN} for a receiver pin [37]	—	-0.4	—	—	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) before device configuration	—	—	—	1.6	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) after device configuration	V_{CCR_GXB} = 0.95 V	—	—	2.4	V
	V_{CCR_GXB} = 1.03 V	—	—	2.0	V
Minimum differential eye opening at receiver serial input pins [38]	—	50	—	—	mV
Differential on-chip termination resistors	85-Ω setting	—	85 ± 30%	—	Ω
	100-Ω setting	—	100 ± 30%	—	Ω
V_{ICM} (AC and DC coupled) [39]	V_{CCR_GXB} = 0.95 V	—	600	—	mV
	V_{CCR_GXB} = 1.03 V	—	700	—	mV

continued...

(35) CML, Differential LVPECL, and LVDS are only used on AC coupled links.

(36) The device cannot tolerate prolonged operation at this absolute maximum.

(37) The device cannot tolerate prolonged operation at this absolute minimum.

(38) The differential eye opening specification at the receiver input pins assumes that Receiver Equalization is disabled. If you enable Receiver Equalization, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.

(39) Intel Cyclone 10 GX devices support DC coupling to other Intel Cyclone 10 GX devices and other devices with a transmitter that has matching common mode voltage.

Symbol/Description	Condition	Min	Typ	Max	Unit
t_{LTR} (40)	—	—	—	10	µs
t_{LTD} (41)	—	4	—	—	µs
t_{LTD_manual} (42)	—	4	—	—	µs
$t_{LTR_LTD_manual}$ (43)	—	15	—	—	µs
Run Length	—	—	—	200	UI
CDR PPM tolerance	PCIe-only	-300	—	300	PPM
	All other protocols	-1000	—	1000	PPM
Programmable DC Gain	Setting = 0-4	0	—	10	dB
Programmable AC Gain at High Gain mode and Data Rate ≤ 6 Gbps	Setting = 0-28 V_{CCR_GXB} = 0.95 V	0	—	19	dB
	Setting = 0-28 V_{CCR_GXB} = 1.03 V	0	—	21	dB

Table 26. Transmitter Specifications

Symbol/Description	Condition	Min	Typ	Max	Unit
Supported I/O Standards	—	High Speed Differential I/O (44)			—
Differential on-chip termination resistors	85-Ω setting	—	85 ± 20%	—	Ω

continued...

(40) t_{LTR} is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.

(41) t_{LTD} is time required for the receiver CDR to start recovering valid data after the `rx_is_lockedtodata` signal goes high.

(42) t_{LTD_manual} is the time required for the receiver CDR to start recovering valid data after the `rx_is_lockedtodata` signal goes high when the CDR is functioning in the manual mode.

(43) $t_{LTR_LTD_manual}$ is the time the receiver CDR must be kept in lock to reference (LTR) mode after the `rx_is_lockedtoref` signal goes high when the CDR is functioning in the manual mode.

(44) High Speed Differential I/O is the dedicated I/O standard for the transmitter in Intel Cyclone 10 GX transceivers.

Symbol/Description	Condition	Min	Typ	Max	Unit
	100-Ω setting	—	100 ± 20%	—	Ω
V_{OCM} (AC coupled)	V_{CCT_GXB} = 0.95 V	—	450	—	mV
	V_{CCT_GXB} = 1.03 V	—	500	—	mV
V_{OCM} (DC coupled)	V_{CCT_GXB} = 0.95 V	—	450	—	mV
	V_{CCT_GXB} = 1.03 V	—	500	—	mV
Rise time [45]	20% to 80%	20	—	130	ps
Fall time [45]	80% to 20%	20	—	130	ps
Intra-differential pair skew	TX V_{CM} = 0.5 V and slew rate setting of SLEW_R5 [46]	—	—	15	ps

Table 27. Typical Transmitter V_{OD} Settings

Symbol	V_{OD} Setting	V_{OD}-to-V_{CCT_GXB} Ratio
V_{OD} differential value = V_{OD}-to-V_{CCT_GXB} ratio x V_{CCT_GXB}	31	1.00
	30	0.97
	29	0.93
	28	0.90
	27	0.87
	26	0.83
	25	0.80
	24	0.77
	23	0.73
	22	0.70

continued...

(45) The Intel Quartus Prime software automatically selects the appropriate slew rate depending on the design configurations.

(46) SLEW_R1 is the slowest and SLEW_R5 is the fastest. SLEW_R6 and SLEW_R7 are not used.

Symbol	V_{OD} Setting	V_{OD}-to-V_{CCT_GXB} Ratio
	21	0.67
	20	0.63
	19	0.60
	18	0.57
	17	0.53
	16	0.50
	15	0.47
	14	0.43
	13	0.40
	12	0.37

Table 28. Transmitter Channel-to-channel Skew Specifications

Mode	Channel Span	Maximum Skew	Unit
x6 Clock	Up to 6 channels in one bank	61	ps
xN Clock	Within 2 banks	230	ps
PLL Feedback Compensation [47], [48]	Side-wide	1600	ps

Related Information

PLLs and Clock Networks

(47) `refclk` is set to 125 MHz during the test.

(48) You can reduce the lane-to-lane skew by increasing the reference clock frequency.

Core Performance Specifications

Clock Tree Specifications

Table 29. Clock Tree Performance for Intel Cyclone 10 GX Devices

Parameter	Performance (All Speed Grades)	Unit
Global clock, regional clock, and small periphery clock	644	MHz
Large periphery clock	525	MHz

PLL Specifications

Fractional PLL Specifications

Table 30. Fractional PLL Specifications for Intel Cyclone 10 GX Devices

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{IN}	Input clock frequency	—	30	—	800 (49)	MHz
f_{INPFD}	Input clock frequency to the phase frequency detector (PFD)	—	30	—	700	MHz
f_{CASC_INPFD}	Input clock frequency to the PFD of destination cascade PLL	—	30	—	60	MHz
f_{VCO}	PLL voltage-controlled oscillator (VCO) operating range	—	6	—	12.5	GHz
$t_{EINDUTY}$	Input clock duty cycle	—	45	—	55	%
f_{OUT}	Output frequency for internal global or regional clock	—	—	—	644	MHz
$f_{DYCONFIGCLK}$	Dynamic configuration clock for `reconfig_clk`	—	—	—	100	MHz

continued...

(49) This specification is limited by the I/O maximum frequency. The maximum achievable I/O frequency is different for each I/O standard and is depends on design and system specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{LOCK}	Time required to lock from end-of-device configuration or deassertion of `pll_powerdown`	—	—	—	1	ms
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)	—	—	—	1	ms
f_{CLBW}	PLL closed-loop bandwidth	—	0.3	—	4	MHz
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	—	—	50	ps
t_{ARESET}	Minimum pulse width on the `pll_powerdown` signal	—	10	—	—	ns
t_{INCCJ} (50)(51)	Input clock cycle-to-cycle jitter	$F_{REF} \geq 100$ MHz	—	—	0.13	UI (p-p)
		$F_{REF} < 100$ MHz	—	—	650	ps (p-p)
t_{OUTPJ} (52)	Period jitter for clock output	$F_{OUT} \geq 100$ MHz	—	—	600	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	60	mUI (p-p)
t_{OUTCCJ} (52)	Cycle-to-cycle jitter for clock output	$F_{OUT} \geq 100$ MHz	—	—	600	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	60	mUI (p-p)
dK_{BIT}	Bit number of Delta Sigma Modulator (DSM)	—	—	32	—	bit

Related Information

Memory Output Clock Jitter Specifications on page 43
Provides more information about the external memory interface clock output jitter specifications.

(50) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source with jitter < 120 ps.

(51) F_{REF} is f_{IN}/N, specification applies when $N = 1$.

(52) External memory interface clock output jitter specifications use a different measurement method, which are available in Memory Output Clock Jitter Specification for Intel Cyclone 10 GX Devices table.

I/O PLL Specifications

Table 31. I/O PLL Specifications for Intel Cyclone 10 GX Devices

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{IN}	Input clock frequency	–5 speed grade	10	—	700 (53)	MHz
		–6 speed grade	10	—	650 (53)	MHz
f_{INPFD}	Input clock frequency to the PFD	—	10	—	325	MHz
f_{CASC_INPFD}	Input clock frequency to the PFD of destination cascade PLL	—	10	—	60	MHz
f_{VCO}	PLL VCO operating range	–5 speed grade	600	—	1434	MHz
		–6 speed grade	600	—	1250	MHz
f_{CLBW}	PLL closed-loop bandwidth	—	0.1	—	8	MHz
$t_{EINDUTY}$	Input clock or external feedback clock input duty cycle	—	40	—	60	%
f_{OUT}	Output frequency for internal global or regional clock (C counter)	–5, –6 speed grade	—	—	644	MHz
f_{OUT_EXT}	Output frequency for external clock output	–5 speed grade	—	—	720	MHz
		–6 speed grade	—	—	650	MHz
$t_{OUTDUTY}$	Duty cycle for dedicated external clock output (when set to 50%)	—	45	50	55	%
t_{FCOMP}	External feedback clock compensation time	—	—	—	10	ns
$f_{DYCONFIGCLK}$	Dynamic configuration clock for `mgmt_clk` and `scanclk`	—	—	—	100	MHz
t_{LOCK}	Time required to lock from end-of-device configuration or deassertion of `areset`	—	—	—	1	ms

continued...

(53) This specification is limited by the I/O maximum frequency. The maximum achievable I/O frequency is different for each I/O standard and is depends on design and system specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)	—	—	—	1	ms
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	—	—	±50	ps
t_{ARESET}	Minimum pulse width on the `areset` signal	—	10	—	—	ns
t_{INCCJ} (54)(55)	Input clock cycle-to-cycle jitter	$F_{REF} \geq 100$ MHz	—	—	0.15	UI (p-p)
		$F_{REF} < 100$ MHz	—	—	750	ps (p-p)
t_{OUTPJ_DC}	Period jitter for dedicated clock output	$F_{OUT} \geq 100$ MHz	—	—	175	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	17.5	mUI (p-p)
t_{OUTCCJ_DC}	Cycle-to-cycle jitter for dedicated clock output	$F_{OUT} \geq 100$ MHz	—	—	175	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	17.5	mUI (p-p)
t_{OUTPJ_IO} (56)	Period jitter for clock output on the regular I/O	$F_{OUT} \geq 100$ MHz	—	—	600	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	60	mUI (p-p)
t_{OUTCCJ_IO} (56)	Cycle-to-cycle jitter for clock output on the regular I/O	$F_{OUT} \geq 100$ MHz	—	—	600	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	60	mUI (p-p)
$t_{CASC_OUTPJ_DC}$	Period jitter for dedicated clock output in cascaded PLLs	$F_{OUT} \geq 100$ MHz	—	—	175	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	17.5	mUI (p-p)

Related Information

Memory Output Clock Jitter Specifications on page 43
Provides more information about the external memory interface clock output jitter specifications.

(54) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source with jitter < 120 ps.

(55) F_{REF} is f_{IN}/N, specification applies when $N = 1$.

(56) External memory interface clock output jitter specifications use a different measurement method, which are available in Memory Output Clock Jitter Specification for Intel Cyclone 10 GX Devices table.

DSP Block Specifications

Table 32. DSP Block Performance Specifications for Intel Cyclone 10 GX Devices

Mode	Performance				Unit
	–E5	–I5	–E6	–I6	
Fixed-point 18 × 19 multiplication mode	456	438	364	346	MHz
Fixed-point 27 × 27 multiplication mode	450	434	358	344	MHz
Fixed-point 18 × 18 multiplier adder mode	459	440	370	351	MHz
Fixed-point 18 × 18 multiplier adder summed with 36-bit input mode	444	422	349	326	MHz
Fixed-point 18 × 19 systolic mode	459	440	370	351	MHz
Complex 18 × 19 multiplication mode	456	438	364	346	MHz
Floating point multiplication mode	447	427	347	326	MHz
Floating point adder or subtract mode	388	369	288	266	MHz
Floating point multiplier adder or subtract mode	386	368	290	270	MHz
Floating point multiplier accumulate mode	418	393	326	294	MHz
Floating point vector one mode	404	382	306	282	MHz
Floating point vector two mode	383	367	293	278	MHz

Memory Block Specifications

To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL and set to **50%** output duty cycle. Use the Intel Quartus Prime software to report timing for the memory block clocking schemes.

When you use the error detection cyclical redundancy check (CRC) feature, there is no degradation in f_{MAX}.

Table 33. Memory Block Performance Specifications for Intel Cyclone 10 GX Devices

Memory	Mode	Performance			
		–E5, –I5	–E6	–I6	Unit
MLAB	Single port, all supported widths (×16/×32)	570	490	490	MHz
	Simple dual-port, all supported widths (×16/×32)	570	490	490	MHz
	Simple dual-port with the read-during-write option set to **Old Data**, all supported widths	400	330	330	MHz
	ROM, all supported width (×16/×32)	570	490	490	MHz
M20K Block	Single-port, all supported widths	625	530	510	MHz
	Simple dual-port, all supported widths	625	530	510	MHz
	Simple dual-port with the read-during-write option set to **Old Data**, all supported widths	470	410	410	MHz
	Simple dual-port with ECC enabled, 512 × 32	410	360	360	MHz
	Simple dual-port with ECC and optional pipeline registers enabled, 512 × 32	520	470	470	MHz
	True dual port, all supported widths	600	480	480	MHz
	ROM, all supported widths	625	530	510	MHz

Temperature Sensing Diode Specifications

Internal Temperature Sensing Diode Specifications

Table 34. Internal Temperature Sensing Diode Specifications for Intel Cyclone 10 GX Devices

Temperature Range	Accuracy	Offset Calibrated Option	Sampling Rate	Conversion Time	Resolution
–40 to 100°C	±5°C	No	1 MHz	< 5 ms	10 bits

Related Information

Transfer Function for Internal TSD
Provides the transfer function for the internal TSD.

External Temperature Sensing Diode Specifications

Table 35. External Temperature Sensing Diode Specifications for Intel Cyclone 10 GX Devices

- The typical value is at 25°C.
- Diode accuracy improves with lower injection current.
- Absolute accuracy is dependent on third party external diode ADC and integration specifics.

Description	Min	Typ	Max	Unit
I_{bias}, diode source current	10	—	100	µA
V_{bias}, voltage across diode	0.3	—	0.9	V
Series resistance	—	—	< 1	Ω
Diode ideality factor	—	1.03	—	—

Internal Voltage Sensor Specifications

Table 36. Internal Voltage Sensor Specifications for Intel Cyclone 10 GX Devices

Parameter		Minimum	Typical	Maximum	Unit
Resolution		—	—	6	Bit
Sampling rate		—	—	500	Ksps
Differential non-linearity (DNL)		—	—	±1	LSB
Integral non-linearity (INL)		—	—	±1	LSB
Gain error		—	—	±1	%
Offset error		—	—	±1	LSB
Input capacitance		—	20	—	pF
Clock frequency		0.1	—	11	MHz
Unipolar Input Mode	Input signal range for Vsigp	0	—	1.5	V
	Common mode voltage on Vsign	0	—	0.25	V
	Input signal range for Vsigp – Vsign	0	—	1.25	V

Periphery Performance Specifications

This section describes the periphery performance, high-speed I/O, and external memory interface.

Actual achievable frequency depends on design and system specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

High-Speed I/O Specifications

Table 37. High-Speed I/O Specifications for Intel Cyclone 10 GX Devices

When serializer/deserializer (SERDES) factor J = 3 to 10, use the SERDES block.

For LVDS applications, you must use the PLLs in integer PLL mode.

You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine the leftover timing margin.

The Intel Cyclone 10 GX devices support the following output standards using true LVDS output buffer types on all I/O banks:

- True RSDS output standard with data rates of up to 360 Mbps
- True mini-LVDS output standard with data rates of up to 400 Mbps

Symbol	Condition	–E5, –I5			–E6, –I6			Unit
		Min	Typ	Max	Min	Typ	Max	
f_{HSCLK_in} (input clock frequency) True Differential I/O Standards	Clock boost factor W = 1 to 40 (57)	10	—	700	10	—	625	MHz
f_{HSCLK_in} (input clock frequency) Single Ended I/O Standards	Clock boost factor W = 1 to 40 (57)	10	—	625	10	—	525	MHz
f_{HSCLK_OUT} (output clock frequency)	—	—	—	700 (58)	—	—	625 (58)	MHz

continued...

(57) Clock Boost Factor (W) is the ratio between the input data rate and the input clock rate.

(58) This is achieved by using the PHY clock network.

Symbol		Condition	–E5, –I5			–E6, –I6			Unit
			Min	Typ	Max	Min	Typ	Max	
Transmitter	True Differential I/O Standards - f_{HSDR} (data rate) (59)	SERDES factor J = 4 to 10 (60)(61)(62)	(62)	—	1434	(62)	—	1250	Mbps
		SERDES factor J = 3 (60)(61)(62)	(62)	—	1076	(62)	—	938	Mbps
		SERDES factor J = 2, uses DDR registers	(62)	—	275 (63)	(62)	—	250 (63)	Mbps
		SERDES factor J = 1, uses DDR registers	(62)	—	275 (63)	(62)	—	250 (63)	Mbps
	$t_{x\ Jitter}$ - True Differential I/O Standards	Total jitter for data rate, 600 Mbps – 1.6 Gbps	—	—	200	—	—	250	ps
		Total jitter for data rate, < 600 Mbps	—	—	0.12	—	—	0.15	UI
	t_{DUTY} (64)	TX output clock duty cycle for Differential I/O Standards	45	50	55	45	50	55	%
	$t_{RISE\ \&}$ & t_{FALL} (61) (65)	True Differential I/O Standards	—	—	180	—	—	200	ps

continued...

(59) Requires package skew compensation with PCB trace length.

(60) The F_{max} specification is based on the fast clock used for serial data. The interface F_{max} is also dependent on the parallel clock domain which is design dependent and requires timing analysis.

(61) The V_{CC} and V_{CCP} must be on a combined power layer and a maximum load of 5 pF for chip-to-chip interface.

(62) The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and serializer do not have a minimum toggle rate.

(63) The maximum ideal data rate is the SERDES factor (J) x the PLL maximum output frequency (f_{OUT}) provided you can close the design timing and the signal integrity meets the interface requirements.

(64) Not applicable for `DIVCLK = 1`.

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Symbol		Condition	–E5, –I5			–E6, –I6			Unit
			Min	Typ	Max	Min	Typ	Max	
	TCCS (64)(59)	True Differential I/O Standards	—	—	150	—	—	150	ps
Receiver	True Differential I/O Standards - $f_{HSDRDPA}$ (data rate)	SERDES factor J = 4 to 10 (60)(61)(62)	150	—	1434	150	—	1250	Mbps
		SERDES factor J = 3 (60)(61)(62)	150	—	1076	150	—	938	Mbps
	f_{HSDR} (data rate) (without DPA) (59)	SERDES factor J = 3 to 10	(62)	—	(66)	(62)	—	(66)	Mbps
		SERDES factor J = 2, uses DDR registers	(62)	—	(63)	(62)	—	(63)	Mbps
		SERDES factor J = 1, uses DDR registers	(62)	—	(63)	(62)	—	(63)	Mbps
DPA (FIFO mode)	DPA run length	—	—	—	10000	—	—	10000	UI
DPA (soft CDR mode)	DPA run length	SGMII/GbE protocol	—	—	5	—	—	5	UI
		All other protocols	—	—	50 data transition per 208 UI	—	—	50 data transition per 208 UI	—
Soft CDR mode	Soft-CDR ppm tolerance	—	—	—	300	—	—	300	± ppm
Non DPA mode	Sampling Window	—	—	—	300	—	—	300	ps

(65) This applies to default pre-emphasis and V_{OD} settings only.

(66) You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.

DPA Lock Time Specifications

Figure 2. DPA Lock Time Specifications with DPA PLL Calibration Enabled

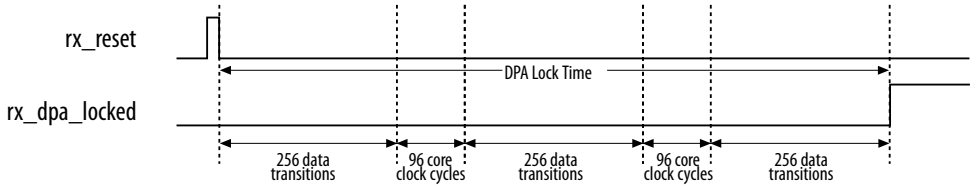


Table 38. DPA Lock Time Specifications for Intel Cyclone 10 GX Devices

The specifications are applicable to both extended and industrial grades. The DPA lock time is for one channel. One data transition is defined as a 0-to-1 or 1-to-0 transition.

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions (67)	Maximum Data Transition
SPI-4	00000000001111111111	2	128	640
Parallel Rapid I/O	00001111	2	128	640
	10010000	4	64	640
Miscellaneous	10101010	8	32	640
	01010101	8	32	640

(67) This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specifications

Figure 3. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specifications for a Data Rate Equal to 1.4 Gbps

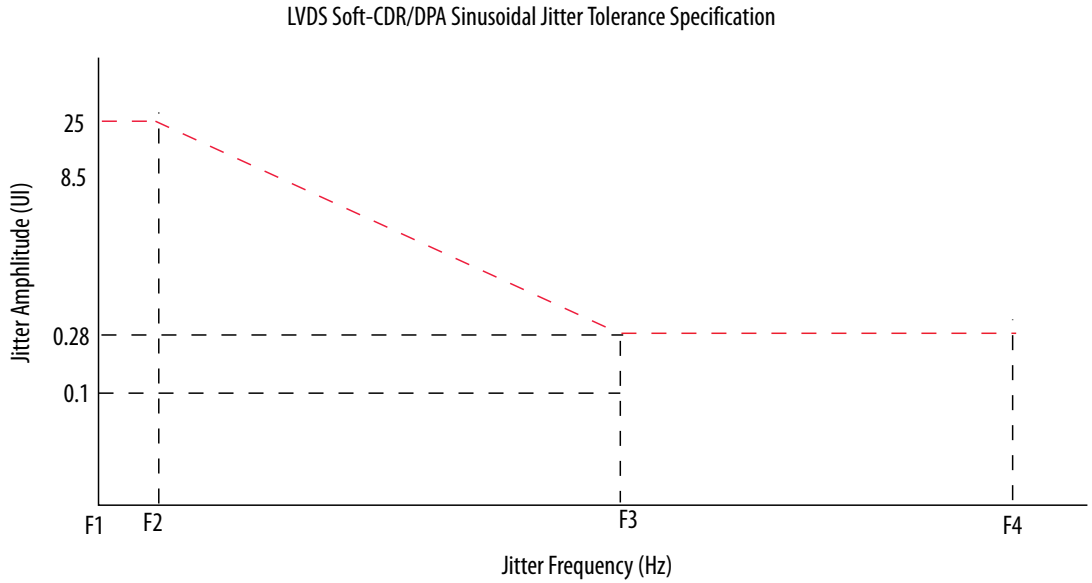
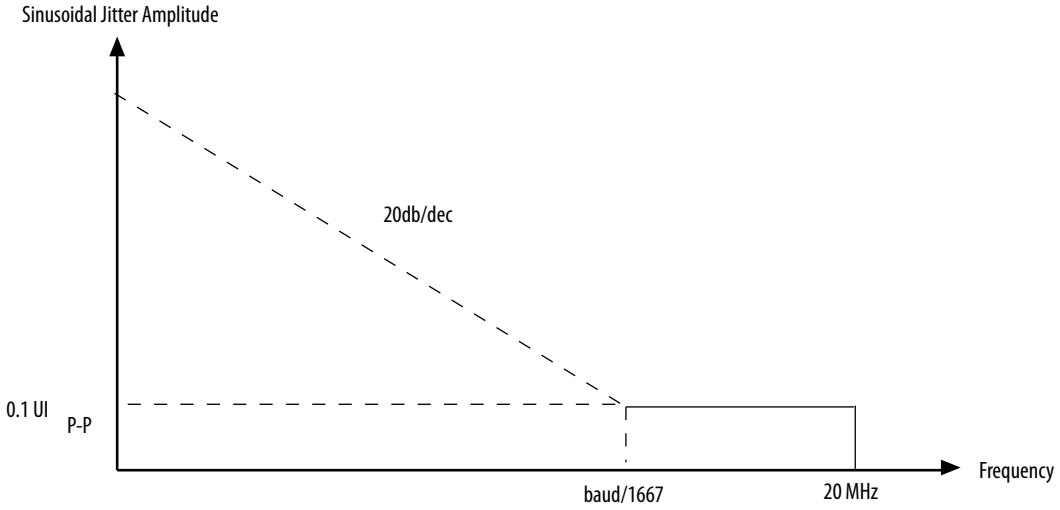


Table 39. LVDS Soft-CDR/DPA Sinusoidal Jitter Mask Values for a Data Rate Equal to 1.4 Gbps

Jitter Frequency (Hz)		Sinusoidal Jitter (UI)
F1	10,000	25.00
F2	17,565	25.00
F3	1,493,000	0.28
F4	50,000,000	0.28

Figure 4. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specifications for a Data Rate Less than 1.4 Gbps



Memory Standards Supported by the Hard Memory Controller

Table 40. Memory Standards Supported by the Hard Memory Controller for Intel Cyclone 10 GX Devices

This table lists the overall capability of the hard memory controller. For specific details, refer to the External Memory Interface Spec Estimator.

Memory Standard	Rate Support	Speed Grade	Ping Pong PHY Support	Maximum Frequency (MHz)	
				I/O Bank	3 V I/O Bank
DDR3 SDRAM	Half rate	–5	Yes	533	225
			—	533	225
		–6	Yes	466	166
			—	466	166
	Quarter rate	–5	Yes	933	450
			—	933	450
		–6	Yes	933	333

continued...

Memory Standard	Rate Support	Speed Grade	Ping Pong PHY Support	Maximum Frequency (MHz)	
				I/O Bank	3 V I/O Bank
			—	933	333
DDR3L SDRAM	Half rate	–5	Yes	533	225
			—	533	225
		–6	Yes	466	166
			—	466	166
	Quarter rate	–5	Yes	933	450
			—	933	450
		–6	Yes	933	333
			—	933	333
LPDDR3 SDRAM	Half rate	–5	—	400	225
		–6	—	333	166
	Quarter rate	–5	—	800	450
		–6	—	666	333

Related Information

External Memory Interface Spec Estimator
Provides the specific details of the memory standards supported.

DLL Range Specifications

Table 41. DLL Frequency Range Specifications for Intel Cyclone 10 GX Devices

Intel Cyclone 10 GX devices support memory interface frequencies lower than 600 MHz, although the reference clock that feeds the DLL must be at least 600 MHz. To support interfaces below 600 MHz, multiply the reference clock feeding the DLL to ensure the frequency is within the supported range.

Parameter	Performance (for All Speed Grades)	Unit
DLL operating frequency range	600 – 1333	MHz

DQS Logic Block Specifications

Table 42. DQS Phase Shift Error Specifications for DLL-Delayed Clock (t_{DQS_PSERR}) for Intel Cyclone 10 GX Devices

This error specification is the absolute maximum and minimum error.

Symbol	Performance (for All Speed Grades)	Unit
t_{DQS_PSERR}	5	ps

Memory Output Clock Jitter Specifications

Table 43. Memory Output Clock Jitter Specifications for Intel Cyclone 10 GX Devices

The clock jitter specification applies to the memory output clock pins clocked by an I/O PLL, or generated using differential signal-splitter and double data I/O circuits clocked by a PLL output routed on a PHY clock network as specified. Intel recommends using PHY clock networks for better jitter performance.

The memory output clock jitter is applicable when an input jitter of 10 ps peak-to-peak is applied with bit error rate (BER) 10^{-12}, equivalent to 14 sigma.

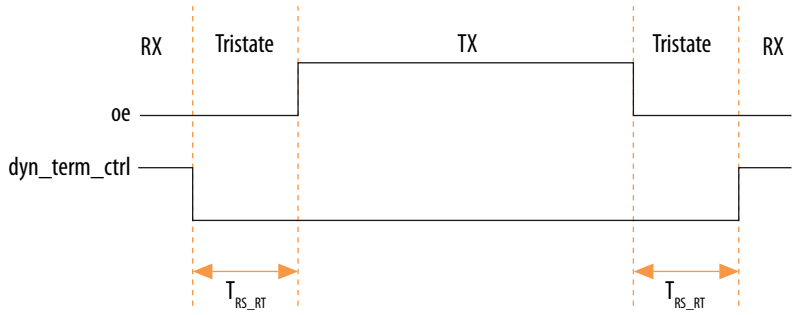
Protocol	Parameter	Symbol	Data Rate (Mbps)	Min	Max	Unit
DDR3	Clock period jitter	$t_{JIT(per)}$	1,866	–40	40	ps
	Cycle-to-cycle period jitter	$t_{JIT(cc)}$	1,866	–40	40	ps
	Duty cycle jitter	$t_{JIT(duty)}$	1,866	–40	40	ps

OCT Calibration Block Specifications

Table 44. OCT Calibration Block Specifications for Intel Cyclone 10 GX Devices

Symbol	Description	Min	Typ	Max	Unit
OCTUSRCLK	Clock required by OCT calibration blocks	—	—	20	MHz
T_{OCTCAL}	Number of OCTUSRCLK clock cycles required for R_S OCT /R_T OCT calibration	> 2000	—	—	Cycles
$T_{OCTSHIFT}$	Number of OCTUSRCLK clock cycles required for OCT code to shift out	—	32	—	Cycles
T_{RS_RT}	Time required between the `dyn_term_ctrl` and `oe` signal transitions in a bidirectional I/O buffer to dynamically switch between R_S OCT and R_T OCT	—	2.5	—	ns

Figure 5. Timing Diagram for on oe and dyn_term_ctrl Signals



Configuration Specifications

This section provides configuration specifications and timing for Intel Cyclone 10 GX devices.

POR Specifications

Power-on reset (POR) delay is defined as the delay between the time when all the power supplies monitored by the POR circuitry reach the minimum recommended operating voltage to the time when the nSTATUS is released high and your device is ready to begin configuration.

Table 45. Fast and Standard POR Delay Specification for Intel Cyclone 10 GX Devices

POR Delay	Minimum	Maximum	Unit
Fast	4	12 [68]	ms
Standard	100	300	ms

Related Information

MSEL Pin Settings
Provides more information about POR delay based on MSEL pin settings for each configuration scheme.

[68] The maximum pulse width of the fast POR delay is 12 ms, providing enough time for the PCIe hard IP to initialize after the POR trip.

JTAG Configuration Timing

Table 46. JTAG Timing Parameters and Values for Intel Cyclone 10 GX Devices

Symbol	Description	Min	Max	Unit
t_{JCP}	TCK clock period	30, 167 (69)	—	ns
t_{JCH}	TCK clock high time	14	—	ns
t_{JCL}	TCK clock low time	14	—	ns
$t_{JPSU\ (TDI)}$	TDI JTAG port setup time	2	—	ns
$t_{JPSU\ (TMS)}$	TMS JTAG port setup time	3	—	ns
t_{JPH}	JTAG port hold time	5	—	ns
t_{JPCO}	JTAG port clock to output	—	11	ns
t_{JPZX}	JTAG port high impedance to valid output	—	14	ns
t_{JPXZ}	JTAG port valid output to high impedance	—	14	ns

FPP Configuration Timing

DCLK-to-DATA[] Ratio (r) for FPP Configuration

Fast passive parallel (FPP) configuration requires a different DCLK-to-DATA[] ratio when you turn on encryption or the compression feature.

Depending on the DCLK-to-DATA[] ratio, the host must send a DCLK frequency that is *r* times the DATA[] rate in byte per second (Bps) or word per second (Wps). For example, in FPP ×16 where the *r* is 2, the DCLK frequency must be 2 times the DATA[] rate in Wps.

(69) The minimum TCK clock period is 167 ns if V_{CCBAT} is within the range 1.2 V – 1.5 V when you perform the volatile key programming.

Table 47. DCLK-to-DATA[] Ratio for Intel Cyclone 10 GX Devices

You cannot turn on encryption and compression at the same time for Intel Cyclone 10 GX devices.

Configuration Scheme	Encryption	Compression	DCLK-to-DATA[] Ratio (r)
FPP (8-bit wide)	Off	Off	1
	On	Off	1
	Off	On	2
FPP (16-bit wide)	Off	Off	1
	On	Off	2
	Off	On	4
FPP (32-bit wide)	Off	Off	1
	On	Off	4
	Off	On	8

FPP Configuration Timing when DCLK-to-DATA[] = 1

Note: When you enable decompression or the design security feature, the DCLK-to-DATA[] ratio varies for FPP ×8, FPP ×16, and FPP ×32. For the respective DCLK-to-DATA[] ratio, refer to the DCLK-to-DATA[] Ratio for Intel Cyclone 10 GX Devices table.

Table 48. FPP Timing Parameters When the DCLK-to-DATA[] Ratio is 1 for Intel Cyclone 10 GX Devices

Use these timing parameters when the decompression and design security features are disabled.

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CD}	nCONFIG low to CONF_DONE low	480	1,440	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	320	960	ns
t_{CFG}	nCONFIG low pulse width	2	—	µs
t_{STATUS}	nSTATUS low pulse width	268	3,000 (70)	µs
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	3,000 (71)	µs

continued...

(70) This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CK} (72)	nCONFIG high to first rising edge on DCLK	3,010	—	µs
t_{ST2CK} (72)	nSTATUS high to first rising edge of DCLK	10	—	µs
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	0	—	ns
t_{CH}	DCLK high time	$0.45 \times 1/f_{MAX}$	—	s
t_{CL}	DCLK low time	$0.45 \times 1/f_{MAX}$	—	s
t_{CLK}	DCLK period	$1/f_{MAX}$	—	s
f_{MAX}	DCLK frequency (FPP ×8/×16/×32)	—	100	MHz
t_{CD2UM}	CONF_DONE high to user mode (73)	175	830	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (600 × CLKUSR period)	—	—

Related Information

FPP Configuration Timing
Provides the FPP configuration timing waveforms.

(71) This value is applicable if you do not delay configuration by externally holding the nSTATUS low.

(72) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

(73) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

FPP Configuration Timing when DCLK-to-DATA[] >1

Table 49. FPP Timing Parameters When the DCLK-to-DATA[] Ratio is >1 for Intel Cyclone 10 GX Devices

Use these timing parameters when you use the decompression and design security features.

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CD}	nCONFIG low to CONF_DONE low	480	1,440	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	320	960	ns
t_{CFG}	nCONFIG low pulse width	2	—	µs
t_{STATUS}	nSTATUS low pulse width	268	3,000 (74)	µs
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	3,000 (74)	µs
t_{CF2CK} (75)	nCONFIG high to first rising edge on DCLK	3,010	—	µs
t_{ST2CK} (75)	nSTATUS high to first rising edge of DCLK	10	—	µs
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	$N–1/f_{DCLK}$ (76)	—	s
t_{CH}	DCLK high time	$0.45 \times 1/f_{MAX}$	—	s
t_{CL}	DCLK low time	$0.45 \times 1/f_{MAX}$	—	s
t_{CLK}	DCLK period	$1/f_{MAX}$	—	s
f_{MAX}	DCLK frequency (FPP ×8/×16/×32)	—	100	MHz
t_R	Input rise time	—	40	ns
t_F	Input fall time	—	40	ns

continued...

(74) You can obtain this value if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

(75) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

(76) *N* is the DCLK-to-DATA ratio and f_{DCLK} is the DCLK frequency the system is operating.

Symbol	Parameter	Minimum	Maximum	Unit
t_{CD2UM}	CONF_DONE high to user mode [77]	175	830	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (600 × CLKUSR period)	—	—

Related Information

FPP Configuration Timing
Provides the FPP configuration timing waveforms.

AS Configuration Timing

Table 50. AS Timing Parameters for AS ×1 and AS ×4 Configurations in Intel Cyclone 10 GX Devices

The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.

The t_{CF2CD}, t_{CF2ST0}, t_{CFG}, t_{STATUS}, and t_{CF2ST1} timing parameters are identical to the timing parameters for passive serial (PS) mode listed in PS Timing Parameters for Intel Cyclone 10 GX Devices table.

Symbol	Parameter	Minimum	Maximum	Unit
t_{CO}	DCLK falling edge to AS_DATA0/ASDO output	—	2	ns
t_{SU}	Data setup time before falling edge on DCLK	1	—	ns
t_{DH}	Data hold time after falling edge on DCLK	1.5	—	ns
t_{CD2UM}	CONF_DONE high to user mode	175	830	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (600 × CLKUSR period)	—	—

(77) The minimum and maximum numbers apply only if you use the internal oscillator as the clock source for initializing the device.

Related Information

- PS Configuration Timing on page 50
- AS Configuration Timing
  Provides the AS configuration timing waveform.

DCLK Frequency Specification in the AS Configuration Scheme

Table 51. DCLK Frequency Specification in the AS Configuration Scheme

This table lists the internal clock frequency specification for the AS configuration scheme.

The DCLK frequency specification applies when you use the internal oscillator as the configuration clock source.

The AS multi-device configuration scheme does not support DCLK frequency of 100 MHz.

You can only set 12.5, 25, 50, and 100 MHz in the Intel Quartus Prime software.

Parameter	Minimum	Typical	Maximum	Intel Quartus Prime Software Settings	Unit
DCLK frequency in AS configuration scheme	5.3	7.5	9.7	12.5	MHz
	10.5	15.0	19.3	25.0	MHz
	21.0	30.0	38.5	50.0	MHz
	42.0	60.0	77.0	100.0	MHz

PS Configuration Timing

Table 52. PS Timing Parameters for Intel Cyclone 10 GX Devices

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CD}	nCONFIG low to CONF_DONE low	480	1,440	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	320	960	ns
t_{CFG}	nCONFIG low pulse width	2	—	µs
t_{STATUS}	nSTATUS low pulse width	268	3,000 (78)	µs
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	3,000 (79)	µs

continued...

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CK} (80)	nCONFIG high to first rising edge on DCLK	3,010	—	µs
t_{ST2CK} (80)	nSTATUS high to first rising edge of DCLK	10	—	µs
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	0	—	ns
t_{CH}	DCLK high time	$0.45 \times 1/f_{MAX}$	—	s
t_{CL}	DCLK low time	$0.45 \times 1/f_{MAX}$	—	s
t_{CLK}	DCLK period	$1/f_{MAX}$	—	s
f_{MAX}	DCLK frequency	—	125	MHz
t_{CD2UM}	CONF_DONE high to user mode (81)	175	830	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (600 × CLKUSR period)	—	—

Related Information

PS Configuration Timing
Provides the PS configuration timing waveform.

(78) This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

(79) This value is applicable if you do not delay configuration by externally holding the nSTATUS low.

(80) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

(81) The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.

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Initialization

Table 53. Initialization Clock Source Option and the Maximum Frequency for Intel Cyclone 10 GX Devices

Initialization Clock Source	Configuration Scheme	Maximum Frequency (MHz)	Minimum Number of Clock Cycles
Internal Oscillator	AS, PS, and FPP	12.5	600
CLKUSR [82][83]	AS, PS, and FPP	100	

Configuration Files

There are two types of configuration bit stream formats for different configuration schemes:

- PS and FPP—Raw Binary File (`.rbf`)
- AS—Raw Programming Data File (`.rpd`)

The `.rpd` file size follows the Intel configuration devices capacity. However, the actual configuration bit stream size for `.rpd` file is the same as `.rbf` file.

(82) To enable CLKUSR as the initialization clock source, in the Intel Quartus Prime software, select **Device and Pin Options ➤ General ➤ Device initialization clock source ➤ CLKUSR pin**.

(83) If you use the CLKUSR pin for AS and transceiver calibration simultaneously, the only allowed frequency is 100 MHz.

Table 54. Configuration Bit Stream Sizes for Intel Cyclone 10 GX Devices

Use this table to estimate the file size before design compilation. Different configuration file formats, such as a hexadecimal file (`.hex`) or tabular text file (`.ttf`) format, have different file sizes.

For the different types of configuration file and file sizes, refer to the Intel Quartus Prime software. However, for a specific version of the Intel Quartus Prime software, any design targeted for the same device has the same uncompressed configuration file size.

I/O configuration shift register (IOCSR) is a long shift register that facilitates the device I/O peripheral settings. The IOCSR bit stream is part of the uncompressed configuration bit stream, and it is specifically for the Configuration via Protocol (CvP) feature.

Uncompressed configuration bit stream sizes are subject to change for improvements and optimizations in the configuration algorithm.

Variant	Product Line	Uncompressed Configuration Bit Stream Size (bits)	IOCSR Bit Stream Size (bits)	Recommended EPCQ-L Serial Configuration Device
Intel Cyclone 10 GX	GX 085	81,923,582	2,507,264	EPCQ-L256 or higher density
	GX 105	81,923,582	2,507,264	EPCQ-L256 or higher density
	GX 150	81,923,582	2,507,264	EPCQ-L256 or higher density
	GX 220	81,923,582	2,507,264	EPCQ-L256 or higher density

Minimum Configuration Time Estimation

Table 55. Minimum Configuration Time Estimation for Intel Cyclone 10 GX Devices

The estimated values are based on the uncompressed configuration bit stream sizes in the Configuration Bit Stream Sizes for Intel Cyclone 10 GX Devices table.

Variant	Product Line	Active Serial [84]			Fast Passive Parallel [85]		
		Width	DCLK (MHz)	Minimum Configuration Time (ms)	Width	DCLK (MHz)	Minimum Configuration Time (ms)
Intel Cyclone 10 GX	GX 085	4	100	204.81	32	100	25.60
	GX 105	4	100	204.81	32	100	25.60
	GX 150	4	100	204.81	32	100	25.60
	GX 220	4	100	204.81	32	100	25.60

Related Information

- Configuration Files on page 52
- DCLK Frequency Specification in the AS Configuration Scheme on page 50
  Provides the DCLK frequency using internal oscillator.

(84) The minimum configuration time is calculated based on DCLK frequency of 100 MHz. Only external CLKUSR may guarantee the frequency accuracy of 100 MHz. If you use internal oscillator of 100 MHz, you may not get the actual frequency of 100 MHz. For the DCLK frequency using internal oscillator, refer to the DCLK Frequency Specification in the AS Configuration Scheme table.

(85) Maximum FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.

Remote System Upgrades

Table 56. Remote System Upgrade Circuitry Timing Specifications for Intel Cyclone 10 GX Devices

Parameter	Minimum	Maximum	Unit
$f_{MAX_RU_CLK}$ (86)	—	40	MHz
$t_{RU_nCONFIG}$ (87)	250	—	ns
$t_{RU_nRSTIMER}$ (88)	250	—	ns

Related Information

- Remote System Upgrade State Machine
  Provides more information about configuration reset (RU_CONFIG) signal.
- User Watchdog Timer
  Provides more information about reset_timer (RU_nRSTIMER) signal.

User Watchdog Internal Circuitry Timing Specifications

Table 57. User Watchdog Internal Oscillator Frequency Specifications for Intel Cyclone 10 GX Devices

Parameter	Minimum	Typical	Maximum	Unit
User watchdog internal oscillator frequency	5.3	7.9	12.5	MHz

I/O Timing

I/O timing data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the timing analysis. You may generate the I/O timing report manually using the Timing Analyzer or using the automated script.

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(86) This clock is user-supplied to the remote system upgrade circuitry. If you are using the Remote Update Intel FPGA IP core, the clock user-supplied to the Remote Update Intel FPGA IP core must meet this specification.

(87) This is equivalent to strobing the reconfiguration input of the Remote Update Intel FPGA IP core high for the minimum timing specification.

(88) This is equivalent to strobing the reset_timer input of the Remote Update Intel FPGA IP core high for the minimum timing specification.

The Intel Quartus Prime Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete place-and-route.

Related Information

AN775: I/O Timing Information Generation Guidelines
Provides the techniques to generate I/O timing information using the Intel Quartus Prime software.

Programmable IOE Delay

Table 58. IOE Programmable Delay for Intel Cyclone 10 GX Devices

For the exact values for each setting, use the latest version of the Intel Quartus Prime software. The values in the table show the delay of programmable IOE delay chain with maximum offset settings after excluding the intrinsic delay (delay at minimum offset settings).

Programmable IOE delay settings are only applicable for I/O buffers and do not apply for any other delay elements in the PHYLite for Parallel Interfaces Intel Cyclone 10 FPGA IP core.

Parameter [89]	Maximum Offset	Minimum Offset [90]	Fast Model		Slow Model		Unit
			Extended	Industrial	–E5, –I5	–E6, –I6	
Input Delay Chain Setting (`IO_IN_DLY_CHN`)	63	0	2.012	2.003	5.241	6.035	ns
Output Delay Chain Setting (`IO_OUT_DLY_CHN`)	15	0	0.478	0.475	1.263	1.462	ns

Glossary

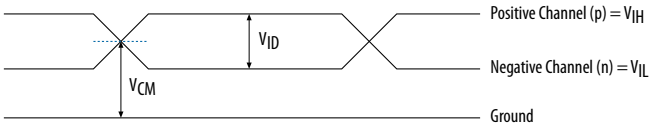
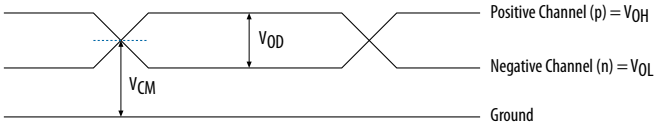
Table 59. Glossary

Term	Definition
Differential I/O Standards	Receiver Input Waveforms

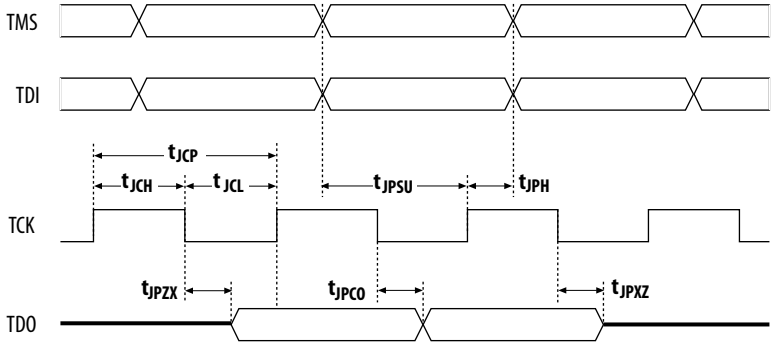
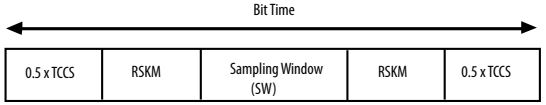
continued...

(89) You can set this value in the Intel Quartus Prime software by selecting **Input Delay Chain Setting** or **Output Delay Chain Setting** in the **Assignment Name** column.

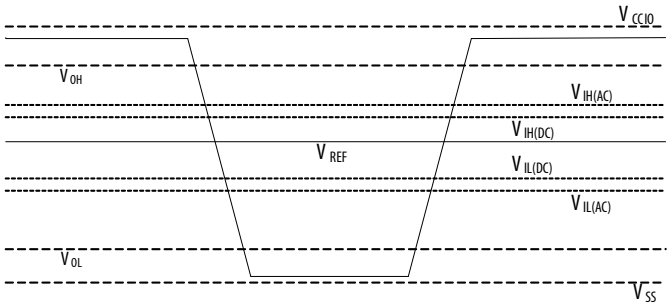
(90) Minimum offset does not include the intrinsic delay.

Term	Definition
	Single-Ended Waveform  **Differential Waveform** Transmitter Output Waveforms **Single-Ended Waveform**  **Differential Waveform**
f_{HSCLK}	I/O PLL input clock frequency.
f_{HSDR}	High-speed I/O block—Maximum/minimum LVDS data transfer rate (f_{HSDR} = 1/TUI), non-DPA.
$f_{HSDRDPA}$	High-speed I/O block—Maximum/minimum LVDS data transfer rate ($f_{HSDRDPA}$ = 1/TUI), DPA.
J	High-speed I/O block—Deserialization factor (width of parallel data bus).
JTAG Timing Specifications	JTAG Timing Specifications:

continued...

Term	Definition
	
R_L	Receiver differential input discrete resistor (external to the Intel Cyclone 10 GX device).
Sampling window (SW)	Timing Diagram—the period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position in the sampling window, as shown: 
Single-ended voltage referenced I/O standard	The JEDEC standard for the SSTL and HSTL I/O defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state. The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing. Single-Ended Voltage Referenced I/O Standard

continued...

Term	Definition
	
t_C	High-speed receiver/transmitter input and output clock period.
TCCS (channel-to-channel-skew)	The timing difference between the fastest and slowest output edges, including the t_{CO} variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the Timing Diagram figure under SW in this table).
t_{DUTY}	High-speed I/O block—Duty cycle on high-speed transmitter output clock.
t_{FALL}	Signal high-to-low transition time (80–20%)
t_{INCCJ}	Cycle-to-cycle jitter tolerance on the PLL clock input
t_{OUTPJ_IO}	Period jitter on the GPIO driven by a PLL
t_{OUTPJ_DC}	Period jitter on the dedicated clock output driven by a PLL
t_{RISE}	Signal low-to-high transition time (20–80%)
Timing Unit Interval (TUI)	The timing budget allowed for skew, propagation delays, and the data sampling window. (TUI = 1/(Receiver Input Clock Frequency Multiplication Factor) = t_C/w).
$V_{CM(DC)}$	DC Common mode input voltage.
V_{ICM}	Input Common mode voltage—The common mode of the differential signal at the receiver.
V_{ID}	Input differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
$V_{DIF(AC)}$	AC differential input voltage—Minimum AC input differential voltage required for switching.
$V_{DIF(DC)}$	DC differential input voltage— Minimum DC input differential voltage required for switching.
V_{IH}	Voltage input high—The minimum positive voltage applied to the input which is accepted by the device as a logic high.

continued...

Term	Definition
$V_{IH(AC)}$	High-level AC input voltage
$V_{IH(DC)}$	High-level DC input voltage
V_{IL}	Voltage input low—The maximum positive voltage applied to the input which is accepted by the device as a logic low.
$V_{IL(AC)}$	Low-level AC input voltage
$V_{IL(DC)}$	Low-level DC input voltage
V_{OCM}	Output Common mode voltage—The common mode of the differential signal at the transmitter.
V_{OD}	Output differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission line at the transmitter.
V_{SWING}	Differential input voltage
V_{IX}	Input differential cross point voltage
V_{OX}	Output differential cross point voltage
W	High-speed I/O block—Clock Boost Factor

Document Revision History for the Intel Cyclone 10 GX Device Datasheet

Document Version	Changes
2018.06.15	• Added *Intel Cyclone 10 GX Devices Overshoot Duration* figure and description. • Added a link in the *OCT Calibration Accuracy Specifications* section. • Removed *Equation for OCT Variation Without Recalibration*. • Updated the note to CLKUSR in the *Initialization Clock Source Option and the Maximum Frequency for Intel Cyclone 10 GX Devices* table. • Updated the *I/O Timing* section on the I/O timing information generation guidelines. • Updated the description and maximum offset values in the *IOE Programmable Delay for Intel Cyclone 10 GX Devices* table.
2018.04.06	Added notes to I_{OUT} specification in the *Absolute Maximum Ratings for Intel Cyclone 10 GX Devices* table.

Date	Version	Changes
November 2017	2017.11.10	• Changed the full symbol names for V_{CCR_GXB} and V_{CCT_GXB}, and changed the description for V_{CCH_GXB} in the *Transceiver Power Supply Operating Conditions for Intel Cyclone 10 GX Devices* table. • Removed note from the *Transceiver Power Supply Operating Conditions* section. • Added a footnote in the *Reference Clock Specifications* table. • Removed the "Programmable AC Gain at High Gain mode and Data Rate ≤ 12.5 Gbps" parameter from the *Receiver Specifications* table. • Changed the channel span descriptions for the x1 and x6 clock networks in the *Transceiver Clock Network Maximum Data Rate Specifications* table. • Changed the description of the VOD ratio in the *Typical Transmitter V_{OD} Settings* table. • Changed the specifications for CDR PPM deviation limit in the *Receiver Specifications* table. • Updated the description for V_{CCT_GXB}, V_{CCR_GXB}, and V_{CCH_GXB}. • Added note to V_I in the *Recommended Operating Conditions for Intel Cyclone 10 GX Devices* table. • Updated notes to RSDS and Mini-LVDS in the *Differential I/O Standards Specifications for Intel Cyclone 10 GX Devices* table. • Updated f_{VCO} specifications in the *Fractional PLL Specifications for Intel Cyclone 10 GX Devices* table. • Updated temperature range from "–40 to 125°C" to "–40 to 100°C" in the *Internal Temperature Sensing Diode Specifications for Intel Cyclone 10 GX Devices* table. • Updated the description for the *Memory Output Clock Jitter Specifications for Intel Cyclone 10 GX Devices* table. • Updated the following IP cores name: — Remote Update Intel FPGA — PHYLite for Parallel Interfaces Intel Cyclone 10 FPGA • Removed automotive-grade information. • Removed Preliminary tags.
May 2017	2017.05.08	Initial release.

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