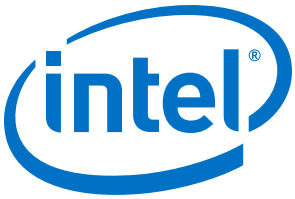
THE DATASHEET OF FPGA



Intel® Stratix® 10 DX Device Overview

S10-DX-OVERVIEW | 2020.03.24
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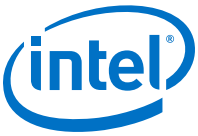

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1. Intel® Stratix® 10 DX Device Overview

Targeting high-performance acceleration applications, increasingly used in Datacenter, Networking, Cloud Computing, and Test & Measurement markets, Intel® Stratix® 10 DX FPGAs feature hard intellectual property blocks supporting both coherent and non-coherent protocol interfaces.

A low latency, high performance coherent interface is achieved when connecting the FPGA to selected Intel Xeon® Scalable Processors via Intel Ultra Path Interconnect (UPI), while the non-coherent interface takes advantage of any PCI Express* (PCIe) Gen4 capable device.

The FPGA's external memory capability now includes support for a new DDR-T soft IP memory controller, allowing interfaces to attach up to 1 TB of high-performance, persistent Intel Optane™ PMem modules per controller, directly to the FPGAs GPIO banks.

In addition to supporting these interface protocols, the DX variant FPGAs also offer hard intellectual property blocks for 100 Gigabit Ethernet and DDR4 memory control, combined with a high-performance monolithic 14 nm FPGA fabric die, all inside a single flip-chip FBGA package. Select Intel Stratix 10 DX devices include an integrated quad-core 64-bit Arm* Cortex*-A53 hard processor subsystem (HPS) on the fabric die, or embedded 3D stacked High-Bandwidth (up to 512 GB/s) DRAM memory (HBM2) inside the package.

As part of the Intel Stratix 10 family, the DX variant devices feature other innovations such as the Intel Hyperflex™ core architecture, variable precision DSP blocks with hardened support for both floating-point and fixed-point operation, and advanced packaging technology based on Intel Embedded Multi-die Interconnect Bridge (EMIB).

Important innovations in Intel Stratix 10 DX devices include:

- Intel Hyperflex core architecture delivering higher core performance compared to previous generation high-performance FPGAs
- Manufactured using Intel high volume 14 nm tri-gate (FinFET) technology
- Intel Embedded Multi-die Interconnect Bridge (EMIB) packaging technology
- A soft IP memory controller and PHY supporting DDR-T to directly attach Intel Optane PMem modules to the FPGA, two to four controllers per FPGA, and rates up to 2400 megatransfers per second (one module per channel)
- Transceivers on separate heterogeneous tiles, supporting data rates up to 57.8 gigabits per second (Gbps) Pulse Amplitude Modulation (PAM4) and 28.9 Gbps non-return-to-zero (NRZ) for chip-to-chip, chip-to-module, and backplane driving
- Hard PCI Express Gen4 x16 intellectual property blocks, with useful features such as Endpoint and Root Port bifurcation modes, virtualization support for Single-Root I/O virtualization (SR-IOV), Virtual I/O device (VIRTIO), Intel Scalable I/O Virtualization (Intel Scalable IOV), and Transaction Layer bypass mode

- Hard Intel UPI intellectual property blocks in select devices, supporting Home Agent soft IP
- Hard 100G Ethernet MAC, 100G Reed-Solomon forward error correction (FEC), and KP-FEC blocks
- 3D stacked High-Bandwidth DRAM Memory (HBM2) in select devices
- Monolithic core fabric with up to 2.8 million logic elements (LEs)
- Hard fixed-point and IEEE 754 compliant hard floating-point variable precision digital signal processing (DSP) blocks
- Hard memory controllers and PHY supporting DDR4 rates up to 2666 megabits per second (Mbps) per pin
- Hard HBM2 memory controllers in devices that include in-package 3D stacked HBM2 DRAM memory
- M20K, 20 kilobit (Kb) internal SRAM memory blocks
- eSRAM, 47.25 megabit (Mb) internal SRAM blocks in select devices
- Quad-core 64-bit Arm Cortex-A53 embedded processor running up to 1.5 GHz in select devices, processor subsystem peripherals, and high bandwidth buses to and from the FPGA logic fabric
- Programmable clock tree synthesis for flexible, low power, low skew clock trees
- Dedicated Secure Device Manager (SDM) for enhanced device configuration and security, supporting AES-256, SHA-256/384 and elliptic curve digital signature algorithm (ECDSA) -256/384 encrypt/decrypt accelerators, and multi-factor authentication
- Comprehensive set of advanced power saving features

1.1. Intel Stratix 10 DX Devices

In addition to the coherent and non-coherent protocol interfaces that are required for high-performance acceleration applications, Intel Stratix 10 DX FPGAs deliver improved core logic performance compared to previous generation high-performance FPGAs, with densities up to 2.8 million LEs in a monolithic fabric.

The devices also feature up to 84 full-duplex transceivers on separate transceiver tiles, a subset of which are capable of supporting data rates up to 57.8 Gbps PAM4 and 28.9 Gbps NRZ for both short reach and backplane driving applications. External memory interfaces up to 2666 Mbps DDR4 are achieved using hard memory controllers, and some DX variant devices include in-package 3D stacked HBM2 DRAM memory capable of supporting 512 GByte/s memory bandwidth. Select devices contain an embedded hard processor system (HPS) based on an application-class quad-core 64-bit Arm Cortex-A53, running at clock rates up to 1.5 GHz, including processor peripherals and high-bandwidth buses to and from the FPGA logic fabric.

The high-performance monolithic FPGA fabric is based on the Intel Hyperflex core architecture that includes additional Hyper-Registers everywhere throughout the interconnect routing and at the inputs of all functional blocks. The core fabric also contains an enhanced logic array utilizing Intel's adaptive logic module (ALM) and a rich set of high-performance building blocks including:

- M20K, 20 Kb embedded SRAM memory blocks
- eSRAM, 47.25 Mb embedded SRAM memory blocks (in select devices)
- Variable precision DSP blocks with hard fixed point and IEEE 754 compliant hard floating-point
- General purpose IO cells with integer PLLs in every IO bank
- Hard memory controllers and PHY for external memory interfaces
- Hard memory controllers for in-package 3D stacked HBM2 DRAM memory (in select devices)

To clock these fabric building blocks, Intel Stratix 10 DX FPGAs use programmable clock tree synthesis, which uses dedicated clock tree routing to synthesize only those branches of the clock trees required for the application.

The high-speed serial transceivers contain both the physical medium attachment (PMA) and the physical coding sublayer (PCS) required to implement a variety of industry standard protocols. In addition to the hard PCS for each transceiver, Intel Stratix 10 DX devices contain hard PCI Express IP that supports up to Gen4 x16 lane configuration, hard Intel UPI IP in select devices that supports Home Agent soft IP, and hard 10/25/100 Gbps Ethernet MAC IP with dedicated Reed-Solomon FEC for NRZ signals (528, 514) and PAM4 signals (544, 514). These hardened intellectual property blocks free up valuable core logic resources, save power, and increase your productivity.

All Intel Stratix 10 DX devices support in-system, fine-grained partial reconfiguration of the logic array, allowing logic add and subtract from the system while it is operating.

1.2. Intel Stratix 10 DX Features Summary

Table 1. Intel Stratix 10 DX Device Features

Feature	Description
Configuration	• Dedicated Secure Device Manager • Software programmable device configuration • Serial and parallel flash interface • Configuration via protocol (CvP) using PCI Express Gen1/Gen2/Gen3/Gen4 • Fine-grained partial reconfiguration of core fabric • Dynamic reconfiguration of transceivers and PLLs • Comprehensive set of security features including AES-256, SHA-256/384, and ECDSA-256/384 accelerators, and multi-factor authentication • Physically Unclonable Function (PUF) service
Core clock networks	• Programmable clock tree synthesis, backwards compatible with global, regional and peripheral clock networks • Clocks only synthesized where needed, to minimize dynamic power • 667 MHz external memory interface clocking, supports 2666 Mbps DDR4 interface • 800 MHz LVDS interface clocking, supports 1600 Mbps LVDS interface
	continued...

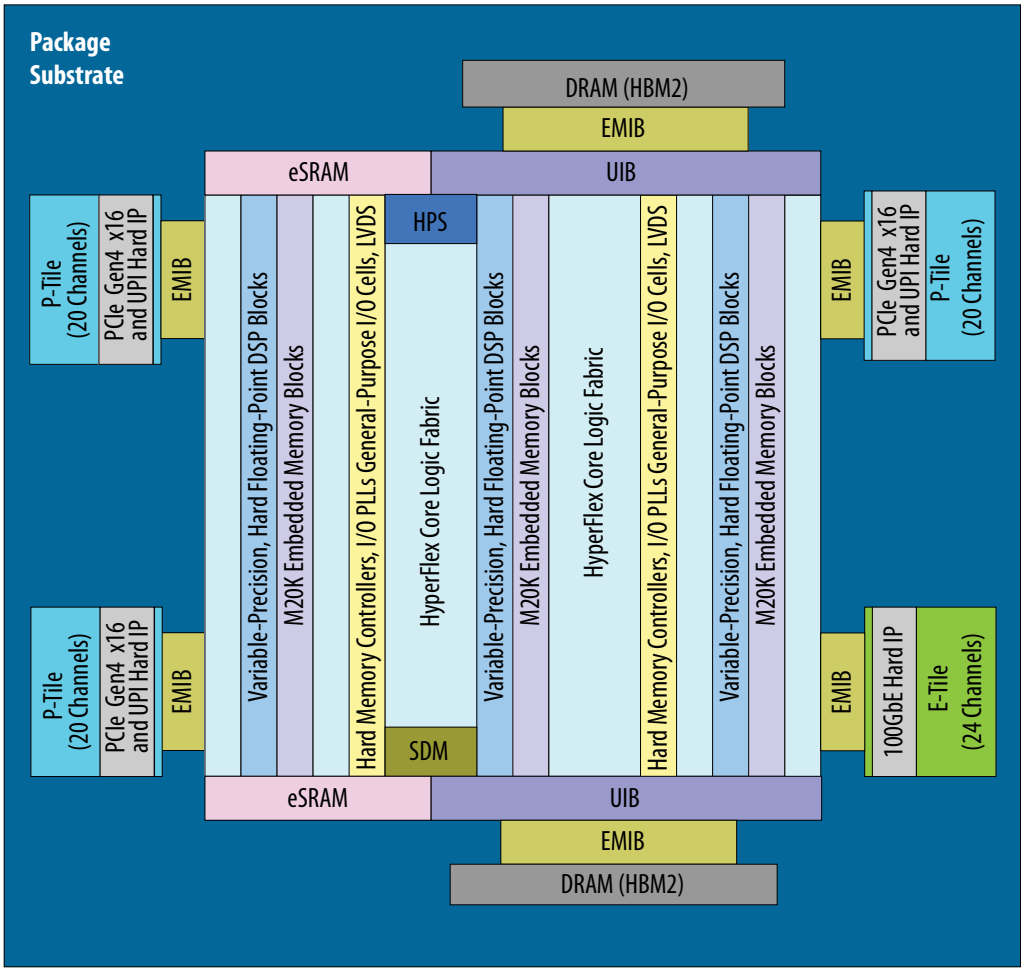
Feature	Description
Core process technology	• 14 nm Intel tri-gate (FinFET) process technology • SmartVID controlled core voltage, standard power devices
Embedded hard IP	• PCIe* Gen1/Gen2/Gen3/Gen4 x16 complete protocol stack, endpoint and root port bifurcation, SR-IOV, VIRTIO, Intel Scalable IOV, and Transaction Layer bypass • Intel UPI hard IP requires Intel soft IP (separate licensing required, selected customers only, 1SD210 and 1SD280 devices only) • 100 GbE MAC, Reed-Solomon FEC hard IP, and KP-FEC hard IP • DDR4/DDR3 hard memory controller (RLDRAM3/QDR II+/QDR IV using soft memory controller) • HBM2 DRAM hard memory controller (select devices) • Hard Processor system, Quad-core 64-bit Arm Cortex-A53 (select devices)
General purpose I/Os	• Up to 816 total GPIO available • 1.6 Gbps LVDS—every pair can be configured as an input or output • Up to 2400 megatransfers per second DDR-T external memory interface (Intel soft IP license required) • 1333 MHz/2666 Mbps DDR4 external memory interface • 1067 MHz/2133 Mbps DDR3 external memory interface • 1.2 V to 1.8 V single-ended LVCMOS/LVTTL interfacing • On-chip termination (OCT)
High performance monolithic core fabric	• Intel Hyperflex core architecture with Hyper-Registers everywhere throughout the interconnect routing and at the inputs of all functional blocks • Monolithic fabric minimizes compile times and increases logic utilization • Enhanced adaptive logic module (ALM) • Improved multi-rack routing architecture reduces congestion and improves compile times • Hierarchical core clocking architecture with programmable clock tree synthesis • Fine-grained partial reconfiguration
Internal memory blocks	• eSRAM—47.25 Mbit with hard ECC support (select devices) • M20K—20 Kbit with hard ECC support • MLAB—640 bit distributed LUTRAM
Low power serial transceivers	• Up to 84 total transceivers available • Continuous operating range of 1 Gbps to 57.8 Gbps PAM4 and 28.9 Gbps NRZ (E-tile transceivers) • Backplane support up to 57.8 Gbps PAM4 and 28.9 Gbps NRZ (E-tile transceivers) • Transmit pre-emphasis and de-emphasis • Dynamic partial reconfiguration of individual transceiver channels • On-chip instrumentation (Eye Viewer non-intrusive data eye monitoring)
Packaging	• Intel Embedded Multi-die Interconnect Bridge (EMIB) packaging technology • 1.0 mm ball-pitch FBGA packaging • Lead and lead-free package options
Phase locked loops (PLLs)	• Integer PLLs adjacent to general purpose I/Os, support external memory, and LVDS interfaces, clock delay compensation, zero delay buffering
Power management	• SmartVID controlled core voltage, standard power devices • Intel Quartus® Prime Pro Edition integrated power analysis
Software and tools	• Intel Quartus Prime Pro Edition design suite with new compiler and Hyper-Aware design flow • Fast Forward compiler to allow Intel Hyperflex architecture performance exploration • Transceiver toolkit

continued...

Feature	Description
	• Platform Designer system integration tool • DSP Builder system integration tool • OpenCL* support
Variable precision DSP blocks	• IEEE 754-compliant hard single-precision floating point capability • Supports signal processing with precision ranging from 18x19 up to 54x54 • Native 27x27 and 18x19 multiply modes • 64-bit accumulator and cascade for systolic FIRs • Internal coefficient memory banks • Pre-adder/subtractor improves efficiency • Additional pipeline register increases performance and reduces power

1.3. Intel Stratix 10 DX Block Diagram

Figure 1. Intel Stratix 10 DX Architecture Block Diagram



HPS: Quad Arm Cortex-A53 Hard Processor System
SDM: Secure Device Manager
EMIB: Embedded Multi-Die Interconnect Bridge
eSRAM: Embedded SRAM Memory Block
HBM2: High Bandwidth Memory
UIB: Universal Interface Bus

1.4. Intel Stratix 10 DX Family Plan

Table 2. Intel Stratix 10 DX FPGA Family Plan—FPGA Core (part 1)

Intel Stratix 10 DX Device Name	Logic Elements (KLE)	eSRAM Blocks	eSRAM Mbits	M20K Blocks	M20K Mbits	MLAB Counts	MLAB Mbits
DX 1100	1,325	—	—	5,461	107	11,556	7
DX 2100	2,073	2	94.5	6,847	134	17,856	11
DX 2800	2,753	—	—	11,721	229	23,796	15

Table 3. Intel Stratix 10 DX FPGA Family Plan—DSP, HPS, Interconnects, and PLLs (part 2)

Intel Stratix 10 DX Device Name	18x19 Multipliers(1)	HPS Quad Core	Interconnects			PLL
			Maximum GPIOs	Maximum Transceiver	External Memory Interfaces (x72 width)	I/O PLLs
DX 1100	5,184	Yes	528	32	2	16
DX 2100	7,920	—	612	84	4	16
DX 2800	11,520	—	816	84	4	24

Table 4. Intel Stratix 10 DX FPGA Family Plan—Hard IP and HBM2 (part 3)

Intel Stratix 10 DX Device Name	Hard IP			HBM2		Tile Layout
	Config PCIe Gen4x16, or Intel UPI, Hard IP Blocks	PCIe Gen4x16 Only, Hard IP Blocks	10/25/100 GbE MACs	Bandwidth (GByte/s)	Density (GByte)	
DX 1100	—	1	4	—	—	Figure 2
DX 2100	3	—	4	512	8	Figure 3
DX 2800	3	1	2	—	—	Figure 4

(1) The number of 27x27 multipliers is one-half the number of 18x19 multipliers.

(2) All packages are ball grid arrays with 1.0 mm pitch.

(3) High-voltage I/O pins are used for 3 V and 2.5 V interfacing.

(4) Each LVDS pair can be configured as either a differential input or a differential output.

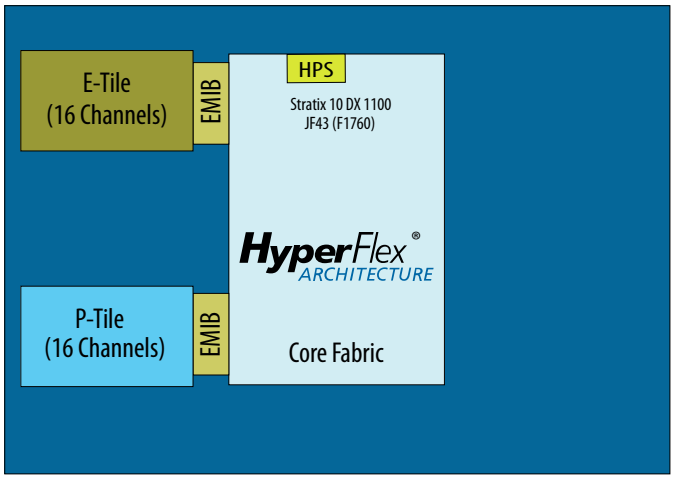
(5) High-voltage I/O pins and LVDS pairs are included in the General Purpose I/O count. Transceivers are counted separately.

Table 5. Intel Stratix 10 DX FPGA Package Plan

Cell legend: General Purpose I/Os, High-voltage I/Os, LVDS Pairs, P-tile Transceivers, E-tile Transceivers. (2) (3) (4) (5)

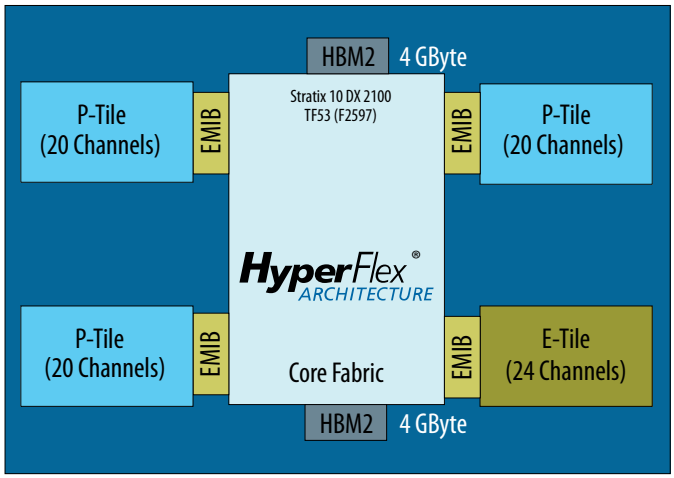
Intel Stratix 10 DX Device Name	F1760 JF43- 32 Transceivers (42.5 mm x 42.5 mm)	F2597 TF53- 84 Transceivers (52.5 mm x 52.5 mm)	F2912 TF55- 84 Transceivers (55 mm x 55 mm)
DX 1100	528, 0, 264, 16, 16	—	—
DX 2100	—	612, 0, 306, 60, 24	—
DX 2800	—	—	816, 0, 408, 76, 8

Figure 2. Intel Stratix 10 DX 1100, 1 P-Tile, 1 E-Tile (32 Transceiver Channels)



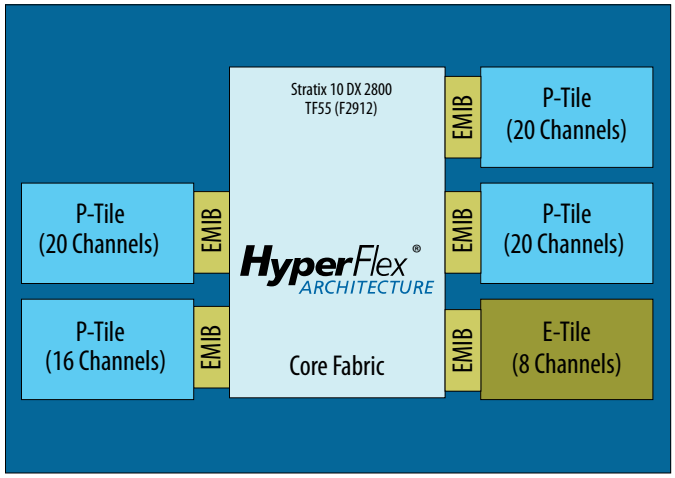
Note: The P-tile with 16 channels can be used for PCIe only, not for Intel UPI.

Figure 3. Intel Stratix 10 DX 2100, 3 P-Tiles, 1 E-Tile (84 Transceiver Channels) and 2 HBM2 (8 GBytes total)



Note: The P-tile with 20 channels can be used for either PCIe, or for Intel UPI.

Figure 4. Intel Stratix 10 DX 2800, 4 P-Tiles, 1 E-Tile (84 Transceiver Channels)

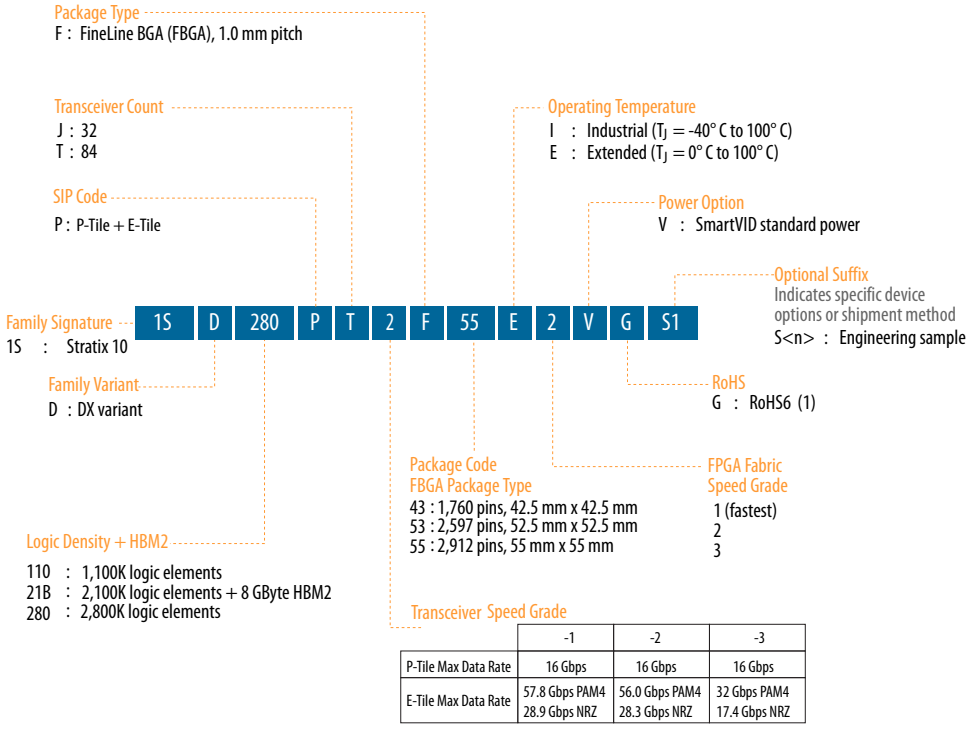


Note: The P-tile with 16 channels can be used for PCIe only, not for Intel UPI.

The P-tile with 20 channels can be used for either PCIe, or for Intel UPI.

1.4.1. Available Options

Figure 5. Sample Ordering Code and Available Options for Intel Stratix 10 DX Devices



	-1	-2	-3
P-Tile Max Data Rate	16 Gbps	16 Gbps	16 Gbps
E-Tile Max Data Rate	57.8 Gbps PAM4 28.9 Gbps NRZ	56.0 Gbps PAM4 28.3 Gbps NRZ	32 Gbps PAM4 17.4 Gbps NRZ

Note:
1. Lead-free RoHS6 devices use SAC405 solder balls, 95.5% Tin, 4.0% Silver, and 0.5% Copper.

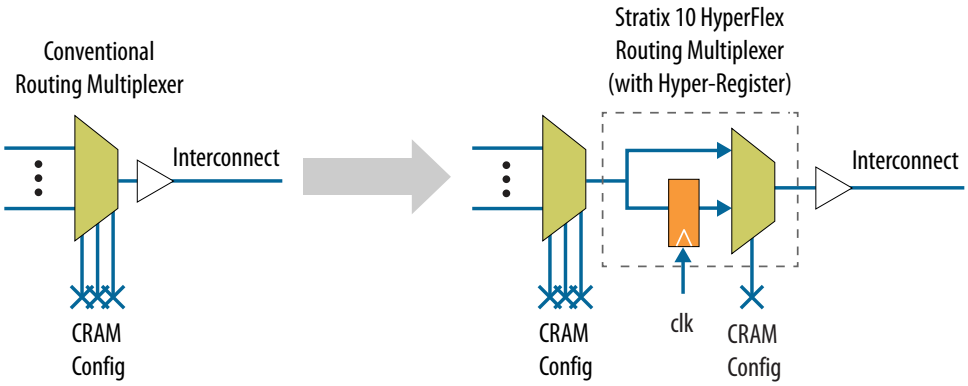
1.5. Intel Hyperflex Core Architecture

Intel Stratix 10 DX devices are based on a monolithic core fabric featuring the new Intel Hyperflex core architecture. The Intel Hyperflex core architecture delivers higher performance and up to 70% lower power compared to previous generation high-end FPGAs. Along with this performance breakthrough, the Intel Hyperflex core architecture delivers a number of advantages including:

- **Higher Throughput**—Capitalizes on high core clock frequency performance to obtain throughput breakthroughs
- **Improved Power Efficiency**—Uses reduced IP size, enabled by Intel Hyperflex, to consolidate designs which previously spanned multiple devices into a single device, thereby reducing power by up to 70% versus previous generation devices
- **Greater Design Functionality**—Uses faster clock frequency to reduce bus widths and reduce IP size, freeing up additional FPGA resources to add greater functionality
- **Increased Designer Productivity**—Boosts performance with less routing congestion and fewer design iterations using Hyper-Aware design tools, obtaining greater timing margin for more rapid timing closure

In addition to the traditional user registers found in the Adaptive Logic Modules (ALM), the Intel Hyperflex core architecture introduces additional bypassable registers everywhere throughout the fabric of the FPGA. These additional registers, called Hyper-Registers are available on every interconnect routing segment and at the inputs of all functional blocks.

Figure 6. Bypassable Hyper-Register

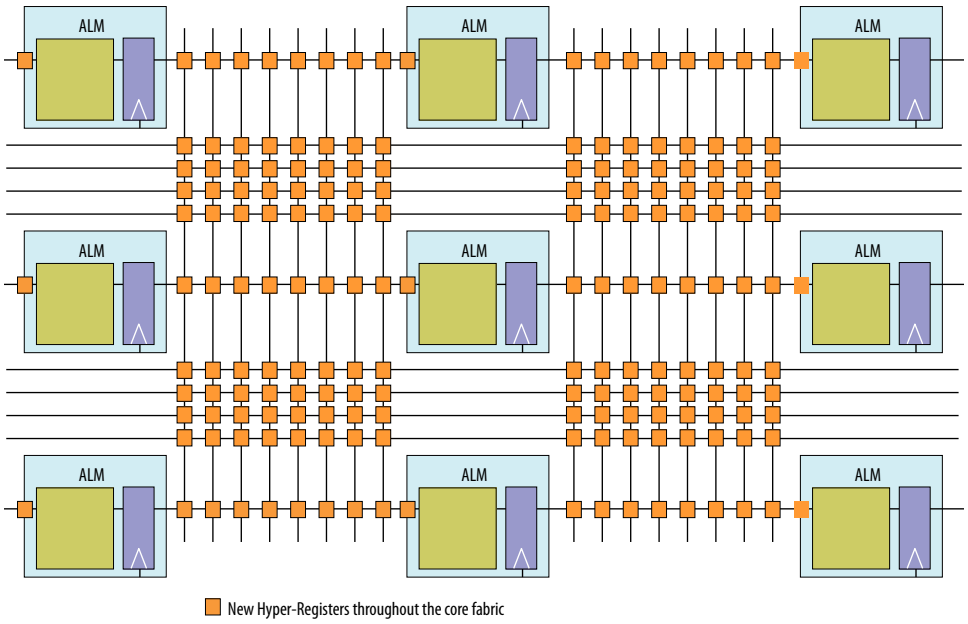


The Hyper-Registers enable the following key design techniques to achieve the 2X core performance increases:

- Fine grain Hyper-Retiming to eliminate critical paths
- Zero latency Hyper-Pipelining to eliminate routing delays
- Flexible Hyper-Optimization for best-in-class performance

By implementing these techniques in your design, the Hyper-Aware design tools automatically make use of the Hyper-Registers to achieve maximum core clock frequency.

Figure 7. Intel Hyperflex Core Architecture



1.6. Heterogeneous 3D SiP Transceiver Tiles

Intel Stratix 10 DX devices feature power efficient, high bandwidth, low latency transceivers. The transceivers are implemented on heterogeneous 3D System-in-Package (SiP) transceiver tiles, each containing up to 24 full-duplex transceiver channels. In addition to providing a high-performance transceiver solution to meet current connectivity needs, this allows for future flexibility and scalability as data rates, modulation schemes, and protocol IPs evolve.

1.7. Intel Stratix 10 DX Transceivers

1.7.1. Intel P-Tile Transceivers and Hard IP

Intel Stratix 10 DX devices contain one or more P-tiles, each P-tile containing up to 20 full-duplex transceiver channels, along with PCIe Gen4 x16 hard IP and Intel UPI hard IP. If all 20 channels from the P-tile are available in the device, the P-tile can be configured to support either a PCIe interface or an Intel UPI interface. If only 16 channels are available, the P-tile supports PCIe but does not support Intel UPI which requires all 20 channels. Support for protocols other than PCIe or Intel UPI is not possible with the P-tile; it is not possible to bypass the hard IP blocks and connect the P-tile transceivers directly to the FPGA fabric.

Table 6. Intel Stratix 10 P-Tile PCIe Features

Feature	Capability
PCIe Configurations	• Gen4 or Gen3, x16 endpoint or root port • Gen4 or Gen3, x8 + x8 static port bifurcation, endpoints only • Gen4 or Gen3, x4 + x4 + x4 + x4 static port bifurcation, root ports only

continued...

Feature	Capability
	• Gen2 and Gen1 configurations supported indirectly through link negotiation • x1, x2 widths supported indirectly through protocol width reduction capability • Chip-to-chip and low-loss cable support
Virtualization Support	• Single-Root I/O Virtualization (SR-IOV), 8 physical functions (PF) and 2048 virtual functions (VF) per endpoint • Intel Scalable IOV support for software-based virtualization • Virtual I/O Device (VIRTIO)
Switch Support	• Transaction Layer Bypass (TLP bypass) enables PCIe switch implementations using SWUP and SWDN ports

Table 7. Intel Stratix 10 P-Tile Intel UPI Features

Feature	Capability
Intel UPI Configurations	• 20 lane support for 9.6 GT/s, 10.4 GT/s, 11.2 GT/s data rates • PHY and Link Layer support for Home Agent soft IP, Home Agent is implemented in the FPGA fabric • Chip-to-chip and low-loss cable support

1.7.2. Intel E-Tile Transceivers and Hard IP

Intel Stratix 10 DX devices contain one E-tile.

Each E-tile contains up to 24 full-duplex dual-mode transceivers, each transceiver capable of supporting both Pulse Amplitude Modulation with 4 levels (PAM4) up to 57.8 Gbps, and non-return-to-zero (NRZ) up to 28.9 Gbps. In addition to the transceivers, each E-tile contains multiple instances of 10/25/100 Gbps Ethernet MAC + FEC hard IP blocks. Both Reed-Solomon and KP FEC hard IP blocks are included, allowing complete Ethernet interfaces to be implemented, simplifying the design of complex multi-port Ethernet systems.

Table 8. Available E-Tile Transceiver Channels in Intel Stratix 10 DX FPGA Devices

Intel Stratix 10 DX Device Name	Number of E-Tile Transceiver Channels	Available E-Tile Transceiver Channel Locations
DX 1100	16	0, 1, 2, 3, 8, 9, 10, 11, 12, 13, 14, 15, 20, 21, 22, 23
DX 2100	24	0 through 23
DX 2800	8	0, 1, 2, 3, 12, 13, 14, 15

For more information about the E-tile transceivers and the E-tile Ethernet hard IP, refer to the *Intel Stratix 10 E-Tile Transceiver PHY User Guide.*

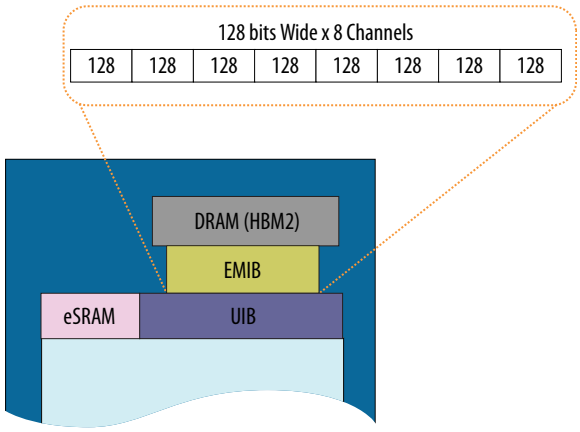
1.8. Heterogeneous 3D Stacked HBM2 DRAM Memory

Select Intel Stratix 10 DX devices integrate 3D stacked High-Bandwidth DRAM Memory (HBM2) alongside a high-performance monolithic 14 nm FPGA fabric die, and multiple high-speed transceiver tiles, all inside a single flip-chip FBGA package.

This results in a "near memory" implementation where the high-density stacked DRAM is integrated very close to the FPGA in the same package. In this configuration the in-package memory is able to deliver up to 512 GByte/s of total aggregate bandwidth which represents over a 10X increase in bandwidth compared to traditional "far

memory" implemented in separate devices on the board. A near memory configuration also reduces system power by reducing traces between the FPGA and memory, while also reducing board area.

Figure 8. Heterogeneous 3D Stacked HBM2 DRAM Architecture



Select Intel Stratix 10 DX devices integrate two 3D HBM2 DRAM memory stacks inside the package. Each of these DRAM stacks has:

- 4 GByte density per stack, for a total density of 8 GByte per device
- 256 GByte/s bandwidth per stack, for a total aggregate bandwidth of 512 GByte/s per device
- 8 independent channels, each 128 bits wide, or 16 independent pseudo channels, each 64 bits wide (in pseudo channel mode)
- Data transfer rates up to 2 Gbps, per signal, between core fabric and HBM2 DRAM
- Half-rate transfer to core fabric

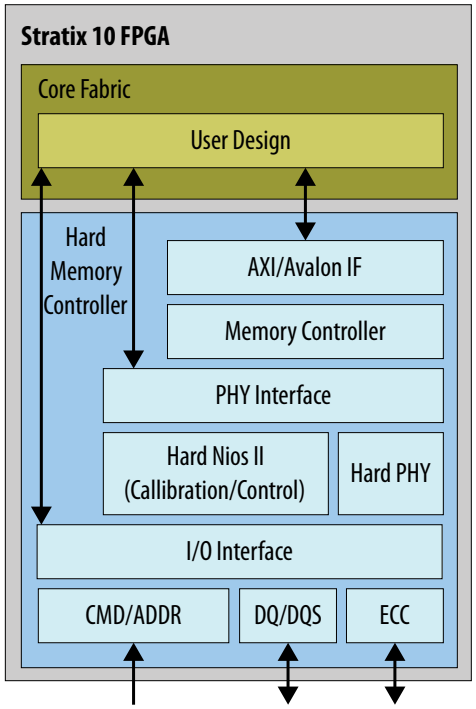
Intel Stratix 10 DX devices use embedded hard memory controllers to access the HBM2 DRAM.

1.9. External Memory and General Purpose I/O

In addition to the bandwidth delivered by the in-package HBM2 DRAM near memory (in selected devices), all Intel Stratix 10 DX devices offer substantial external memory bandwidth, supporting DDR4 memory interfaces running at up to 2666 Mbps and DDR-T memory interfaces at up to 2400 megatransfers per second.

This bandwidth is provided along with the ease of design, lower power, and resource efficiencies of hardened high-performance memory controllers. The external memory interfaces can be configured up to a maximum width of 144 bits when using either hard or soft memory controllers.

Figure 9. Hard Memory Controller



Each I/O bank contains 48 general purpose I/Os and a high-efficiency hard memory controller capable of supporting many different memory types, each with different performance capabilities. The hard memory controller is also capable of being bypassed and replaced by a soft controller implemented in user logic. The I/Os each have a hardened double data rate (DDR) read/write path (PHY) capable of performing key memory interface functionality such as:

- Read/write leveling
- FIFO buffering to lower latency and improve margin
- Timing calibration
- On-chip termination

The timing calibration is aided by the inclusion of hard microcontrollers based on Intel's Nios® II technology, specifically tailored to control the calibration of multiple memory interfaces. This calibration allows the Intel Stratix 10 DX device to compensate for any changes in process, voltage, or temperature either within the device itself, or within the external memory device. The advanced calibration algorithms ensure maximum bandwidth and robust timing margin across all operating conditions. For the list of features available with the Intel DDR-T memory controller IP, see External Memory Interface and the *DDR-T Memory Controller IP User Guide*. For the *DDR-T Memory Controller IP User Guide*, contact My Intel support.

Table 9. External Memory Interface Performance

The listed speeds are for the 1-rank case.

Interface	Controller Type	Performance (maximum rate possible)
Intel DDR-T	Soft	2400 megatransfers per second (one module per controller)
DDR4	Hard	2666 Mbps
DDR3	Hard	2133 Mbps
QDRII+	Soft	1,100 Mtps
QDRII+ Xtreme	Soft	1,266 Mtps
QDRIV	Soft	2,133 Mtps
RLDRAM III	Soft	2400 Mbps
RLDRAM II	Soft	533 Mbps

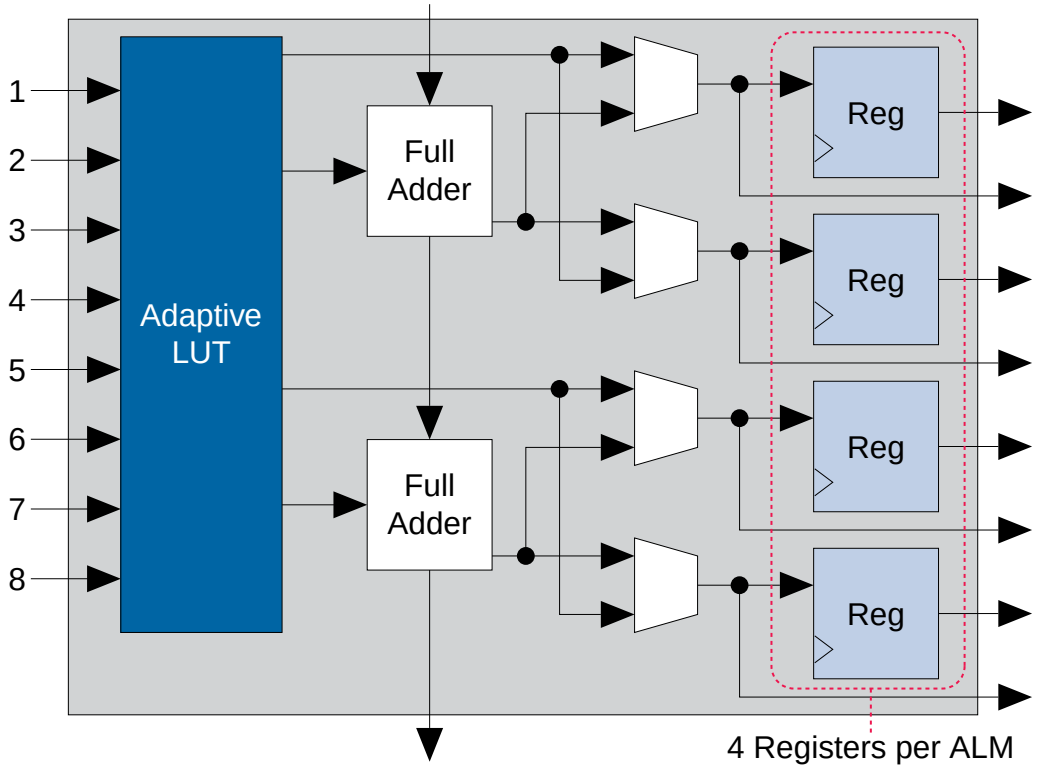
Intel Stratix 10 DX devices also feature general purpose I/Os capable of supporting a wide range of single-ended and differential I/O interfaces. LVDS rates up to 1.6 Gbps are supported, with each pair of pins having both a differential driver and a differential input buffer. This enables configurable direction for each LVDS pair.

1.10. Adaptive Logic Module (ALM)

Intel Stratix 10 DX devices use a similar adaptive logic module (ALM) as the previous generation Intel Arria® 10 and Stratix V FPGAs, allowing for efficient implementation of logic functions and easy conversion of IP between the devices.

The ALM block diagram shown in the following figure has eight inputs with a fracturable look-up table (LUT), two dedicated embedded adders, and four dedicated registers.

Figure 10. ALM Block Diagram



Key features and capabilities of the ALM include:

- High register count with 4 registers per 8-input fracturable LUT, operating in conjunction with the new Intel Hyperflex architecture, enables Intel Stratix 10 DX devices to maximize core performance at very high core logic utilization
- Implements select 7-input logic functions, all 6-input logic functions, and two independent functions consisting of smaller LUT sizes (such as two independent 4-input LUTs) to optimize core logic utilization

The Intel Quartus Prime software takes advantage of the ALM logic structure to deliver the highest performance, optimal logic utilization, and lowest compile times. The Intel Quartus Prime software simplifies design reuse as it automatically maps legacy designs into the Intel Stratix 10 ALM architecture.

1.11. Core Clocking

Core clocking in Intel Stratix 10 DX devices makes use of programmable clock tree synthesis.

This technique uses dedicated clock tree routing and switching circuits, and allows the Intel Quartus Prime software to create the exact clock trees required for your design. Clock tree synthesis minimizes clock tree insertion delay, reduces dynamic power dissipation in the clock tree and allows greater clocking flexibility in the core while still maintaining backwards compatibility with legacy global and regional clocking schemes.

The core clock network in Intel Stratix 10 DX devices supports the high-performance Intel Hyperflex core architecture and also supports the hard memory controllers at rates up to 2666 Mbps with a quarter rate transfer to the core. The core clock network is driven by either dedicated clock input pins, or integer I/O PLLs.

1.12. I/O PLLs

Intel Stratix 10 DX devices contain up to 24 integer I/O PLLs (IOPLLs) available for general purpose use in the core fabric and for simplifying the design of external memory interfaces and high-speed LVDS interfaces. The IOPLLs are located in each bank of 48 general purpose I/O, one per I/O bank, adjacent to the hard memory controllers and LVDS SerDes in each I/O bank. This makes it easier to close timing because the IOPLLs are tightly coupled with I/Os that need to use them. The IOPLLs can be used for general purpose applications in the core such as clock network delay compensation and zero-delay clock buffering

1.13. Internal Embedded Memory

Intel Stratix 10 DX devices contain three types of embedded memory blocks: eSRAM (47.25 Mbit), M20K (20 Kb), and MLAB (640 bit). This variety of on-chip memory provides fast access times and low latency for applications such as wide and deep FIFOs and variable buffers. Combined with the in-package memory provided by the HBM2 DRAM stacks in select devices, the internal embedded memory completes the memory hierarchy in Intel Stratix 10 DX devices.

The eSRAM blocks are a new innovation in Intel Stratix 10 devices. These large embedded SRAM blocks are tightly coupled to the core fabric and are directly accessible with no need for a separate memory controller. Each eSRAM block is arranged as 8 channels, 42 banks per channel, with a total capacity of 47.25 Mbits running at clock rates up to 750 MHz. Within the eSRAM block, each channel has a bus width of 72 bit read and 72 bit write, and has one READ and one WRITE per channel. This allows each eSRAM block to support a total aggregate bandwidth (read + write) of up to 864 Gbps.

The eSRAM block is implemented as a simple dual port memory with concurrent read and write access per channel, and includes integrated hard ECC generation and checking. Compared to an off-chip SRAM solution, the eSRAM block allows you to reduce system power and save board space and cost.

The M20K and MLAB blocks are familiar block sizes carried over from previous Intel device families. The MLAB blocks are ideal for wide and shallow memories, while the M20K blocks are intended to support larger memory configurations and include hard ECC. Both M20K and MLAB embedded memory blocks can be configured as a single-port or dual-port RAM, FIFO, ROM, or shift register. These memory blocks are highly flexible and support a number of memory configurations as shown in the table.

Table 10. Internal Embedded Memory Block Configurations

MLAB (640 bits)	M20K (20 Kb)
64 x 10 (supported through emulation) 32 x 20	2K x 10 (or x8) 1K x 20 (or x16) 512 x 40 (or x32)

1.14. Variable Precision DSP Block

The Intel Stratix 10 DX DSP blocks are based upon the Variable Precision DSP Architecture used in Intel's previous generation devices. They feature hard fixed point and IEEE 754 compliant floating point capability.

The DSP blocks can be configured to support signal processing with precision ranging from 18x19 up to 54x54. A pipeline register has been added to increase the maximum operating frequency of the DSP block and reduce power consumption.

Figure 11. DSP Block: Standard Precision Fixed Point Mode

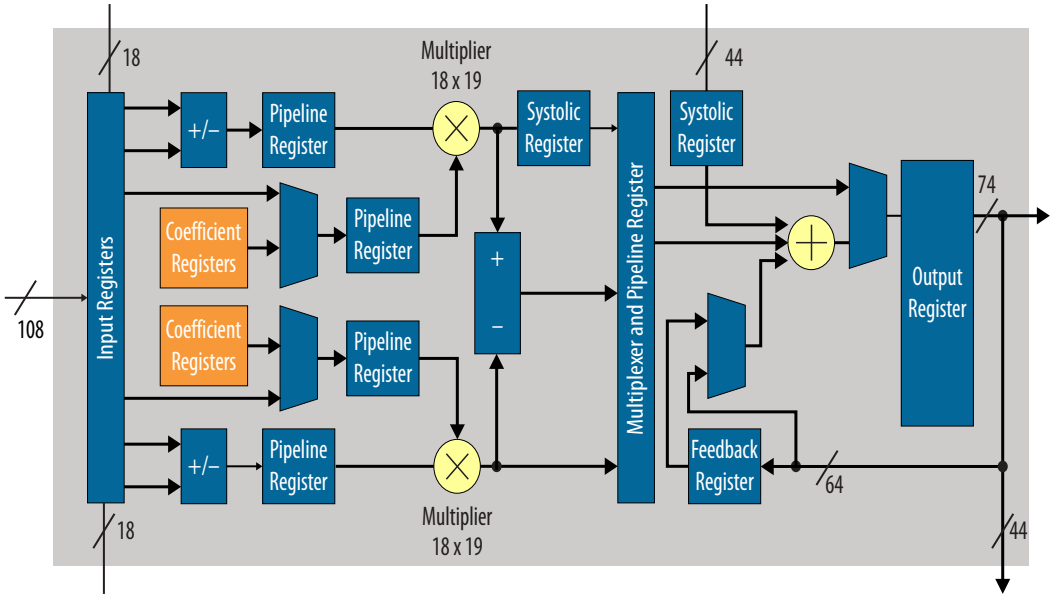


Figure 12. DSP Block: High Precision Fixed Point Mode

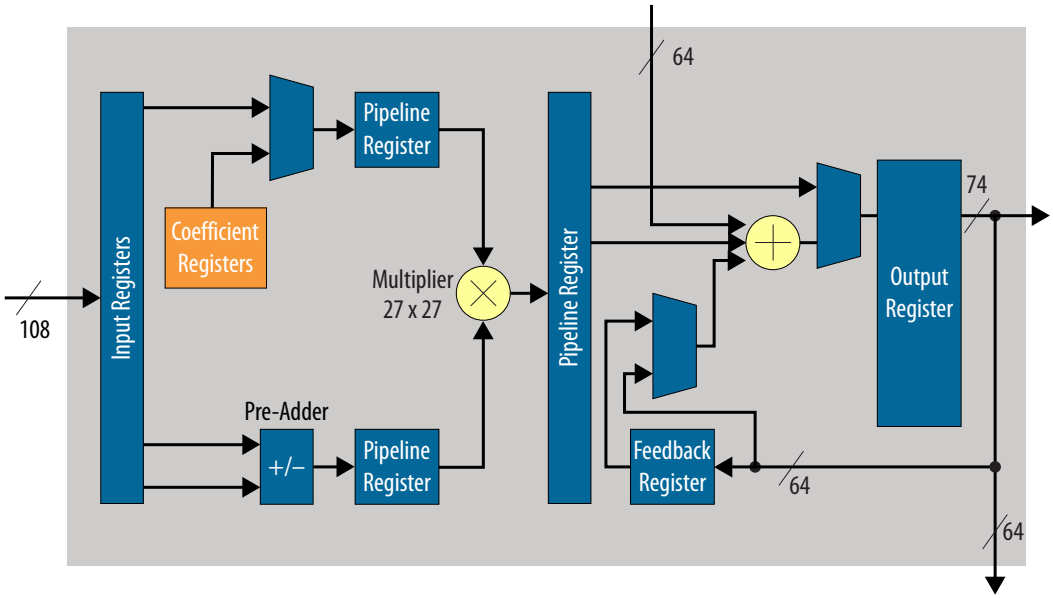
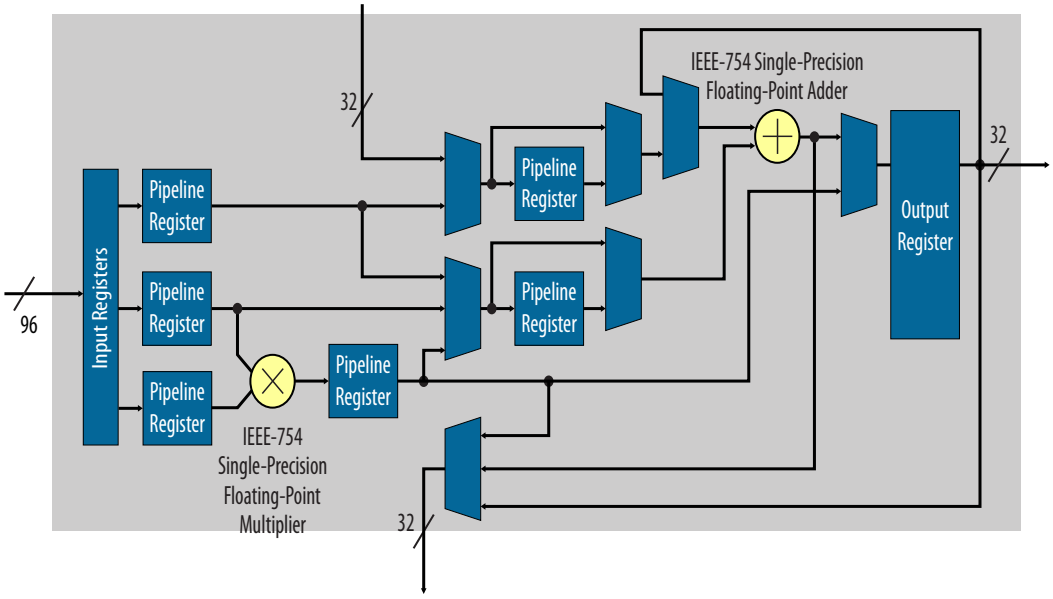


Figure 13. DSP Block: Single Precision Floating Point Mode



Each DSP block can be independently configured at compile time as either dual 18x19 or a single 27x27 multiply accumulate. With a dedicated 64 bit cascade bus, multiple variable precision DSP blocks can be cascaded to implement even higher precision DSP functions efficiently.

In floating point mode, each DSP block provides one single precision floating point multiplier and adder. Floating point additions, multiplications, mult-adds and mult-accumulates are supported.

The following table shows how different precisions are accommodated within a DSP block, or by utilizing multiple blocks.

Table 11. Variable Precision DSP Block Configurations

Multiplier Size	DSP Block Resources	Expected Usage
18x19 bits	1/2 of Variable Precision DSP Block	Medium precision fixed point
27x27 bits	1 Variable Precision DSP Block	High precision fixed point
19x36 bits	1 Variable Precision DSP Block with external adder	Fixed point FFTs
36x36 bits	2 Variable Precision DSP Blocks with external adder	Very high precision fixed point
54x54 bits	4 Variable Precision DSP Blocks with external adder	Double Precision floating point
Single Precision floating point	1 Single Precision floating point adder, 1 Single Precision floating point multiplier	Floating point

Complex multiplication is very common in DSP algorithms. One of the most popular applications of complex multipliers is the FFT algorithm. This algorithm has the characteristic of increasing precision requirements on only one side of the multiplier. The Variable Precision DSP block supports the FFT algorithm with proportional increase in DSP resources as the precision grows.

Table 12. Complex Multiplication With Variable Precision DSP Block

Complex Multiplier Size	DSP Block Resources	FFT Usage
18x19 bits	2 Variable Precision DSP Blocks	Resource optimized FFT
27x27 bits	4 Variable Precision DSP Blocks	Highest precision FFT

For FFT applications with high dynamic range requirements, the Intel FFT IP Core offers an option of single precision floating point implementation with resource usage and performance similar to high precision fixed point implementations.

Other features of the DSP block include:

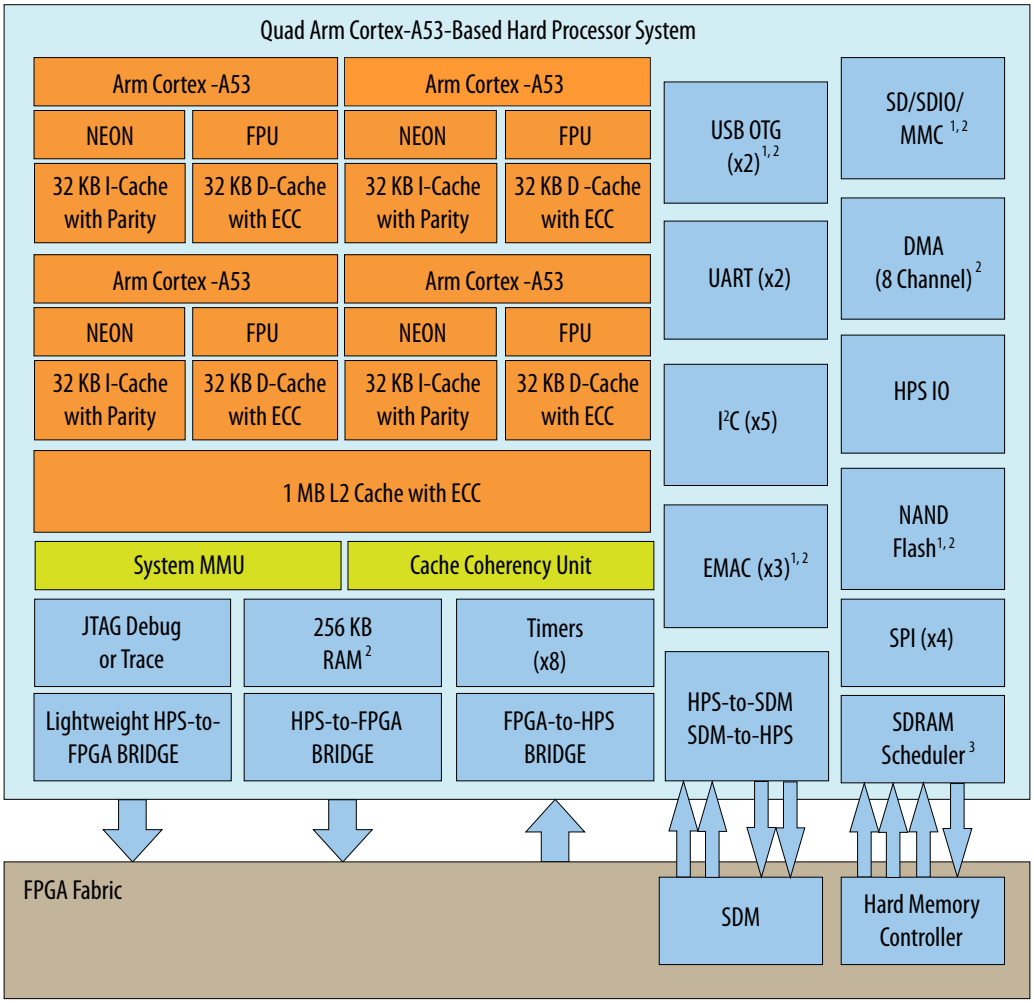
- Hard 18 bit and 25 bit pre-adders
- Hard floating point multipliers and adders
- 64 bit dual accumulator (for separate I, Q product accumulations)
- Cascaded output adder chains for 18 and 27 bit FIR filters
- Embedded coefficient registers for 18 and 27 bit coefficients
- Fully independent multiplier outputs
- Inferability using HDL templates supplied by the Intel Quartus Prime software for most modes

The Variable Precision DSP block is ideal to support the growing trend towards higher bit precision in high performance DSP applications. At the same time, it can efficiently support the many existing 18 bit DSP applications, such as high definition video processing and remote radio heads. With the Variable Precision DSP block architecture and hard floating point multipliers and adders, Intel Stratix 10 DX devices can efficiently support many different precision levels up to and including floating point implementations. This flexibility can result in increased system performance, reduced power consumption, and reduce architecture constraints on system algorithm designers.

1.15. Hard Processor System (HPS)

The Hard Processor System (HPS) in select Intel Stratix 10 DX devices is Intel's third generation HPS. Leveraging the performance of Intel 14 nm tri-gate technology, the HPS provides more than double the performance of previous generation devices with an integrated quad-core 64-bit Arm Cortex-A53. The HPS also enables system-wide hardware virtualization capabilities by adding a system memory management unit.

Figure 14. HPS Block Diagram



Notes:
1. Integrated direct memory access (DMA)
2. Integrated error correction code (ECC)
3. Multiport front-end interface to hard memory controller

1.15.1. Key Features of the Intel Stratix 10 HPS

Table 13. Key Features of the Intel Stratix 10 HPS

Feature	Description
Quad-core Arm Cortex-A53 MPCore processor unit	• 2.3 MIPS/MHz instruction efficiency • CPU frequency up to 1.5 GHz • At 1.5 GHz total performance of 13,800 MIPS • Armv8-A architecture • Runs 64-bit and 32-bit Arm instructions • 16-bit and 32-bit Thumb instructions for 30% reduction in memory footprint • Jazelle® RCT execution architecture with 8 bit Java bytecodes

continued...

Feature	Description
	• Superscalar, variable length, out-of-order pipeline with dynamic branch prediction • Improved Arm NEON™ media processing engine • Single- and double-precision floating-point unit • CoreSight™ debug and trace technology
System Memory Management Unit	• Enables a unified memory model and extends hardware virtualization into peripherals implemented in the FPGA fabric
Cache Coherency unit	• Changes in shared data stored in cache are propagated throughout the system providing bi-directional coherency for co-processing elements.
Cache	• L1 Cache — 32 KB of instruction cache w/ parity check — 32 KB of L1 data cache w /ECC — Parity checking • L2 Cache — 1MB shared — 8-way set associative — SEU Protection with parity on TAG ram and ECC on data RAM — Cache lockdown support
On-Chip Memory	• 256 KB of scratch on-chip RAM
External SDRAM and Flash Memory Interfaces for HPS	• Hard memory controller with support for DDR4, DDR3 — 40 bit (32 bit + 8 bit ECC) with select packages supporting 72 bit (64 bit + 8 bit ECC) — Support for up to 2666 Mbps DDR4 and 2166 Mbps DDR3 frequencies — Error correction code (ECC) support including calculation, error correction, write-back correction, and error counters — Software Configurable Priority Scheduling on individual SDRAM bursts — Fully programmable timing parameter support for all JEDEC-specified timing parameters — Multiport front-end (MPFE) scheduler interface to the hard memory controller, which supports the AXI® Quality of Service (QoS) for interface to the FPGA fabric • NAND flash controller — ONFI 1.0 — Integrated descriptor based with DMA — Programmable hardware ECC support — Support for 8 and 16 bit Flash devices • Secure Digital SD/SDIO/MMC controller — eMMC 4.5 — Integrated descriptor based DMA — CE-ATA digital commands supported — 50 MHz operating frequency • Direct memory access (DMA) controller — 8-channel — Supports up to 32 peripheral handshake interface

continued...

Feature	Description
Communication Interface Controllers	• Three 10/100/1000 Ethernet media access controls (MAC) with integrated DMA — Supports RGMII and RMII external PHY Interfaces — Option to support other PHY interfaces through FPGA logic • GMII • MII • RMII (requires MII to RMII adapter) • RGMII (requires GMII to RGMII adapter) • SGMII (requires GMII to SGMII adapter) — Supports IEEE 1588-2002 and IEEE 1588-2008 standards for precision networked clock synchronization — Supports IEEE 802.1Q VLAN tag detection for reception frames — Supports Ethernet AVB standard • Two USB On-the-Go (OTG) controllers with DMA — Dual-Role Device (device and host functions) • High-speed (480 Mbps) • Full-speed (12 Mbps) • Low-speed (1.5 Mbps) • Supports USB 1.1 (full-speed and low-speed) — Integrated descriptor-based scatter-gather DMA — Support for external ULPI PHY — Up to 16 bidirectional endpoints, including control endpoint — Up to 16 host channels — Supports generic root hub — Configurable to OTG 1.3 and OTG 2.0 modes • Five I^2C controllers (three can be used by EMAC for MIO to external PHY) — Support both 100 Kbps and 400 Kbps modes — Support both 7 bit and 10 bit addressing modes — Support Master and Slave operating mode • Two UART 16550 compatible — Programmable baud rate up to 115.2 Kbaud • Four serial peripheral interfaces (SPI) (2 Masters, 2 Slaves) — Full and Half duplex
Timers and I/O	• Timers — 4 general-purpose timers — 4 watchdog timers • 48 HPS direct I/O allow HPS peripherals to connect directly to I/O • Up to three IO48 banks may be assigned to HPS for HPS DDR access
Interconnect to Logic Core	• FPGA-to-HPS Bridge — Allows IP bus masters in the FPGA fabric to access to HPS bus slaves — Configurable 32, 64, or 128 bit AMBA AXI interface • HPS-to-FPGA Bridge — Allows HPS bus masters to access bus slaves in FPGA fabric — Configurable 32, 64, or 128 bit AMBA AXI interface allows high-bandwidth HPS master transactions to FPGA fabric • HPS-to-SDM and SDM-to-HPS Bridges — Allows the HPS to reach the SDM block and the SDM to bootstrap the HPS • Light Weight HPS-to-FPGA Bridge — Light weight 32 bit AXI interface suitable for low-latency register accesses from HPS to soft peripherals in FPGA fabric • FPGA-to-HPS SDRAM Bridge — Up to three AMBA AXI interfaces supporting 32, 64, or 128 bit data paths

1.16. Power Management

Intel Stratix 10 DX devices use the advanced Intel 14 nm tri-gate process technology, the all new Intel Hyperflex core architecture to enable Hyper-Folding, power gating, and optional power reduction techniques to reduce total power consumption by as much as 70% compared to previous generation high-performance Stratix V devices.

Intel Stratix 10 standard power devices (-V) are SmartVID devices. The core voltage supplies (VCC and VCCP) for each SmartVID device must be driven by a PMBus voltage regulator dedicated to that Intel Stratix 10 device. Use of a PMBus voltage regulator for each SmartVID (-V) device is mandatory; it is not an option. A code is programmed into each SmartVID device during manufacturing that allows the PMBus voltage regulator to operate at the optimum core voltage to meet the device performance specifications.

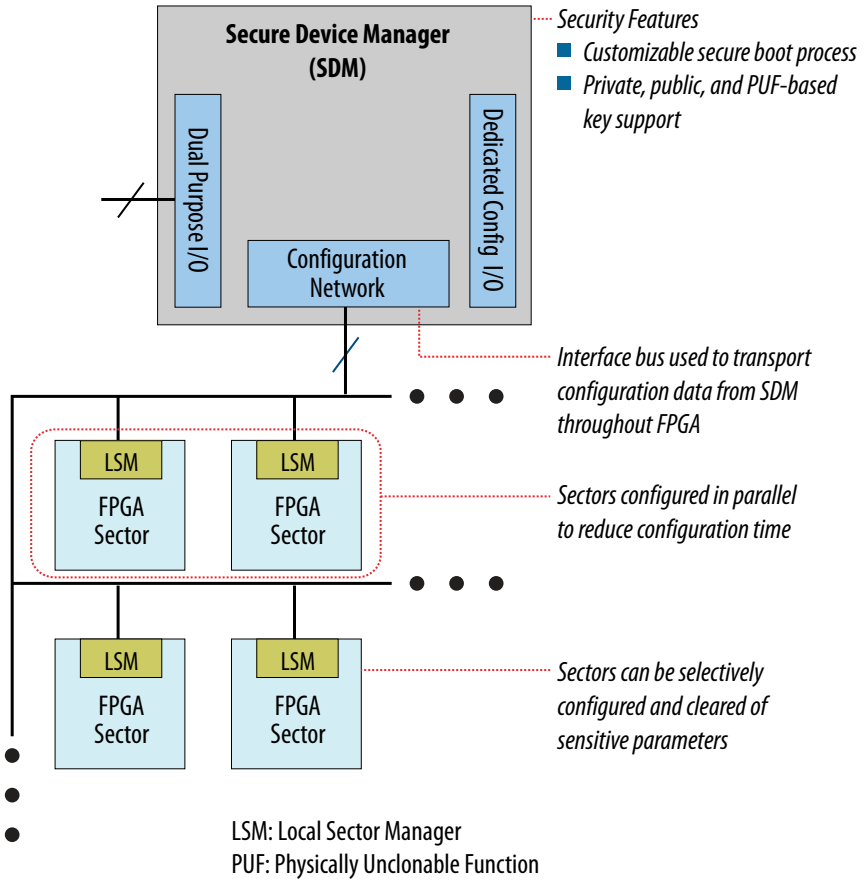
With the new Intel Hyperflex core architecture, designs can run faster than previous generation FPGAs. With faster performance and same required throughput, architects can reduce the width of the data path to save power. This optimization is called Hyper-Folding. Additionally, power gating reduces static power of unused resources in the FPGA by powering them down. The Intel Quartus Prime software automatically powers down specific unused resource blocks such as DSP and M20K blocks, at configuration time.

Furthermore, Intel Stratix 10 DX devices feature Intel's low power transceivers and include a number of hard IP blocks that not only reduce logic resources but also deliver substantial power savings compared to soft implementations. In general, hard IP blocks consume up to 50% less power than the equivalent soft logic implementations.

1.17. Device Configuration and Secure Device Manager (SDM)

All Intel Stratix 10 DX devices contain a Secure Device Manager (SDM), which is a dedicated triple-redundant processor that serves as the point of entry into the device for all JTAG and configuration commands. The SDM also bootstraps the HPS in SoC devices ensuring that the HPS can boot using the same security features that the FPGA devices have.

Figure 15. SDM Block Diagram



During configuration, Intel Stratix 10 DX devices are divided into logical sectors, each of which is managed by a local sector manager (LSM). The SDM passes configuration data to each of the LSMs across the on-chip configuration network. This allows the sectors to be configured independently, one at a time, or in parallel. This approach achieves simplified sector configuration and reconfiguration, as well as reduced overall configuration time due to the inherent parallelism. The same sector-based approach is used to respond to single-event upsets and security attacks.

While the sectors provide a logical separation for device configuration and reconfiguration, they overlay the normal rows and columns of FPGA logic and routing. This means there is no impact to the Intel Quartus Prime software place and route, and no impact to the timing of logic signals that cross the sector boundaries.

The SDM enables robust, secure, fully-authenticated device configuration. It also allows for customization of the configuration scheme, which can enhance device security. For configuration and reconfiguration, this approach offers a variety of advantages:

- Dedicated secure configuration manager
- Reduced device configuration time, because sectors are configured in parallel
- Updateable configuration process
- Reconfiguration of one or more sectors independent of all other sectors
- Zeroization of individual sectors or the complete device

1.18. Device Security

Building on top of the robust security features present in the previous generation devices, Intel Stratix 10 DX devices include a number of new and innovative security enhancements. These features are also managed by the SDM, tightly coupling device configuration and reconfiguration with encryption, authentication, key storage and anti-tamper services.

Security services provided by the SDM include:

- Bitstream encryption
- Multi-factor authentication
- Hard encryption and authentication acceleration; AES-256, SHA-256/384, ECDSA-256/384
- Volatile and non-volatile encryption key storage and management
- Physically Unclonable Function (PUF) service
- Updateable configuration process
- Secure device maintenance and upgrade functions
- Side channel attack protection
- Scripted response to sensor inputs and security attacks, including selective sector zeroization
- Readback, JTAG and test mode disable
- Enhanced response to single-event upsets (SEU)
- Black key provisioning
- Physical anti-tamper

See the *Intel Stratix 10 Device Security User Guide* for a complete list of all security features.

The SDM and associated security services provide a robust, multi-layered security solution for your Intel Stratix 10 DX design.

Table 14. Device Security

Intel Stratix 10 Family Variant	Bitstream Authentication	Advanced Security Features[6]
DX	All devices	All devices

Related Information

- My Intel Support
- Intel Stratix 10 Device Security User Guide

1.19. Configuration via Protocol Using PCI Express

Configuration via protocol using PCI Express allows the FPGA to be configured across the PCI Express bus, simplifying the board layout and increasing system integration. Making use of the embedded PCI Express hard IP operating in autonomous mode before the FPGA is configured, this technique allows the PCI Express bus to be powered up and active within the 100 ms time allowed by the PCI Express specification. Intel Stratix 10 DX devices also support partial reconfiguration across the PCI Express bus which reduces system down time by keeping the PCI Express link active while the device is being reconfigured.

1.20. Partial and Dynamic Reconfiguration

Partial reconfiguration allows you to reconfigure part of the FPGA while other sections continue running. This capability is required in systems where uptime is critical, because it allows you to make updates or adjust functionality without disrupting services.

In addition to lowering power and cost, partial reconfiguration also increases the effective logic density by removing the necessity to place in the FPGA those functions that do not operate simultaneously. Instead, these functions can be stored in external memory and loaded as needed. This reduces the size of the required FPGA by allowing multiple applications on a single FPGA, saving board space and reducing power. The partial reconfiguration process is built on top of the proven incremental compile design flow in the Intel Quartus Prime design software

Dynamic reconfiguration in Intel Stratix 10 DX devices allows transceiver data rates, protocols and analog settings to be changed dynamically on a channel-by-channel basis while maintaining data transfer on adjacent transceiver channels. Dynamic reconfiguration is ideal for applications that require on-the-fly multiprotocol or multi-rate support. Both the PMA and PCS blocks within the transceiver can be reconfigured using this technique. Dynamic reconfiguration of the transceivers can be used in conjunction with partial reconfiguration of the FPGA to enable partial reconfiguration of both core and transceivers simultaneously.

1.21. Fast Forward Compile

The innovative Fast Forward Compile feature in the Intel Quartus Prime software identifies performance bottlenecks in your design and provides detailed, step-by-step performance improvement recommendations that you can then implement. The Compiler reports estimates of the maximum operating frequency that can be achieved

(6) Contact My Intel Support for additional information.

by applying the recommendations. As part of the new Hyper-Aware design flow, Fast Forward Compile maximizes the performance of your Intel Stratix 10 DX design and achieves rapid timing closure.

Previously, this type of optimization required multiple time-consuming design iterations, including full design re-compilation to determine the effectiveness of the changes. Fast Forward Compile enables you to make better decisions about where to focus your optimization efforts, and how to increase your design performance and throughput. This technique removes much of the guesswork of performance exploration, resulting in fewer design iterations.

1.22. Single Event Upset (SEU) Error Detection and Correction

Intel Stratix 10 DX devices offer robust SEU error detection and correction circuitry. The detection and correction circuitry includes protection for Configuration RAM (CRAM) programming bits and user memories. The CRAM is protected by a continuously running parity checker circuit with integrated ECC that automatically corrects one or two bit errors and detects higher order multibit errors.

The physical layout of the CRAM array is optimized to make the majority of multi-bit upsets appear as independent single-bit or double-bit errors which are automatically corrected by the integrated CRAM ECC circuitry. In addition to the CRAM protection, user memories also include integrated ECC circuitry and are layout optimized for error detection and correction.

The SEU error detection and correction hardware is supported by both soft IP and the Intel Quartus Prime software to provide a complete SEU mitigation solution. The components of the complete solution include:

- Hard error detection and correction for CRAM and user eSRAM and M20K memory blocks
- Optimized physical layout of memory cells to minimize probability of SEU
- Sensitivity processing soft IP that reports if CRAM upset affects a used or unused bit
- Fault injection soft IP with the Intel Quartus Prime software support that changes state of CRAM bits for testing purposes
- Hierarchy tagging in the Intel Quartus Prime software
- Triple Mode Redundancy (TMR) used for the Secure Device Manager and critical on-chip state machines

In addition to the SEU mitigation features listed above, the Intel 14 nm tri-gate process technology used for Intel Stratix 10 DX devices is based on FinFET transistors which have reduced SEU susceptibility versus conventional planar transistors.

1.23. Document Revision History for the Intel Stratix 10 DX Device Overview

Document Version	Changes
2020.03.24	Made the following changes: • Added advanced security (-AS) devices. • Added Intel Optane memory support.
2019.09.19	Initial release.

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Year Established	2018
Main Markets	North America South Asia Western Europe

sales@fpgamall.com +00852-56428680