THE DATASHEET OF FPGA

APEX II

Programmable Logic Device Family

August 2002, ver. 3.0 Data Sheet

Features...

- Programmable logic device (PLD) manufactured using a 0.15-µm all-layer copper-metal fabrication process (up to eight layers of metal)
  - 1-gigabit per second (Gbps) True-LVDS™, LVPECL, pseudo current mode logic (PCML), and HyperTransport™ interface
  - Clock-data synchronization (CDS) in True-LVDS interface to correct any fixed clock-to-data skew
  - Enables common networking and communications bus I/O standards such as RapidIO™, CSIX, Utopia IV, and POS-PHY Level 4
  - Support for high-speed external memory interfaces, including zero bus turnaround (ZBT), quad data rate (QDR), and double data rate (DDR) static RAM (SRAM), and single data rate (SDR) and DDR synchronous dynamic RAM (SDRAM)
  - 30% to 40% faster design performance than APEX™ 20KE devices on average
  - Enhanced 4,096-bit embedded system blocks (ESBs) implementing first-in first-out (FIFO) buffers, Dual-Port+ RAM (bidirectional dual-port RAM), and content-addressable memory (CAM)
  - High-performance, low-power copper interconnect
  - Fast parallel byte-wide synchronous device configuration
  - Look-up table (LUT) logic available for register-intensive functions
- High-density architecture
  - 1,900,000 to 5,250,000 maximum system gates (see Table 1)
  - Up to 67,200 logic elements (LEs)
  - Up to 1,146,880 RAM bits that can be used without reducing available logic
- Low-power operation design
  - 1.5-V supply voltage
  - Copper interconnect reduces power consumption
  - MultiVolt™ I/O support for 1.5-V, 1.8-V, 2.5-V, and 3.3-V interfaces
  - ESBs offer programmable power-saving mode

Table 1. APEX II Device Features

Feature	EP2A15	EP2A25	EP2A40	EP2A70
Maximum gates	1,900,000	2,750,000	3,000,000	5,250,000
Typical gates	600,000	900,000	1,500,000	3,000,000
LEs	16,640	24,320	38,400	67,200
RAM ESBs	104	152	160	280
Maximum RAM bits	425,984	622,592	655,360	1,146,880
True-LVDS channels	36 *(1)*	36 *(1)*	36 *(1)*	36 *(1)*
Flexible-LVDS™ channels *(2)*	56	56	88	88
True-LVDS PLLs *(3)*	4	4	4	4
General-purpose PLL outputs *(4)*	8	8	8	8
Maximum user I/O pins	492	612	735	1,060

Notes to Table 1:

(1) Each device has 36 input channels and 36 output channels.
(2) EP2A15 and EP2A25 devices have 56 input and 56 output channels; EP2A40 and EP2A70 devices have 88 input and 88 output channels.
(3) PLL: phase-locked loop. True-LVDS PLLs are dedicated to implement True-LVDS functionality.
(4) Two internal outputs per PLL are available. Additionally, the device has one external output per PLL pair (two external outputs per device).

…and More Features

- I/O features
  - Up to 380 Gbps of I/O capability
  - 1-Gbps True-LVDS, LVPECL, PCML, and HyperTransport support on 36 input and 36 output channels that feature clock synchronization circuitry and independent clock multiplication and serialization/deserialization factors
  - Common networking and communications bus I/O standards such as RapidIO, CSIX, Utopia IV, and POS-PHY Level 4 enabled
  - 400-megabits per second (Mbps) Flexible-LVDS and HyperTransport support on up to 88 input and 88 output channels (input channels also support LVPECL)
  - Support for high-speed external memories, including ZBT, QDR, and DDR SRAM, and SDR and DDR SDRAM
  - Compliant with peripheral component interconnect Special Interest Group (PCI SIG) ***PCI Local Bus Specification, Revision 2.2*** for 3.3-V operation at 33 or 66 MHz and 32 or 64 bits
  - Compliant with 133-MHz PCI-X specifications
  - Support for other advanced I/O standards, including AGP, CTT, SSTL-3 and SSTL-2 Class I and II, GTL+, and HSTL Class I and II
  - Six dedicated registers in each I/O element (IOE): two input registers, two output registers, and two output-enable registers
  - Programmable bus hold feature
  - Programmable pull-up resistor on I/O pins available during user mode

  - Programmable output drive for 3.3-V LVTTL at 4 mA, 12 mA, 24 mA, or I/O standard levels
  - Programmable output slew-rate control reduces switching noise
  - Hot-socketing operation supported
  - Pull-up resistor on I/O pins before and during configuration
- Enhanced internal memory structure
  - High-density 4,096-bit ESBs
  - Dual-Port+ RAM with bidirectional read and write ports
  - Support for many other memory functions, including CAM, FIFO, and ROM
  - ESB packing mode partitions one ESB into two 2,048-bit blocks
- Device configuration
  - Fast byte-wide synchronous configuration minimizes in-circuit reconfiguration time
  - Device configuration supports multiple voltages (either 3.3 V and 2.5 V or 1.8 V)
- Flexible clock management circuitry with eight general-purpose PLL outputs
  - Four general-purpose PLLs with two outputs per PLL
  - Built-in low-skew clock tree
  - Eight global clock signals
  - ClockLock™ feature reducing clock delay and skew
  - ClockBoost™ feature providing clock multiplication (by 1 to 160) and division (by 1 to 256)
  - ClockShift™ feature providing programmable clock phase and delay shifting with coarse (90°, 180°, or 270°) and fine (0.5 to 1.0 ns) resolution
- Advanced interconnect structure
  - All-layer copper interconnect for high performance
  - Four-level hierarchical FastTrack® interconnect structure for fast, predictable interconnect delays
  - Dedicated carry chain that implements arithmetic functions such as fast adders, counters, and comparators (automatically used by software tools and megafunctions)
  - Dedicated cascade chain that implements high-speed, high-fan-in logic functions (automatically used by software tools and megafunctions)
  - Interleaved local interconnect allowing one LE to drive 29 other LEs through the fast local interconnect
- Advanced software support
  - Software design support and automatic place-and-route provided by the Altera® Quartus™ II development system for Windows-based PCs, Sun SPARCstations, and HP 9000 Series 700/800 workstations
  - Altera MegaCore® functions and Altera Megafunction Partners Program (AMPP℠) megafunctions optimized for APEX II architecture

- LogicLock™ incremental design for intellectual property (IP) integration and team-based design
- NativeLink™ integration with popular synthesis, simulation, and timing analysis tools
- SignalTap® embedded logic analyzer simplifies in-system design evaluation by giving access to internal nodes during device operation
- Support for popular revision-control software packages, including PVCS, RCS, and SCCS

Tables 2 and 3 show the APEX II ball-grid array (BGA) and FineLine BGA™ device package sizes, options, and I/O pin counts.

Table 2. APEX II Package Sizes

Feature	672-Pin FineLine BGA	724-Pin BGA	1,020-Pin FineLine BGA	1,508-Pin FineLine BGA
Pitch (mm)	1.00	1.27	1.00	1.00
Area (mm^2)	729	1,225	1,089	1,600
Length × Width (mm × mm)	27 × 27	35 × 35	33 × 33	40 × 40

Table 3. APEX II Package Options & I/O Pin Count *Notes (1), (2)*

Feature	672-Pin FineLine BGA	724-Pin BGA	1,020-Pin FineLine BGA	1,508-Pin FineLine BGA
EP2A15	492	492		
EP2A25	492	536		
EP2A40	492	536	735	
EP2A70		536		1,060

Notes to Table 3:

(1) All APEX II devices support vertical migration within the same package (e.g., the designer can migrate between the EP2A15, EP2A25, and EP2A40 devices in the 672-pin FineLine BGA package). Vertical migration means that designers can migrate to devices whose dedicated pins, configuration pins, LVDS pins, and power pins are the same for a given package across device densities. Migration of I/O pins across densities requires the designer to cross reference the available I/O pins using the device pin-outs. This must be done for all planned densities for a given package type to identify which I/O pins are migratable.

(2) I/O pin counts include dedicated clock and fast I/O pins.

General Description

APEX II devices integrate high-speed differential I/O support using the True-LVDS interface. The dedicated serializer, deserializer, and CDS circuitry in the True-LVDS interface support the LVDS, LVPECL, HyperTransport, and PCML I/O standards. Flexible-LVDS pins located in regular user I/O banks offer additional differential support, increasing the total device bandwidth. This circuitry, together with enhanced IOEs and support for numerous I/O standards, allows APEX II devices to meet high-speed interface requirements.

APEX II devices also include other high-performance features such as bidirectional dual-port RAM, CAM, general-purpose PLLs, and numerous global clocks.

Configuration

The logic, circuitry, and interconnects in the APEX II architecture are configured with CMOS SRAM elements. APEX II devices are reconfigurable and are 100% tested prior to shipment. As a result, test vectors do not have to be generated for fault coverage. Instead, the designer can focus on simulation and design verification. In addition, the designer does not need to manage inventories of different ASIC designs; APEX II devices can be configured on the board for the specific functionality required.

APEX II devices are configured at system power-up with data either stored in an Altera configuration device or provided by a system controller. Altera offers in-system programmability (ISP)-capable configuration devices, which configure APEX II devices via a serial data stream. The enhanced configuration devices can configure any APEX II device in under 100 ms. Moreover, APEX II devices contain an optimized interface that permits microprocessors to configure APEX II devices serially or in parallel, synchronously or asynchronously. This interface also enables microprocessors to treat APEX II devices as memory and to configure the device by writing to a virtual memory location, simplifying reconfiguration.

APEX II devices also support a new byte-wide, synchronous configuration scheme at speeds of up to 66 MHz using EPC16 configuration devices or a microprocessor. This parallel configuration reduces configuration time by using eight data lines to send configuration data versus one data line in serial configuration.

APEX II devices support multi-voltage configuration; device configuration can be performed at 3.3 V and 2.5 V or 1.8 V.

After an APEX II device has been configured, it can be reconfigured in-circuit by resetting the device and loading new data. Real-time changes can be made during system operation, enabling innovative reconfigurable computing applications.

Software

APEX II devices are supported by the Altera Quartus II development system: a single, integrated package that offers hardware description language (HDL) and schematic design entry, compilation and logic synthesis, full simulation and worst-case timing analysis, SignalTap logic analysis, and device configuration. The Quartus II software runs on Windows-based PCs, Sun SPARCstations, and HP 9000 Series 700/800 workstations.

The Quartus II software includes the LogicLock incremental design feature. The LogicLock feature allows the designer to make pin and timing assignments, verify functionality and performance, and then set constraints to lock down the placement and performance of a specific block of logic using LogicLock constraints. Constraints set by the LogicLock function guarantee repeatable placement when implementing a block of logic in a current project or exporting the block to another project. The constraints set by the LogicLock feature can lock down logic to a fixed location in the device. The LogicLock feature can also lock the logic down to a floating location, and the Quartus II software determines the best relative placement of the block to meet design requirements. Adding additional logic to a project will not affect the performance of blocks locked down with LogicLock constraints.

The Quartus II software provides NativeLink interfaces to other industry-standard PC- and UNIX workstation-based EDA tools. For example, designers can open the Quartus II software from within third-party design tools. The Quartus II software also contains built-in optimized synthesis libraries; synthesis tools can use these libraries to optimize designs for APEX II devices. For example, the Synopsys Design Compiler library, supplied with the Quartus II development system, includes DesignWare functions optimized for the APEX II architecture.

Functional Description

APEX II devices incorporate LUT-based logic, product-term-based logic, memory, and high-speed I/O standards into one device. Signal interconnections within APEX II devices (as well as to and from device pins) are provided by the FastTrack interconnect—a series of fast, continuous row and column channels that run the entire length and width of the device.

Each I/O pin is fed by an IOE located at the end of each row and column of the FastTrack interconnect. Each IOE contains a bidirectional I/O buffer and six registers that can be used for registering input, output, and output-enable signals. When used with a dedicated clock pin, these registers provide exceptional performance and interface support with external memory devices such as DDR SDRAM and ZBT and QDR SRAM devices.

IOEs provide a variety of features such as: 3.3-V, 64-bit, 66-MHz PCI compliance, 3.3-V, 64-bit, 133-MHz PCI-X compliance, Joint Test Action Group (JTAG) boundary-scan test (BST) support, output drive strength control, slew-rate control, tri-state buffers, bus-hold circuitry, programmable pull-up resistors, programmable input and output delays, and open-drain outputs.

APEX II devices offer enhanced I/O support, including support for 1.5 V, 1.8 V, 2.5 V, 3.3 V, LVCMOS, LVTTL, HSTL, LVDS, LVPECL, HyperTransport, PCML, 3.3-V PCI, PCI-X, GTL+, SSTL-2, SSTL-3, CTT, and 3.3-V AGP I/O standards. High-speed (up to 1.0 Gbps) differential transfers are supported with True-LVDS circuitry for LVDS, LVPECL, HyperTransport, and PCML I/O standards. The optional CDS feature corrects any clock-to-data skew at the True-LVDS receiver channels, allowing for flexible board topologies. Up to 88 Flexible-LVDS channels support differential transfer at up to 400 Mbps (DDR) for LVDS and HyperTransport I/O standards.

An ESB can implement many types of memory, including Dual-Port+ RAM, CAM, ROM, and FIFO functions. Embedding the memory directly into the die improves performance and reduces die area compared to distributed-RAM implementations. The abundance of cascadable ESBs ensures that the APEX II device can implement multiple wide memory blocks for high-density designs. The ESB's high speed ensures it can implement small memory blocks without any speed penalty. The abundance of ESBs, in conjunction with the ability for one ESB to implement two separate memory blocks, ensures that designers can create as many different-sized memory blocks as the system requires.

Figure 1 shows an overview of the APEX II device.

Figure 1. APEX II Device Block Diagram

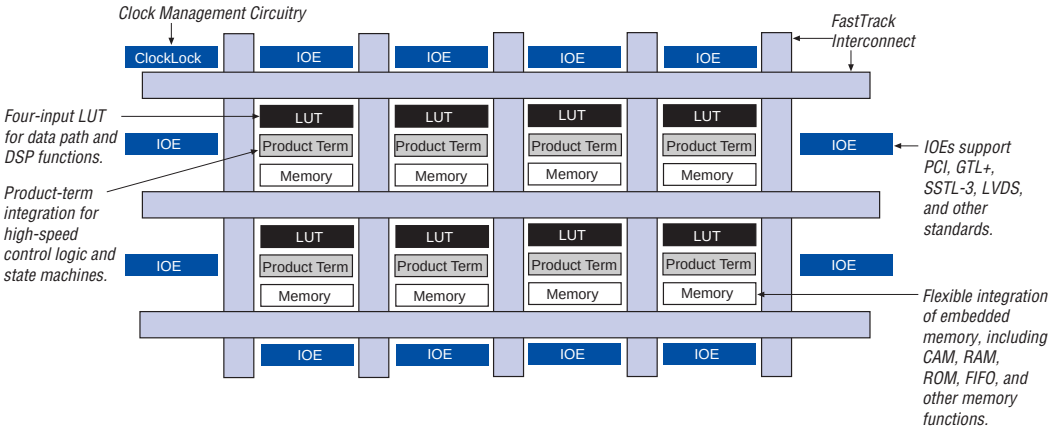


Table 4 lists the resources available in APEX II devices.

Table 4. APEX II Device Resources

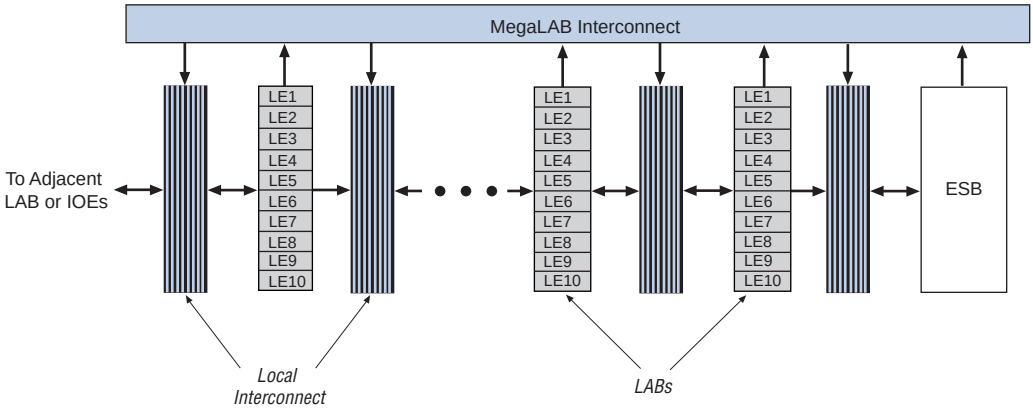
Device	MegaLAB Rows	MegaLAB Columns	ESBs
EP2A15	26	4	104
EP2A25	38	4	152
EP2A40	40	4	160
EP2A70	70	4	280

APEX II devices provide eight dedicated clock input pins and four dedicated fast I/O pins that globally drive register control inputs, including clocks. These signals ensure efficient distribution of high-speed, low-skew control signals. The control signals use dedicated routing channels to provide short delays and low skew. The dedicated fast signals can also be driven by internal logic, providing an ideal solution for a clock divider or internally-generated asynchronous control signal with high fan-out. The dedicated clock and fast I/O pins on APEX II devices can also feed logic. Dedicated clocks can also be used with the APEX II general-purpose PLLs for clock management.

MegaLAB Structure

APEX II devices are constructed from a series of MegaLAB™ structures. Each MegaLAB structure contains a group of logic array blocks (LABs), one ESB, and a MegaLAB interconnect, which routes signals within the MegaLAB structure. EP2A15 and EP2A25 devices have 16 LABs and EP2A40 and EP2A70 devices have 24 LABs. Signals are routed between MegaLAB structures and I/O pins via the FastTrack interconnect. In addition, edge LABs can be driven by I/O pins through the local interconnect. Figure 2 shows the MegaLAB structure.

Figure 2. MegaLAB Structure



Logic Array Block

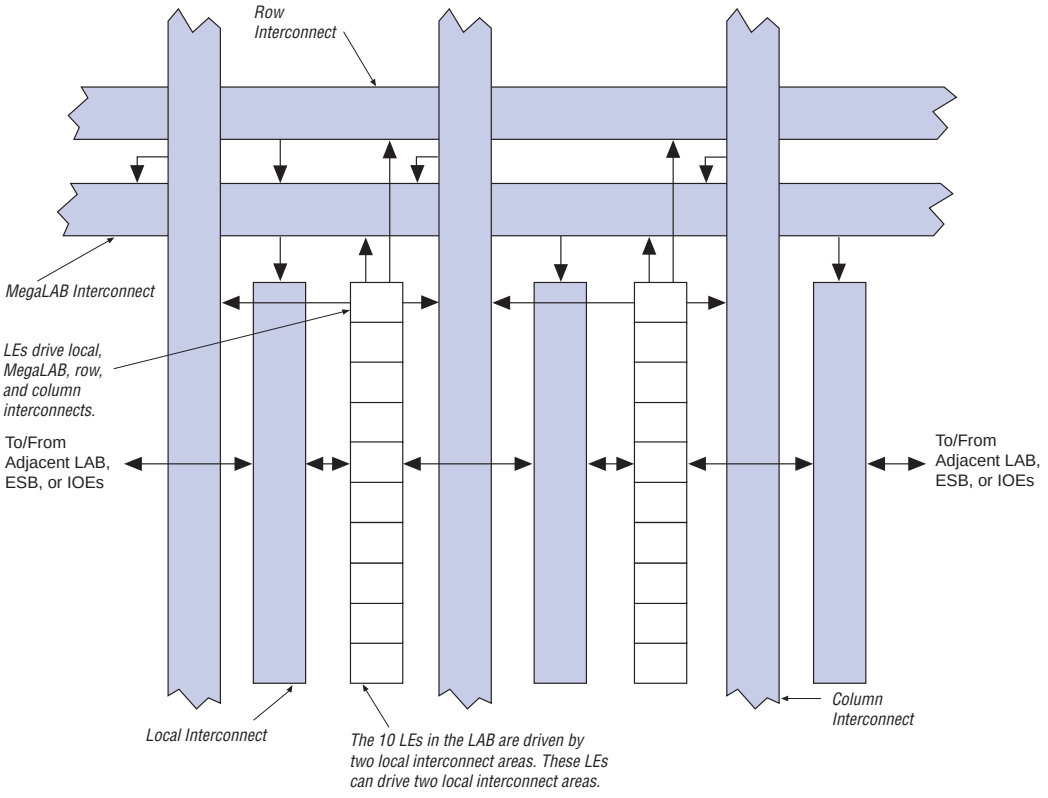
Each LAB consists of 10 LEs, the LEs' associated carry and cascade chains, LAB control signals, and the local interconnect. The local interconnect transfers signals between LEs in the same or adjacent LABs, IOEs, or ESBs.

The Quartus II Compiler places associated logic within a LAB or adjacent LABs, allowing the use of a fast local interconnect for high performance.

APEX II devices use an interleaved LAB structure, so that each LAB can drive two local interconnect areas. Every other LE drives to either the left or right local interconnect area, alternating by LE. The local interconnect can drive LEs within the same LAB or adjacent LABs. This feature minimizes the use of the row and column interconnects, providing higher performance and flexibility. Each LAB structure can drive 30 LEs through fast local interconnects.

Figure 3 shows the APEX II LAB.

Figure 3. APEX II LAB Structure

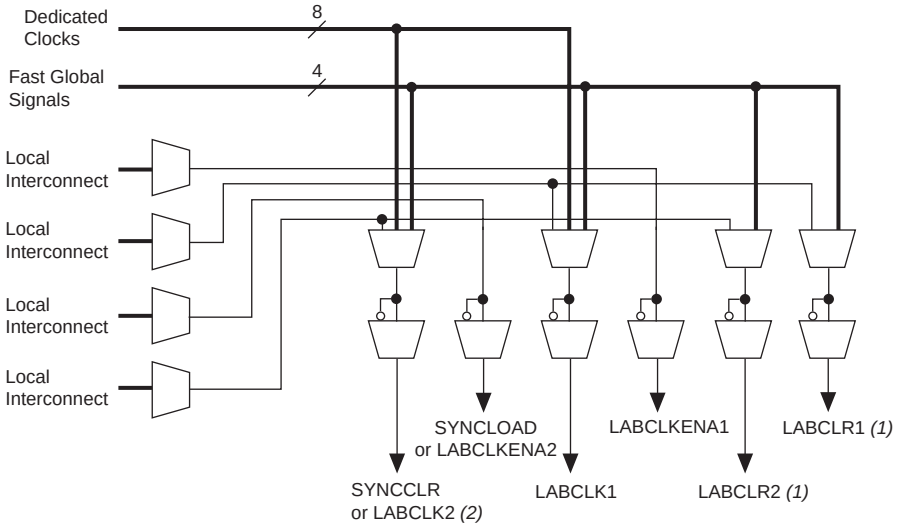


Each LAB contains dedicated logic for driving control signals to its LEs and ESBs. The control signals include clock, clock enable, asynchronous clear, asynchronous preset, asynchronous load, synchronous clear, and synchronous load signals. A maximum of six control signals can be used at a time. Although synchronous load and clear signals are generally used when implementing counters, they can also be used with other functions.

Each LAB can use two clocks and two clock enable signals. The LAB's clock and clock enable signals are linked (e.g., any LE in a particular LAB using `CLK1` will also use `CLKENA1`). LEs with the same clock but different clock enable signals either use both clock signals in one LAB or are placed into separate LABs. If both the rising and falling edges of a clock are used in an LAB, both LAB-wide clock signals are used.

The LAB-wide control signals can be generated from the LAB local interconnect, global signals, and dedicated clock pins. The inherent low skew of the FastTrack interconnect enables it to be used for clock distribution. Figure 4 shows the LAB control signal generation circuit.

Figure 4. LAB Control Signal Generation



Notes to Figure 4:

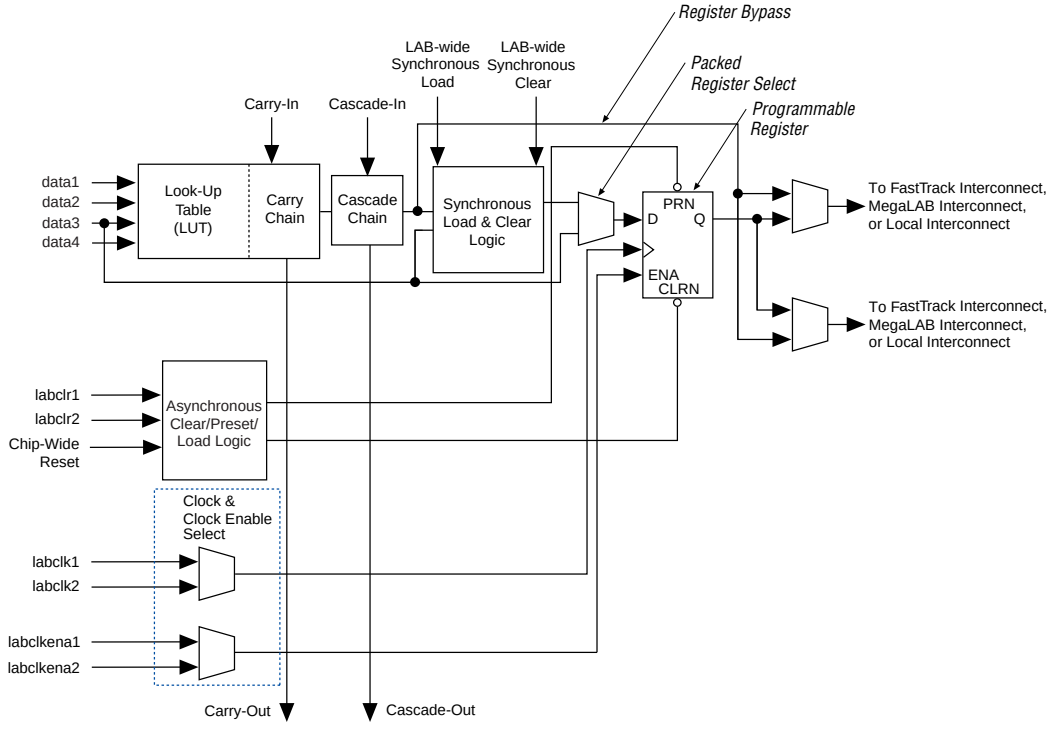
(1) The LABCLR1 and LABCLR2 signals also control asynchronous load and asynchronous preset for LEs within the LAB.

(2) The SYNCCLR signal can be generated by the local interconnect or global signals.

Logic Element

The LE is the smallest unit of logic in the APEX II architecture. Each LE contains a four-input LUT, which is a function generator that can quickly implement any function of four variables. In addition, each LE contains a programmable register and carry and cascade chains. Each LE drives the local interconnect, MegaLAB interconnect, and FastTrack interconnect routing structures. See Figure 5.

Figure 5. APEX II Logic Element



Each LE's programmable register can be configured for D, T, JK, or SR operation. The register's clock and clear control signals can be driven by global signals, general-purpose I/O pins, or any internal logic. For combinatorial functions, the register is bypassed and the output of the LUT drives the outputs of the LE.

Each LE has two outputs that drive the local, MegaLAB, or FastTrack interconnect routing structure. Each output can be driven independently by the LUT's or register's output. For example, the LUT can drive one output while the register drives the other output. This feature, called register packing, improves device utilization because the register and the LUT can be used for unrelated functions. The LE can also drive out registered and unregistered versions of the LUT output. The APEX II architecture provides two types of dedicated high-speed data paths that connect adjacent LEs without using local interconnect paths: carry chains and cascade chains. A carry chain supports high-speed arithmetic functions such as counters and adders, while a cascade chain implements wide-input functions such as equality comparators with minimum delay. Carry and cascade chains connect LEs 1 through 10 in an LAB and all LABs in the same MegaLAB structure.

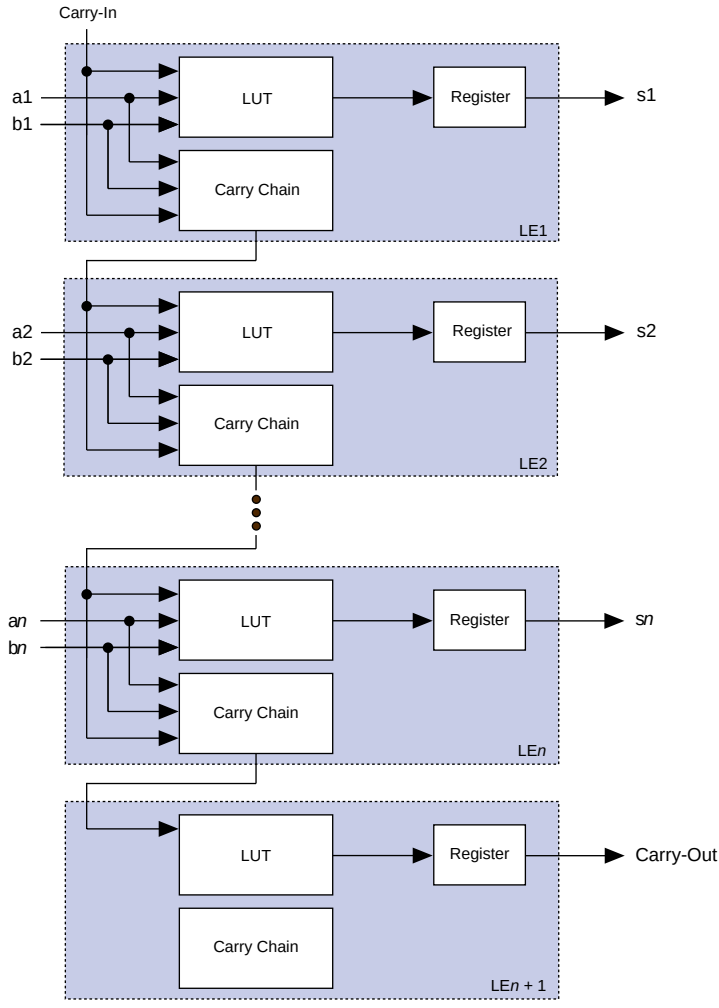
Carry Chain

The carry chain provides a fast carry-forward function between LEs. The carry-in signal from a lower-order bit drives forward into the higher-order bit via the carry chain, and feeds into both the LUT and the next portion of the carry chain. This feature allows the APEX II architecture to implement high-speed counters, adders, and comparators of arbitrary width. The Quartus II Compiler can create carry chain logic automatically during the design process, or the designer can create it manually during design entry. Parameterized functions such as DesignWare functions from Synopsys and library of parameterized modules (LPM) functions automatically take advantage of carry chains for the appropriate functions.

The Quartus II Compiler creates carry chains longer than 10 LEs by linking LABs together automatically. For enhanced fitting, a long carry chain skips alternate LABs in a MegaLAB structure. A carry chain longer than one LAB skips either from an even-numbered LAB to the next even-numbered LAB, or from an odd-numbered LAB to the next odd-numbered LAB. For example, the last LE of the first LAB in the upper-left MegaLAB structure carries to the first LE of the third LAB in the MegaLAB structure.

Figure 6 shows how an *n*-bit full adder can be implemented in *n* + 1 LEs with the carry chain. One portion of the LUT generates the sum of two bits using the input signals and the carry-in signal; the sum is routed to the output of the LE. The register can be bypassed for simple adders or used for accumulator functions. Another portion of the LUT and the carry chain logic generates the carry-out signal, which is routed directly to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it is driven onto the local, MegaLAB, or FastTrack interconnect routing structures.

Figure 6. APEX II Carry Chain

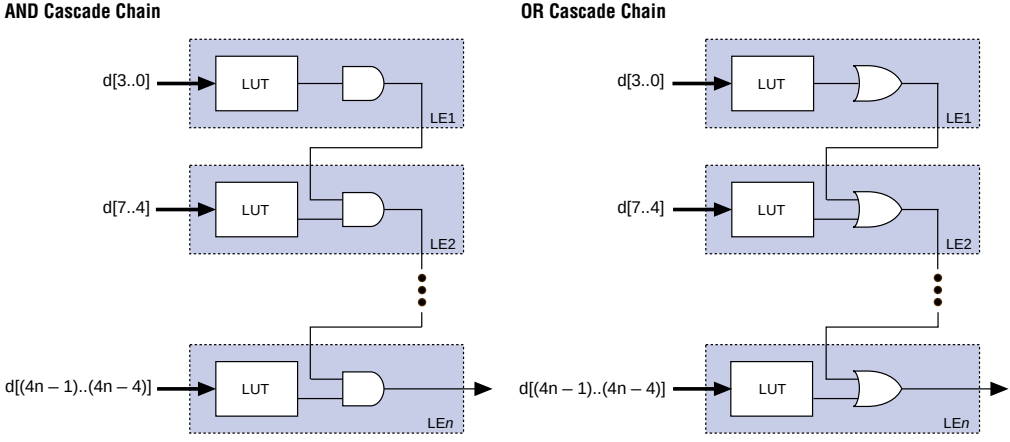


Cascade Chain

With the cascade chain, the APEX II architecture can implement functions with a very wide fan-in. Adjacent LUTs can compute portions of a function in parallel; the cascade chain serially connects the intermediate values. The cascade chain can use a logical AND or logical OR (via DeMorgan's inversion) to connect the outputs of adjacent LEs. Each additional LE provides four more inputs to the effective width of a function, with a short cascade delay. The Quartus II Compiler can create cascade chain logic automatically during the design process, or the designer can create it manually during design entry.

Cascade chains longer than 10 LEs are implemented automatically by linking LABs together. For enhanced fitting, a long cascade chain skips alternate LABs in a MegaLAB structure. A cascade chain longer than one LAB skips either from an even-numbered LAB to the next even-numbered LAB, or from an odd-numbered LAB to the next odd-numbered LAB. For example, the last LE of the first LAB in the upper-left MegaLAB structure carries to the first LE of the third LAB in the MegaLAB structure. Figure 7 shows how the cascade function can connect adjacent LEs to form functions with a wide fan-in.

Figure 7. APEX II Cascade Chain



LE Operating Modes

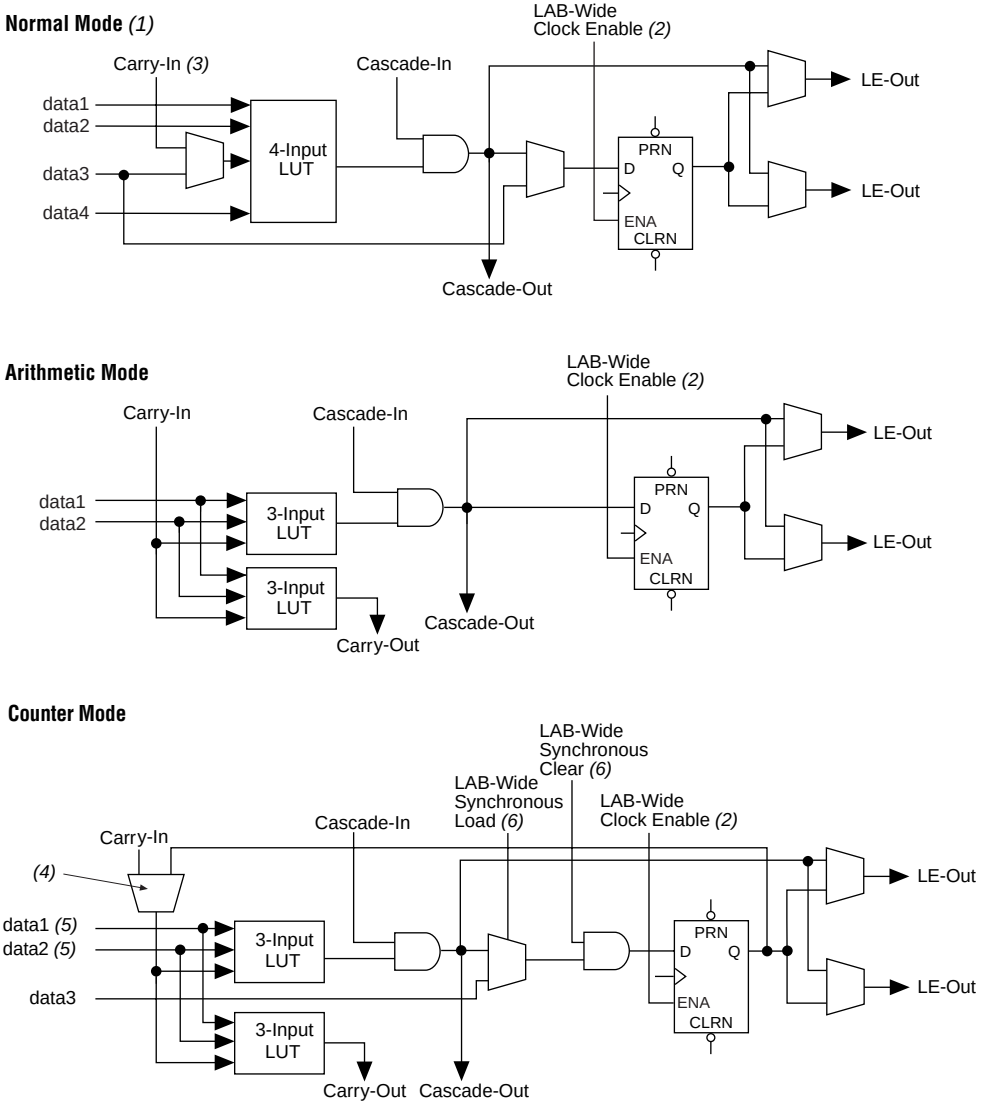
The APEX II LE can operate in one of the following three modes:

- Normal mode
- Arithmetic mode
- Counter mode

Each mode uses LE resources differently. In each mode, seven available inputs to the LE—the four data inputs from the LAB local interconnect, the feedback from the programmable register, and the carry-in and cascade-in from the previous LE—are directed to different destinations to implement the desired logic function. LAB-wide signals provide clock, asynchronous clear, asynchronous preset, asynchronous load, synchronous clear, synchronous load, and clock enable control for the register. These LAB-wide signals are available in all LE modes.

The Quartus II software, in conjunction with parameterized functions such as LPM and DesignWare functions, automatically chooses the appropriate mode for common functions such as counters, adders, and multipliers. If required, the designer can also create special-purpose functions that specify which LE operating mode to use for optimal performance. Figure 8 shows the LE operating modes.

Figure 8. APEX II LE Operating Modes



Notes to Figure 8:

(1) LEs in normal mode support register packing.
(2) There are two LAB-wide clock enables per LAB.
(3) When using the carry-in in normal mode, the packed register feature is unavailable.
(4) A register feedback multiplexer is available on LE1 of each LAB.
(5) The DATA1 and DATA2 input signals can supply counter enable, up or down control, or register feedback signals for LEs other than the second LE in a LAB.
(6) The LAB-wide synchronous clear and LAB-wide synchronous load affect all registers in a LAB.

Normal Mode

The normal mode is suitable for general logic applications, combinatorial functions, or wide decoding functions that can take advantage of a cascade chain. In normal mode, four data inputs from the LAB local interconnect and the carry-in are inputs to a four-input LUT. The Quartus II Compiler automatically selects the carry-in or the DATA3 signal as one of the inputs to the LUT. The LUT output can be combined with the cascade-in signal to form a cascade chain through the cascade-out signal. LEs in normal mode support packed registers.

Arithmetic Mode

The arithmetic mode is ideal for implementing adders, accumulators, and comparators. An LE in arithmetic mode uses two 3-input LUTs. One LUT computes a three-input function; the other generates a carry output. As shown in Figure 8, the first LUT uses the carry-in signal and two data inputs from the LAB local interconnect to generate a combinatorial or registered output. For example, when implementing an adder, this output is the sum of three signals: DATA1, DATA2, and carry-in. The second LUT uses the same three signals to generate a carry-out signal, thereby creating a carry chain. The arithmetic mode also supports simultaneous use of the cascade chain. LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output.

The Quartus II software implements parameterized functions that use the arithmetic mode automatically where appropriate; the designer does not need to specify how the carry chain will be used.

Counter Mode

The counter mode offers clock enable, counter enable, synchronous up / down control, synchronous clear, and synchronous load options. The counter enable and synchronous up / down control signals are generated from the data inputs of the LAB local interconnect. The synchronous clear and synchronous load options are LAB-wide signals that affect all registers in the LAB. Consequently, if any of the LEs in an LAB use the counter mode, other LEs in that LAB must be used as part of the same counter or be used for a combinatorial function. The Quartus II software automatically places any registers that are not used by the counter into other LABs.

The counter mode uses two three-input LUTs: one generates the counter data, and the other generates the fast carry bit. A 2-to-1 multiplexer provides synchronous loading, and another AND gate provides synchronous clearing. If the cascade function is used by an LE in counter mode, the synchronous clear or load overrides any signal carried on the cascade chain. The synchronous clear overrides the synchronous load. LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output.

Clear & Preset Logic Control

Logic for the register's clear and preset signals is controlled by LAB-wide signals. The LE directly supports an asynchronous clear function. The Quartus II Compiler can use a NOT-gate push-back technique to emulate an asynchronous preset. Moreover, the Quartus II Compiler can use a programmable NOT-gate push-back technique to emulate simultaneous preset and clear or asynchronous load. However, this technique uses three additional LEs per register. All emulation is performed automatically when the design is compiled. Registers that emulate simultaneous preset and load will enter an unknown state upon power-up or when the chip-wide reset is asserted.

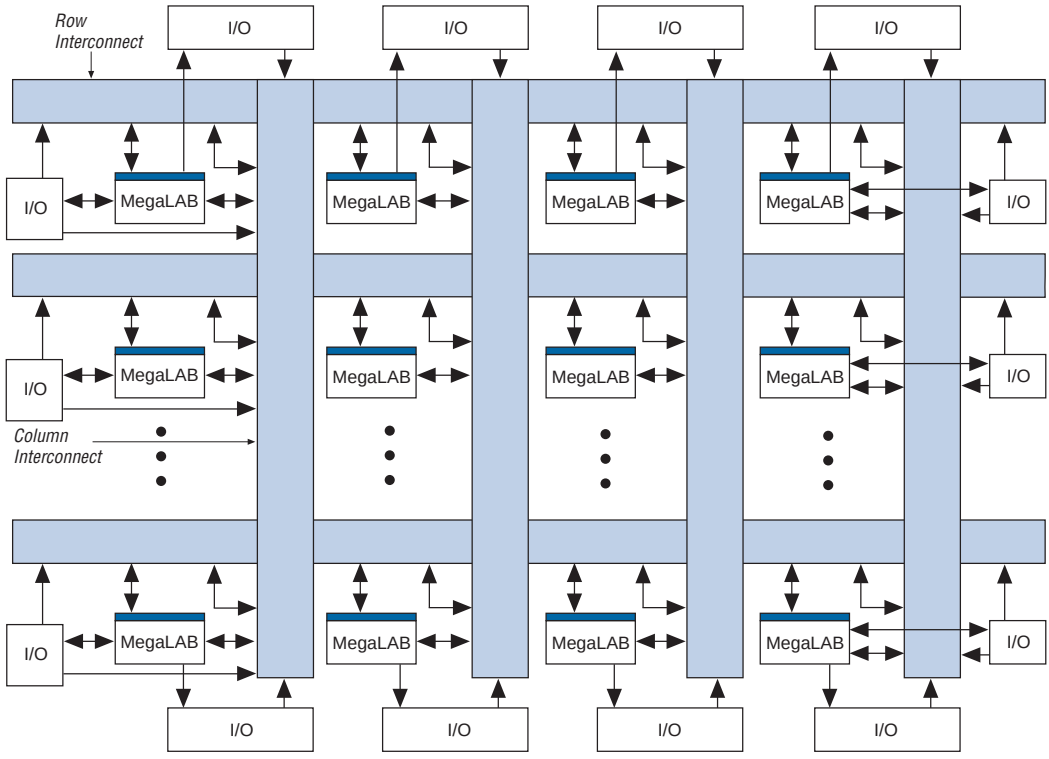
In addition to the two clear and preset modes, APEX II devices provide a chip-wide reset pin (DEV_CLRn) that resets all registers in the device. Use of this pin is controlled through an option in the Quartus II software that is set before compilation. The chip-wide reset overrides all other control signals. Registers using an asynchronous preset are preset when the chip-wide reset is asserted; this effect results from the inversion technique used to implement the asynchronous preset.

FastTrack Interconnect

In the APEX II architecture, connections between LEs, ESBs, and I/O pins are provided by the FastTrack interconnect. The FastTrack interconnect is a series of continuous horizontal and vertical routing channels that traverse the device. This global routing structure provides predictable performance, even in complex designs. In contrast, the segmented routing in FPGAs requires switch matrices to connect a variable number of routing paths, increasing the delays between logic resources and reducing performance.

The FastTrack interconnect consists of row and column interconnect channels that span the entire device. The row interconnect routes signals throughout a row of MegaLAB structures; the column interconnect routes signals throughout a column of MegaLAB structures. When using the row and column interconnect, an LE, IOE, or ESB can drive any other LE, IOE, or ESB in a device. See Figure 9.

Figure 9. APEX II Interconnect Structure



A row line can be driven directly by LEs, IOEs, or ESBs in that row. Further, a column line can drive a row line, allowing an LE, IOE, or ESB to drive elements in a different row via the column and row interconnect. The row interconnect drives the MegaLAB interconnect to drive LEs, IOEs, or ESBs in a particular MegaLAB structure.

A column line can be directly driven by the LEs, IOEs, or ESBs in that column. Row IOEs can drive a column line on a device's left or right edge. The column line is used to route signals from one row to another. A column line can drive a row line; it can also drive the MegaLAB interconnect directly, allowing faster connections between rows.

Figure 10 shows how the FastTrack interconnect uses the local interconnect to drive LEs within MegaLAB structures.

Figure 10. FastTrack Connection to Local Interconnect

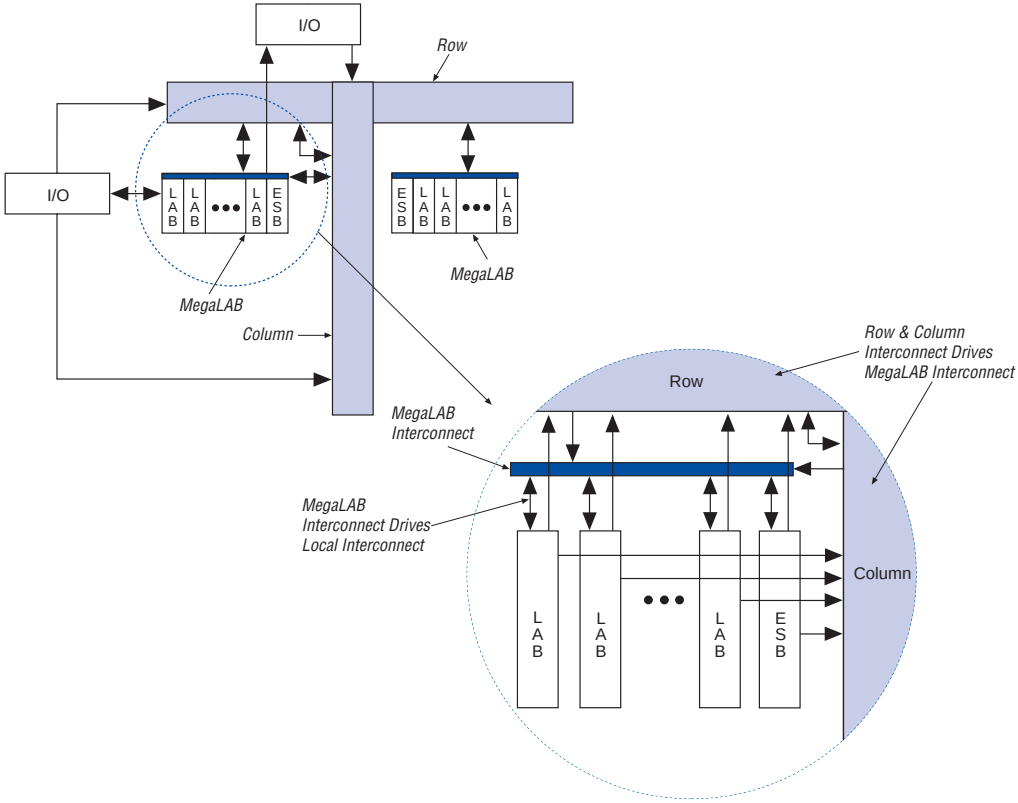
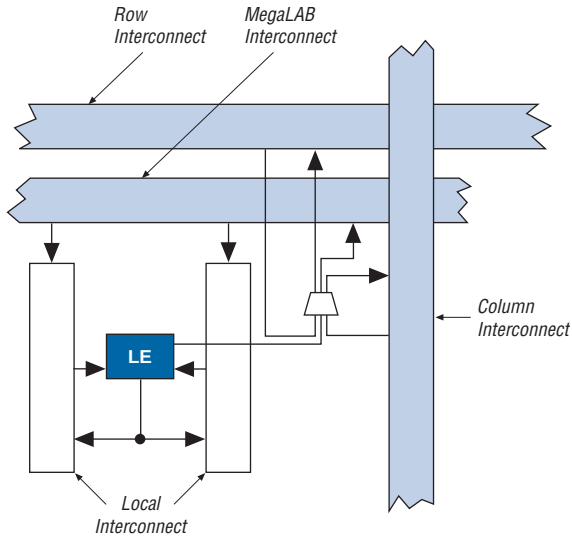


Figure 11 shows the intersection of a row and column interconnect and how these forms of interconnects and LEs drive each other.

Figure 11. Driving the FastTrack Interconnect



APEX II devices feature FastRow™ lines for quickly routing input signals with high fan-out. Column I/O pins can drive the FastRow interconnect, which routes signals directly into the local interconnect without having to drive through the MegaLAB interconnect. FastRow lines traverse two MegaLAB structures. The FastRow interconnect drives the four MegaLABs in the top row and the four MegaLABs in the bottom row of the device. The FastRow interconnect drives all local interconnects in the appropriate MegaLABs. Column pins using the FastRow interconnect achieve a faster set-up time, because the signal does not need to use a MegaLab interconnect line to reach the destination LE. Figure 12 shows the FastRow interconnect.

Figure 12. APEX II FastRow Interconnect

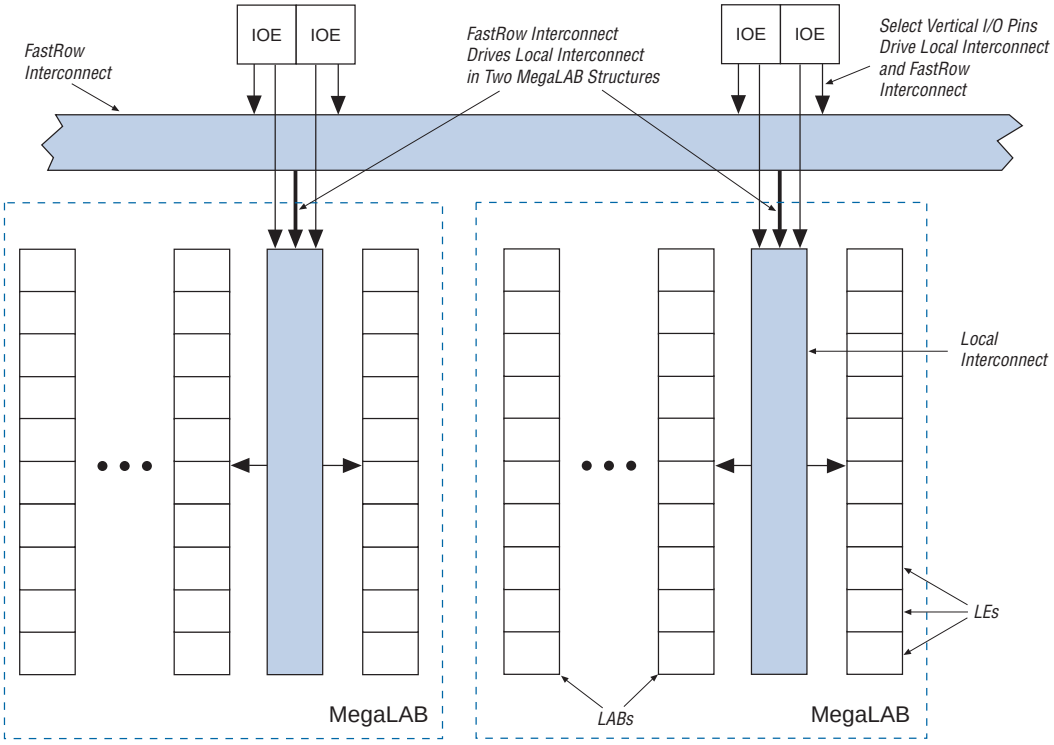


Table 5 summarizes how elements of the APEX II architecture drive each other.

Table 5. APEX II Routing Scheme

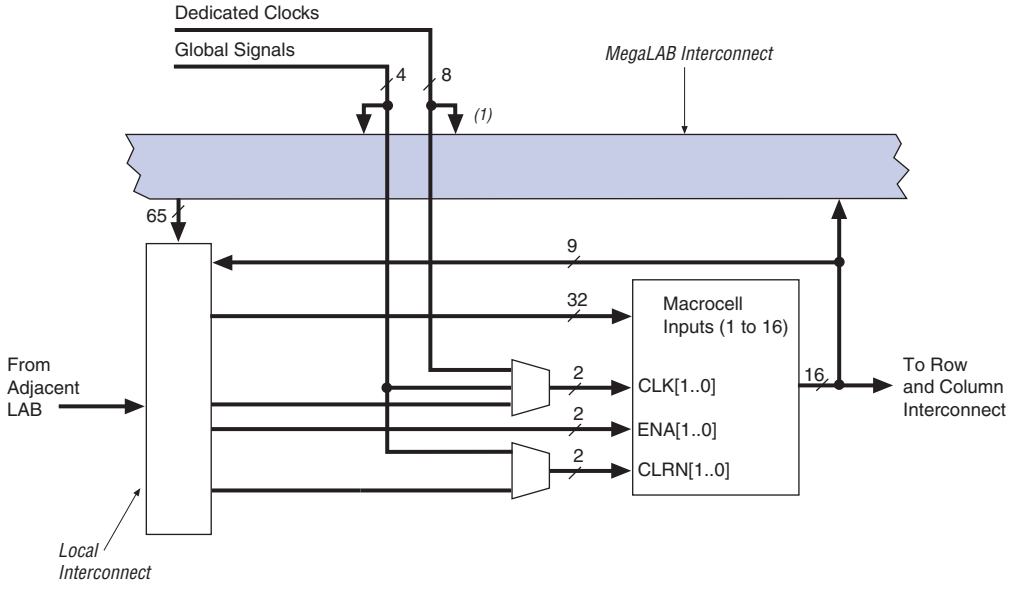
Source	Destination								
	Row I/O Pin	Column I/O Pin	LE	ESB	Local Interconnect	MegaLAB Interconnect	Row FastTrack Interconnect	Column FastTrack Interconnect	FastRow Interconnect
Row I/O pin					✓	✓	✓	✓	
Column I/O pin								✓	✓
LE					✓	✓	✓	✓	
ESB					✓	✓	✓	✓	
Local interconnect	✓	✓	✓	✓					
MegaLAB interconnect					✓				
Row FastTrack interconnect						✓		✓	
Column FastTrack interconnect						✓	✓		
FastRow interconnect					✓				

Product-Term Logic

The product-term portion of the MultiCore architecture is implemented with the ESB. The ESB can be configured to act as a block of macrocells on an ESB-by-ESB basis. 32 inputs from the adjacent local interconnect feed each ESB; therefore, the either MegaLAB or the adjacent LAB can drive the ESB. Also, nine ESB macrocells feed back into the ESB through the local interconnect for higher performance. Dedicated clock pins, global signals, and additional inputs from the local interconnect drive the ESB control signals.

In product-term mode, each ESB contains 16 macrocells. Each macrocell consists of two product terms and a programmable register. Figure 13 shows the ESB in product-term mode.

Figure 13. Product-Term Logic in ESB



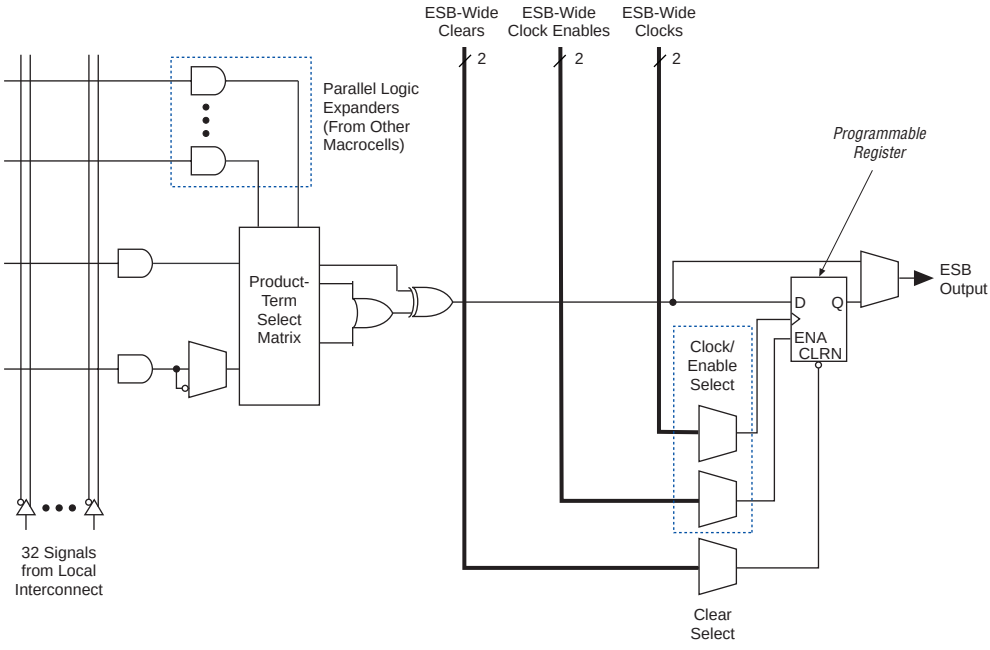
Note ot Figure 13:
(1) PLL outputs cannot drive data input ports.

Macrocells

APEX II macrocells can be configured individually for either sequential or combinatorial logic operation. The macrocell consists of three functional blocks: the logic array, the product-term select matrix, and the programmable register.

Combinatorial logic is implemented in the product terms. The product-term select matrix allocates these product terms for use as either primary logic inputs (to the OR and XOR gates) to implement combinatorial functions, or as parallel expanders to be used to increase the logic available to another macrocell. One product term can be inverted; the Quartus II software uses this feature to perform DeMorgan's inversion for more efficient implementation of wide OR functions. The Quartus II Compiler can use a NOT-gate push-back technique to emulate an asynchronous preset. Figure 14 shows the APEX II macrocell.

Figure 14. APEX II Macrocell



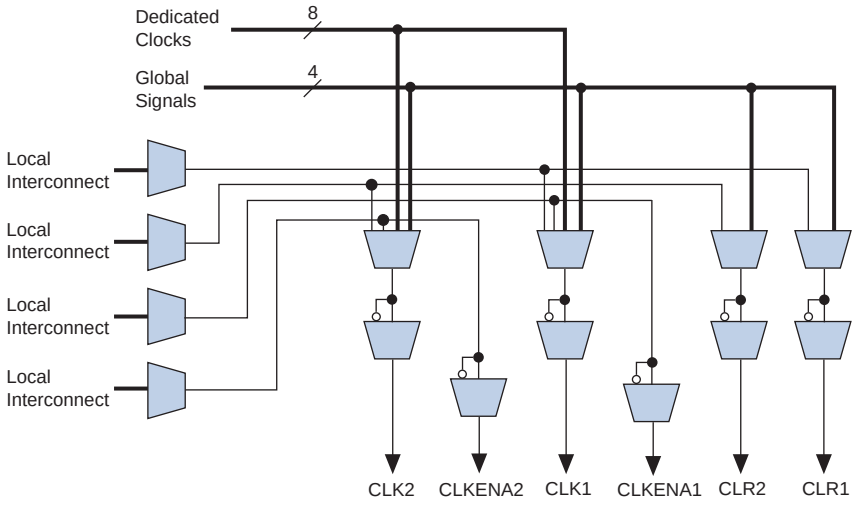
For registered functions, each macrocell register can be programmed individually to implement D, T, JK, or SR operation with programmable clock control. The register can be bypassed for combinatorial operation. During design entry, the designer specifies the desired register type; the Quartus II software then selects the most efficient register operation for each registered function to optimize resource utilization. The Quartus II software or other synthesis tools can also select the most efficient register operation automatically when synthesizing HDL designs.

Each programmable register can be clocked by one of two ESB-wide clocks. The ESB-wide clocks can be generated from device dedicated clock pins, global signals, or local interconnect. Each clock also has an associated clock enable, generated from the local interconnect. The clock and clock enable signals are related for a particular ESB; any macrocell using a clock also uses the associated clock enable.

If both the rising and falling edges of a clock are used in an ESB, both ESB-wide clock signals are used.

The programmable register also supports an asynchronous clear function. Within the ESB, two asynchronous clears are generated from global signals and the local interconnect. Each macrocell can either choose between the two asynchronous clear signals or choose to not be cleared. Either of the two clear signals can be inverted within the ESB. Figure 15 shows the ESB control logic when implementing product-terms.

Figure 15. ESB Product-Term Mode Control Logic

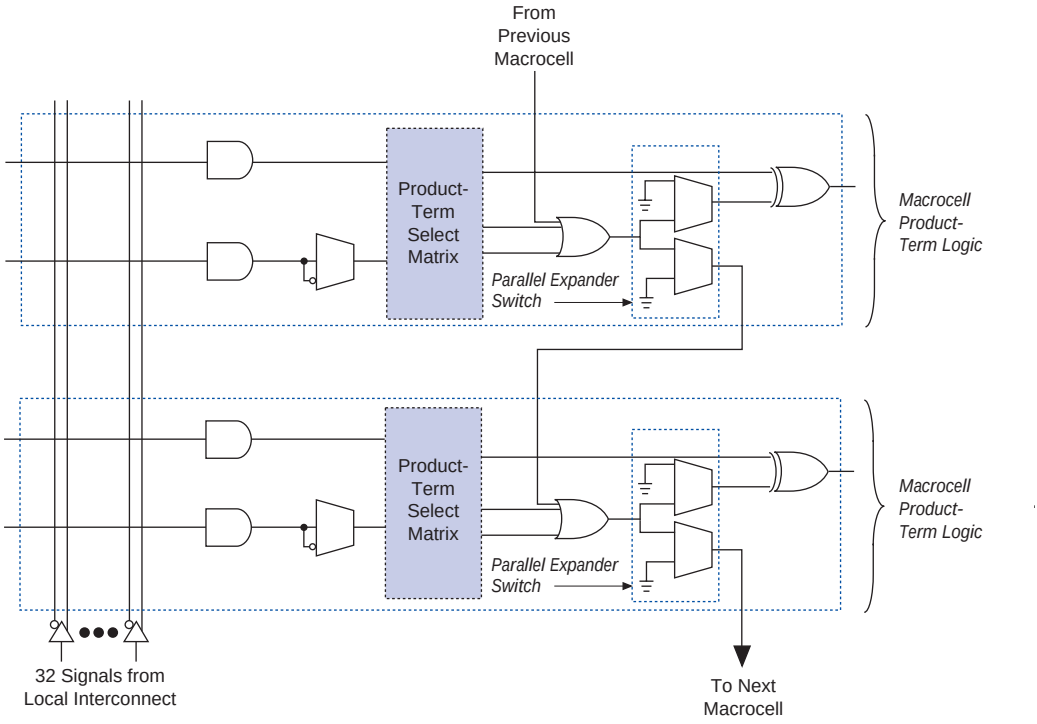


Parallel Expanders

Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 32 product terms to feed the macrocell OR logic directly, with two product terms provided by the macrocell and 30 parallel expanders provided by the neighboring macrocells in the ESB.

The Quartus II Compiler can allocate up to 15 sets of up to two parallel expanders per set to the macrocells automatically. Each set of two parallel expanders incurs a small, incremental timing delay. Figure 16 shows the APEX II parallel expanders.

Figure 16. APEX II Parallel Expanders

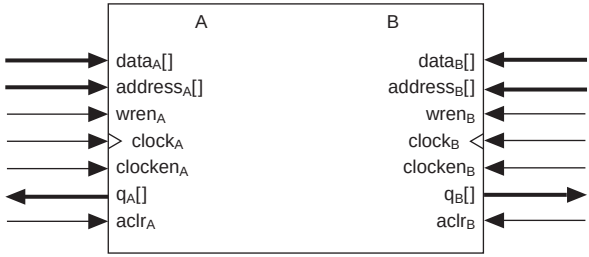


Embedded System Block

The ESB can implement various types of memory blocks, including Dual-Port+ RAM (bidirectional dual-port RAM), dual- and single-port RAM, ROM, FIFO, and CAM blocks.

The ESB includes input and output registers; the input registers synchronize writes, and the output registers can pipeline designs to improve system performance. The ESB offers a bidirectional, dual-port mode, which supports any combination of two port operations: two reads, two writes, or one read and one write at two different clock frequencies. Figure 17 shows the ESB block diagram.

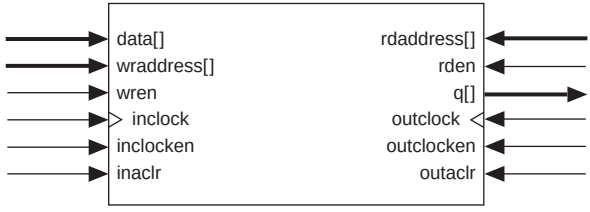
Figure 17. Bidirectional Dual-Port Memory Configuration



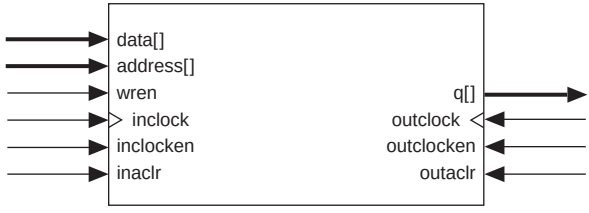
In addition to bidirectional dual-port memory, the ESB also supports dual-port, and single-port RAM. Dual-port memory supports a simultaneous read and write. Single-port memory supports independent read and write. Figure 18 shows these different RAM memory port configurations for an ESB.

Figure 18. Dual- & Single-Port Memory Configurations

Dual-Port Memory



Single-Port Memory *(1)*



Note to Figure 18:

(1) Two single-port memory blocks can be implemented in a single ESB.

The ESB also enables variable width data ports for reading and writing to the RAM ports in dual-port RAM configuration. For example, the ESB can be written in 1× mode at port A while being read in 16× mode from port B. Table 6 lists the supported variable width configurations for an ESB in dual-port mode.

Table 6. Variable Width Configurations for Dual-Port RAM

Read Port Width	Write Port Width
1 bit	2 bits, 4 bits, 8 bits, or 16 bits
2 bits, 4 bits, 8 bits, or 16 bits	1 bit

ESBs can implement synchronous RAM, which is easier to use than asynchronous RAM. A circuit using asynchronous RAM must generate the RAM write enable (WE) signal while ensuring that its data and address signals meet setup and hold time specifications relative to the WE signal. In contrast, the ESB's synchronous RAM generates its own WE signal and is self-timed with respect to the global clock. Circuits using the ESB's self-timed RAM only need to meet the setup and hold time specifications of the global clock.

ESB inputs are driven by the adjacent local interconnect, which in turn can be driven by the MegaLAB or FastTrack interconnects. Because the ESB can be driven by the local interconnect, an adjacent LE can drive it directly for fast memory access. ESB outputs drive the MegaLAB and FastTrack interconnects and the local interconnect for fast connection to adjacent LEs or for fast feedback product-term logic.

When implementing memory, each ESB can be configured in any of the following sizes: 512 × 8, 1,024 × 4, 2,048 × 2, or 4,096 × 1. For dual-port and single-port modes, the ESB can be configured for 256 × 16 in addition to the list above.

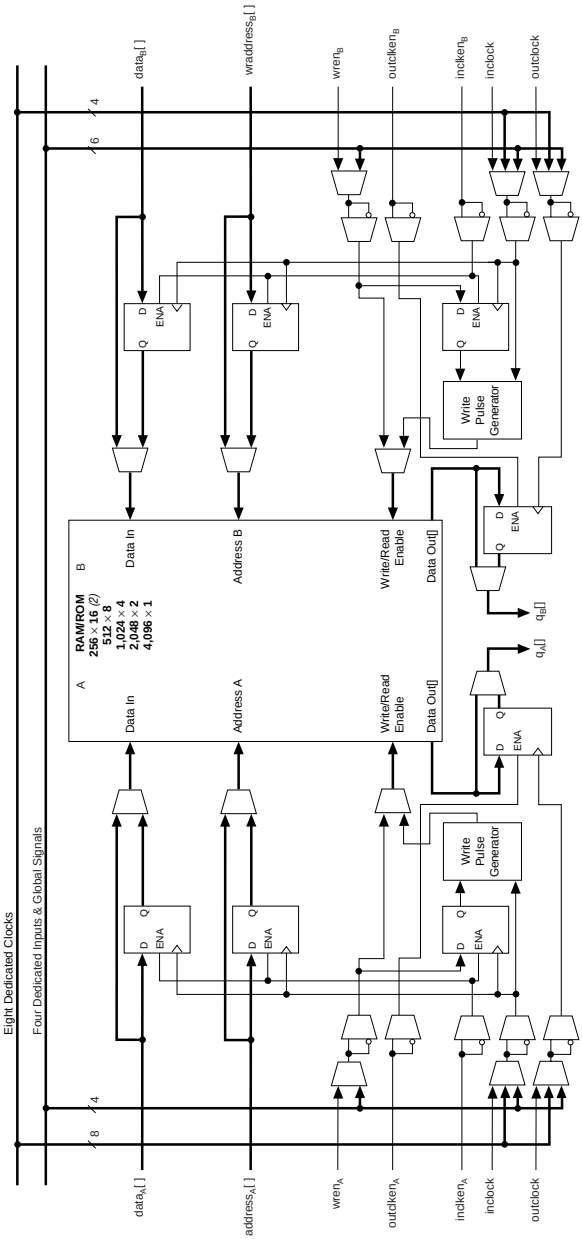
The ESB can also be split in half and used for two independent 2,048-bit single-port RAM blocks. The two independent RAM blocks must have identical configurations with a maximum width of 256 × 8. For example, one half of the ESB can be used as a 256 × 8 single-port memory while the other half is also used for a 256 × 8 single-port memory. This effectively doubles the number of RAM blocks an APEX II device can implement for its given number of ESBs. The Quartus II software automatically merges two logical memory functions in a design into an ESB; the designer does not need to merge the functions manually.

By combining multiple ESBs, the Quartus II software implements larger memory blocks automatically. For example, two 256 × 16 RAM blocks can be combined to form a 256 x 32 RAM block, and two 512 × 8 RAM blocks can be combined to form a 512 × 16 RAM block. Memory performance does not degrade for memory blocks up to 4,096 words deep. Each ESB can implement a 4,096-word-deep memory; the ESBs are used in parallel, eliminating the need for any external control logic that would increase delays. To create a high-speed memory block more than 4,096-words deep, the Quartus II software automatically combines ESBs with LE control logic.

Input/Output Clock Mode

The ESB implements input/output clock mode for both dual-port and bidirectional dual-port memory. An ESB using input/output clock mode can use up to two clocks. On each of the two ports, A or B, one clock controls all registers for inputs into the ESB: data input, WREN, read address, and write address. The other clock controls the ESB data output registers. Each ESB port, A or B, also supports independent read clock enable, write clock enable, and asynchronous clear signals. Input/output clock mode is commonly used for applications where the reads and writes occur at the same system frequency, but require different clock enable signals for the input and output registers. Figure 19 shows the ESB in input/output clock mode.

Figure 19. ESB in Input/Output Clock Mode *Note (1)*



Notes to Figure 19:

(1) All registers can be cleared asynchronously by ESB local interconnect signals, global signals, or the chip-wide reset.

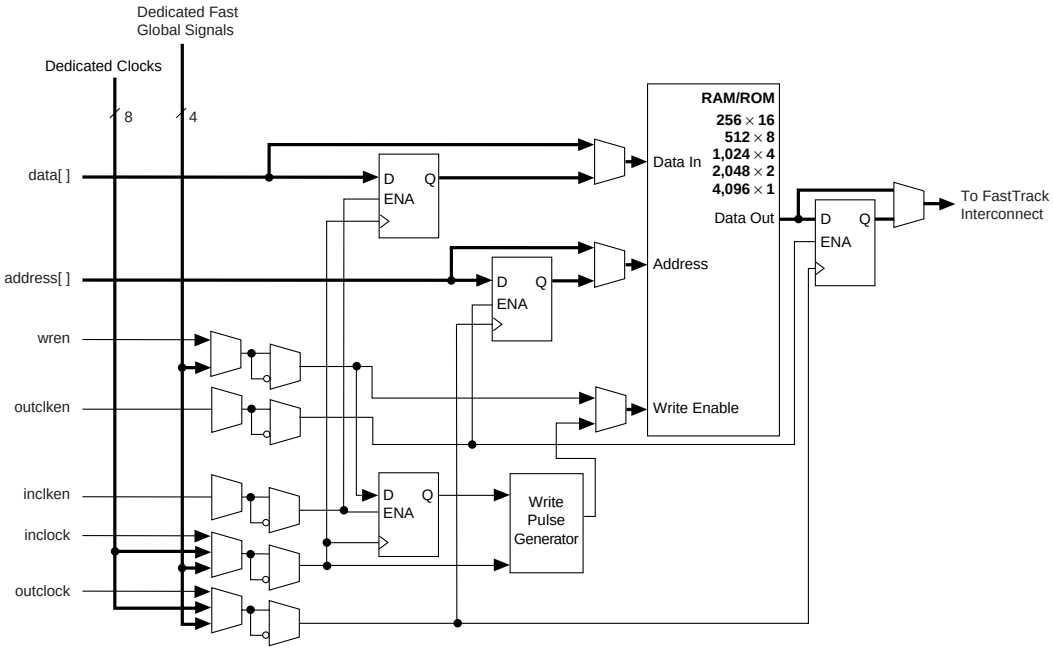
(2) This configuration is not supported for bidirectional dual-port configuration.

In addition to the input/output mode clocking scheme, the clock connections to the various ESB input/output registers are customizable in the MegaWizard® Plug-In Manager.

Single-Port Mode

The APEX II ESB also supports a single-port mode, which is used when simultaneous reads and writes are not required. See Figure 20. A single ESB can support up to two single-port mode RAMs.

Figure 20. ESB in Single-Port Mode *Note (1)*



Note to Figure 20:

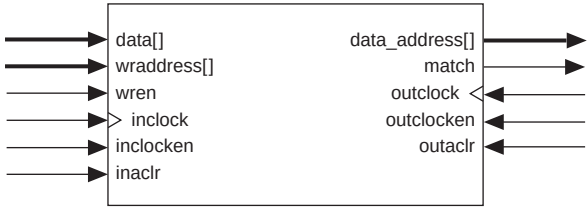
(1) All registers can be asynchronously cleared by ESB local interconnect signals, global signals, or chip-wide reset.

Content-Addressable Memory

APEX II devices can implement CAM in ESBs. CAM can be thought of as the inverse of RAM. RAM stores data in a specific location; when the system submits an address, the RAM block provides the data. Conversely, when the system submits data to CAM, the CAM block provides the address where the data is found. For example, if the data FA12 is stored in address 14, the CAM outputs 14 when FA12 is driven into it.

CAM is used for high-speed search operations. When searching for data within a RAM block, the search is performed serially. Thus, finding a particular data word can take many cycles. CAM searches all addresses in parallel and outputs the address storing a particular word. When a match is found, a match flag is set high. CAM is ideally suited for applications such as Ethernet address lookup, data compression, pattern recognition, cache tags, fast routing table lookup, and high-bandwidth address filtering. Figure 21 shows the CAM block diagram.

Figure 21. CAM Block Diagram



The APEX II on-chip CAM provides faster system performance than traditional discrete CAM. Integrating CAM and logic into the APEX II device eliminates off-chip and on-chip delays, improving system performance.

When in CAM mode, the ESB implements a 32-word, 32-bit CAM. Wider or deeper CAM, such as a 32-word, 64-bit or 128-word, 32-bit block, can be implemented by combining multiple CAM blocks with some ancillary logic implemented in LEs. The Quartus II software automatically combines ESBs and LEs to create larger CAM blocks.

CAM supports writing “don’t care” bits into words of the memory. The don’t-care bit can be used as a mask for CAM comparisons; any bit set to don’t-care has no effect on matches.

CAM can generate outputs in three different modes: single-match mode, multiple-match mode, and fast multiple-match mode. In each mode, the ESB outputs the matched data's location as an encoded or unencoded address. When encoded, the ESB outputs an encoded address of the data's location. For instance, if the data is located in address 12, the ESB output is 12. When unencoded, each ESB port uses its 16 outputs to show the location of the data over two clock cycles. In this case, if the data is located in address 12, the 12th output line goes high. Figures 21 and 22 show the encoded CAM outputs and unencoded CAM outputs, respectively.

Figure 22. Encoded CAM Address Outputs

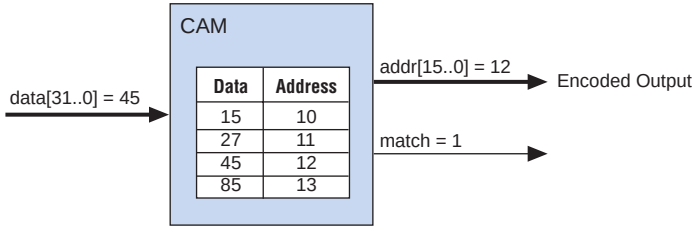
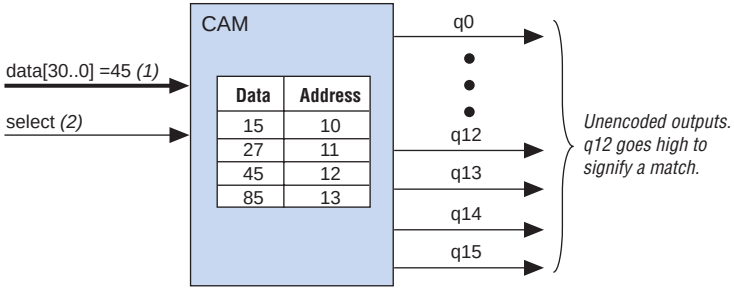


Figure 23. Unencoded CAM Address Outputs



Notes to Figures 22 and 23:

(1) For an unencoded output, the ESB only supports 31 input data bits. One input bit is used by the `select` line to choose one of the two banks of 16 outputs.

(2) If the `select` input is a 1, then CAM outputs odd words between 1 through 15. If the `select` input is a 0, CAM outputs even words between 0 through 14.

In single-match mode, it takes two clock cycles to write into CAM, but only one clock cycle to read from CAM. In this mode, both encoded and unencoded outputs are available without external logic. Single-match mode is better suited for designs without duplicate data in the memory.

If the same data is written into multiple locations in the memory, a CAM block can be used in multiple-match or fast multiple-match modes. The ESB outputs the matched data's locations as an encoded or unencoded address. In multiple-match mode, it takes two clock cycles to write into a CAM block. For reading, there are 16 outputs from each ESB at each clock cycle. Therefore, it takes two clock cycles to represent the 32 words from a single ESB port. In this mode, encoded and unencoded outputs are available. To implement the encoded version, the Quartus II software adds a priority encoder with LEs. Fast multiple-match is identical to the multiple match mode, however, it only takes one clock cycle to read from a CAM block and generate valid outputs. To do this, the entire ESB is used to represent 16 outputs. In fast multiple-match mode, the ESB can implement a maximum CAM block size of 16 words.

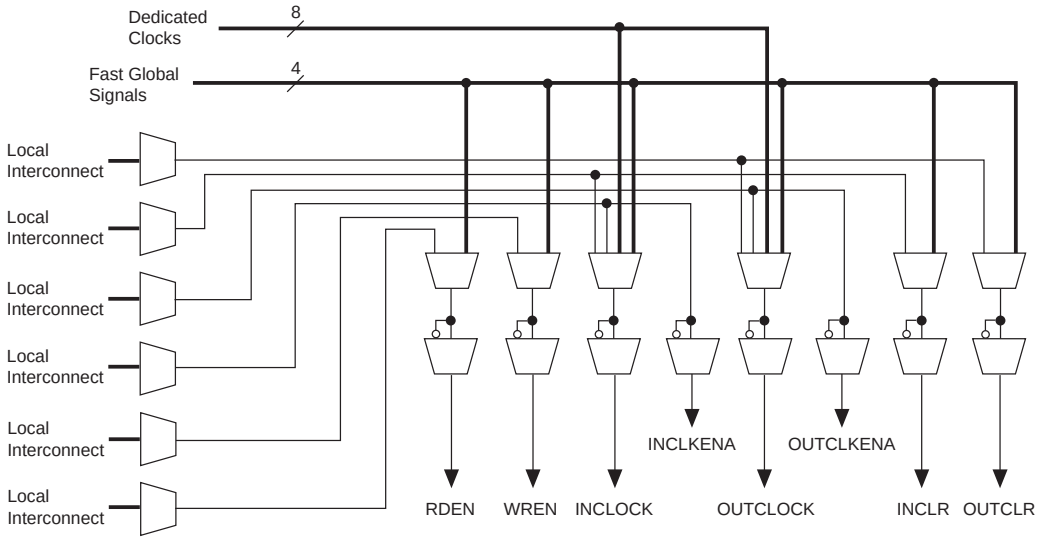
A CAM block can be pre-loaded with data during configuration, or it can be written during system operation. In most cases, two clock cycles are required to write each word into CAM. When don't-care bits are used, a third clock cycle is required.

For more information on CAM, see *Application Note 119 (Implementing High-Speed Search Applications with APEX CAM)*.

Driving Signals to the ESB

ESBs provide flexible options for driving control signals. Different clocks can be used for the ESB inputs and outputs. Registers can be inserted independently on the data input, data output, read address, write address, WE, and RE signals. The global signals and the local interconnect can drive the WE and RE signals. The global signals, dedicated clock pins, and local interconnects can drive the ESB clock signals. Because the LEs drive the local interconnect, the LEs can control the WE and RE signals and the ESB clock, clock enable, and synchronous clear signals. Figure 24 shows the ESB control signal generation logic.

Figure 24. ESB Control Signal Generation



An ESB is fed by the local interconnect, which is driven by adjacent LEs (for high-speed connection to the ESB) or the MegaLAB interconnect. The ESB can drive the local, MegaLAB, or FastTrack interconnect routing structure to drive LEs and IOEs in the same MegaLAB structure or anywhere in the device.

Implementing Logic in ROM

In addition to implementing logic with product terms, the ESB can implement logic functions when it is programmed with a read-only pattern during configuration, creating a large LUT. With LUTs, combinatorial functions are implemented by looking up the results, rather than by computing them. This implementation of combinatorial functions can be faster than using algorithms implemented in general logic, a performance advantage that is further enhanced by the fast access times of ESBs. The large capacity of ESBs enables designers to implement complex functions in one logic level without the routing delays associated with linked LEs or distributed RAM blocks. Parameterized functions such as LPM functions can take advantage of the ESB automatically. Further, the Quartus II software can implement portions of a design with ESBs where appropriate.

Programmable Speed/Power Control

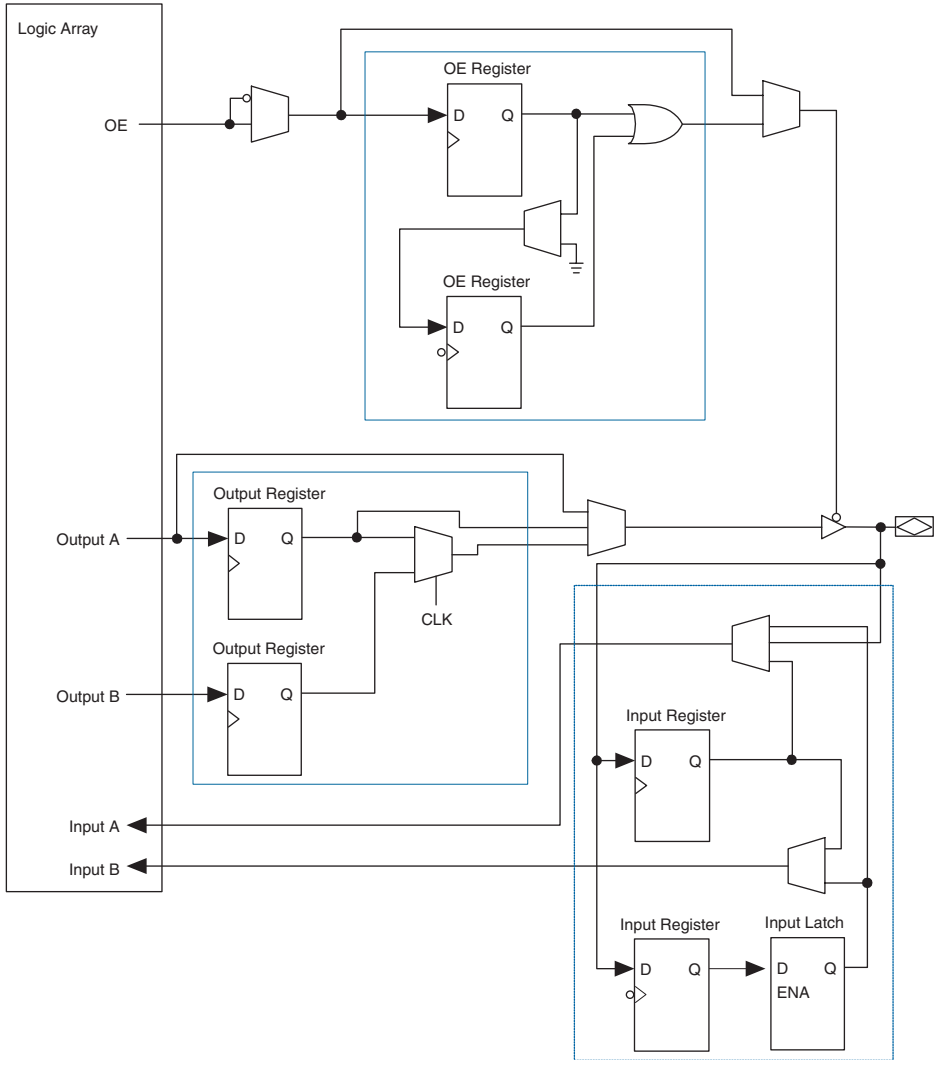
APEX II ESBs offer a high-speed mode that supports fast operation on an ESB-by-ESB basis. When high speed is not required, this feature can be turned off to reduce the ESB's power dissipation by up to 50%. ESBs that run at low power incur a nominal timing delay adder. This Turbo Bit™ option is available for ESBs that implement product-term logic or memory functions. An ESB that is not used will be powered down so that it does not consume DC current.

Designers can program each ESB in the APEX II device for either high-speed or low-power operation. As a result, speed-critical paths in the design can run at high speed, while the remaining paths operate at reduced power.

I/O Structure

The IOE in APEX II devices contains a bidirectional I/O buffer, six registers, and a latch for a complete embedded bidirectional single data rate or DDR IOE. Figure 25 shows the structure of the APEX II IOE. The IOE contains two input registers (plus a latch), two output registers, and two output enable registers. Both input registers and the latch can be used for capturing DDR input. Both output registers can be used to drive DDR outputs. The output enable (OE) register can be used for fast clock-to-output enable timing. The negative edge-clocked OE register is used for DDR SDRAM interfacing. The Quartus II software automatically duplicates a single OE register that controls multiple output or bidirectional pins.

Figure 25. APEX II IOE Structure



The IOEs are located around the periphery of the APEX II device. Each IOE drives a row, column, MegaLAB, or local interconnect when used as an input or bidirectional pin. A row IOE can drive a local, MegaLAB, row, and column interconnect; a column IOE can drive the FastTrack or column interconnect. Figure 26 shows how a row IOE connects to the interconnect.

Figure 26. Row IOE Connection to the Interconnect

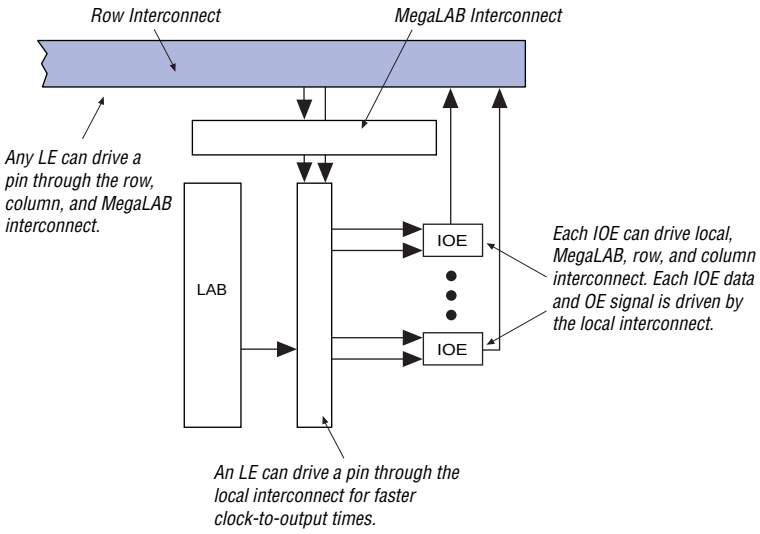
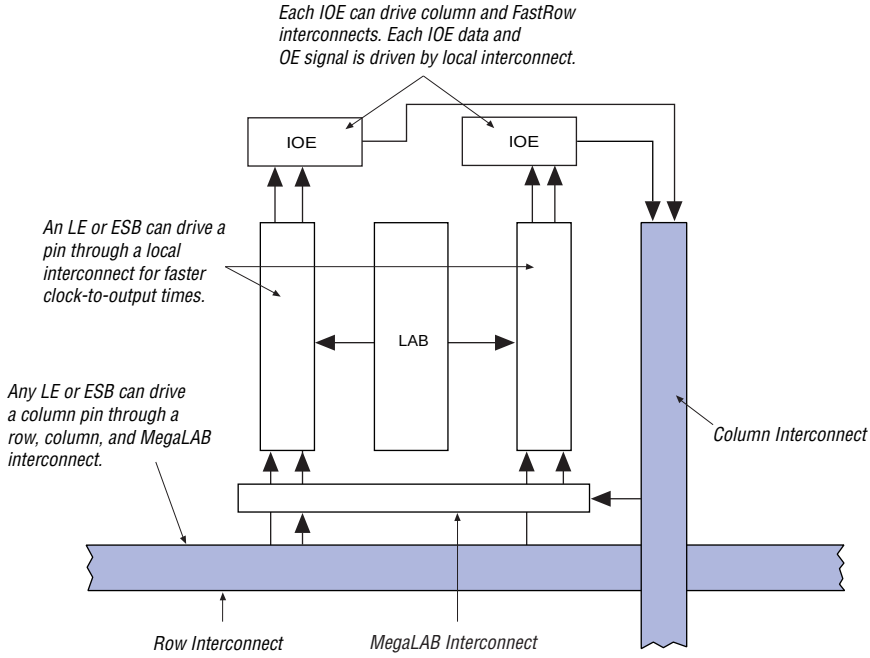


Figure 27 shows how a column IOE connects to the interconnect.

Figure 27. Column IOE Connection to the Interconnect



FastRow interconnects connect a column I/O pin directly to the LAB local interconnect within two MegaLAB structures. This feature provides fast setup times for pins that drive high fan-outs with complex logic, such as PCI designs. For fast bidirectional I/O timing, LE registers using local routing can improve setup times and OE timing.

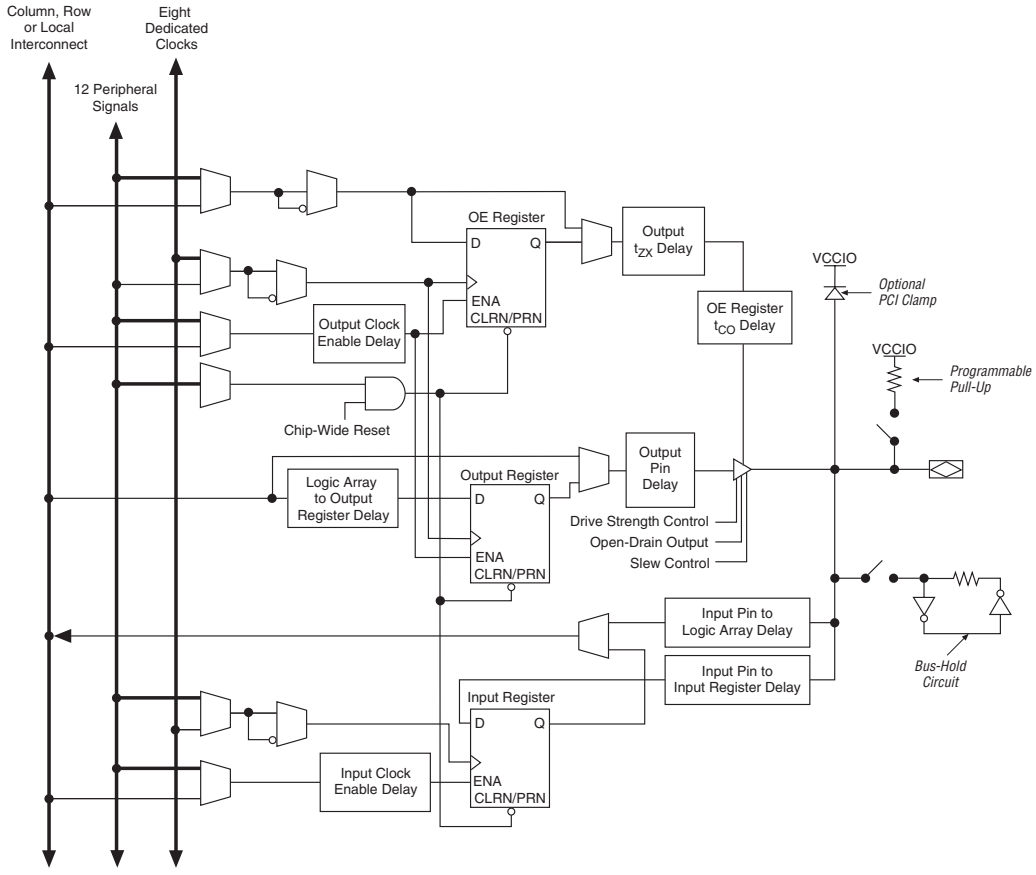
APEX II devices have a peripheral control bus made up of 12 signals that drive the IOE control signals. The peripheral bus is composed of six output enables, `OE[5:0]` and six clock enables, `CE[5:0]`. These twelve signals can be driven from internal logic or from the Fast I/O signals. Table 7 lists the peripheral control signal destinations.

Table 7. Peripheral Control Bus Destinations

Peripheral Bus	I/O Control Signal
Output Enable 0 [OE0]	OE
Output Enable 1 [OE1]	OE
Output Enable 2 [OE2]	OE
Output Enable 3 [OE3]	OE
Output Enable 4 [OE4]	OE
Output Enable 5 [OE5]	OE
Clock Enable 0 [CE0]	CE, CLK
Clock Enable 1 [CE1]	CE, OE
Clock Enable 2 [CE2]	CE, CLK
Clock Enable 3 [CE3]	CE, OE
Clock Enable 4 [CE4]	CE, CLR
Clock Enable 5 [CE5]	CE, CLR

In normal bidirectional operation, the input register can be used for input data requiring fast setup times. The input register can have its own clock input and clock enable separate from the OE and output registers. The output register can be used for data requiring fast clock-to-output performance. The OE register can be used for fast clock-to-output enable timing. The OE and output register share the same clock source and the same clock enable source from local interconnect in the associated LAB, fast global signals, or row global signals. Figure 28 shows the IOE in bidirectional configuration.

Figure 28. APEX II IOE in Bidirectional I/O Configuration



The APEX II IOE includes programmable delays that can be activated to ensure zero hold times, minimum clock-to-output times, input IOE register-to-logic array register transfers, or logic array-to-output IOE register transfers.

A path in which a pin directly drives a register may require the delay to ensure zero hold time, whereas a path in which a pin drives a register through combinatorial logic may not require the delay. Programmable delays exist for decreasing input pin to logic array and IOE input register delays. The Quartus II Compiler can program these delays automatically to minimize setup time while providing a zero hold time. Delays are also programmable for increasing the register to pin delays for output and / or output enable registers. A programmable delay exists for increasing the t_{ZX} delay to the output pin, which is required for ZBT interfaces. Table 8 shows the programmable delays for APEX II devices.

Table 8. APEX II Programmable Delay Chain

Programmable Delays	Quartus II Logic Option
Input pin to logic array delay *(1)*	Decrease input delay to internal cells
Input pin to input register delay	Decrease input delay to input register
Output propagation delay	Increase delay to output pin
Output enable register t_{CO} delay	Increase delay to output enable pin
Output t_{ZX} delay	Increase t_{ZX} delay to output pin
Output clock enable delay	Increase output clock enable delay
Input clock enable delay	Increase input clock enable delay
Logic array to output register delay	Decrease input delay to output register

Note to Table 8:
(1) This delay has four settings: off and three levels of delay.

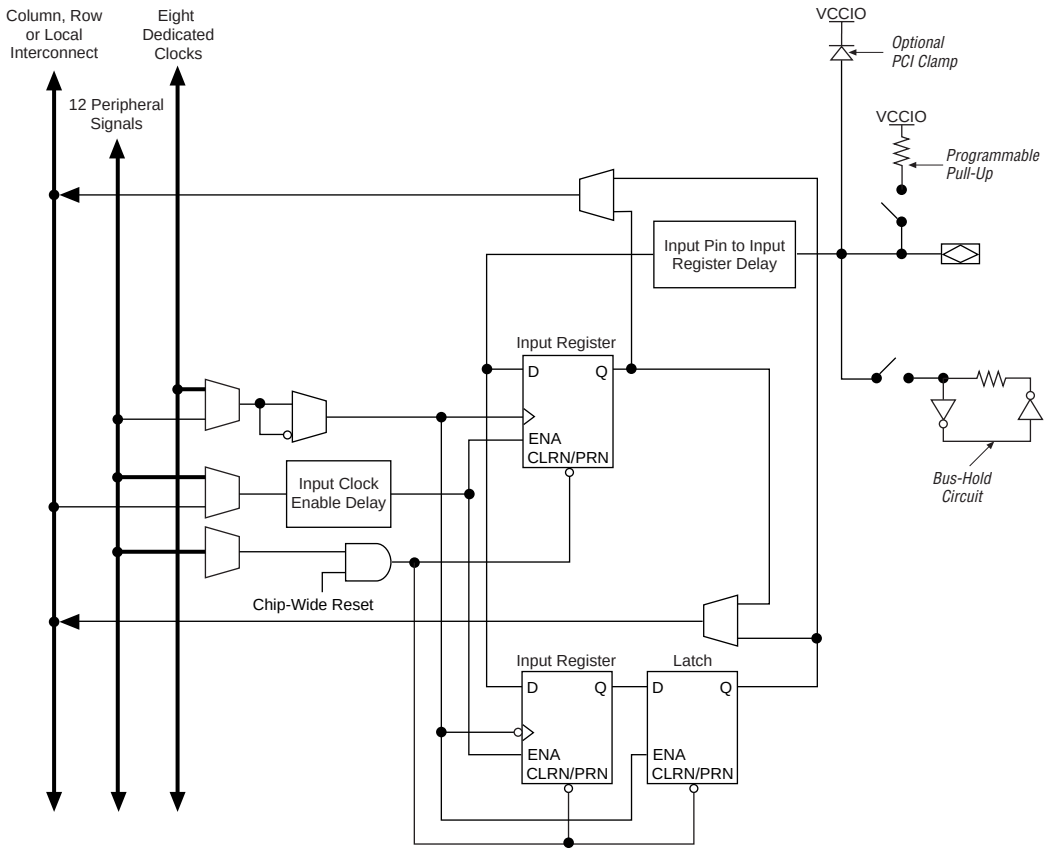
The IOE registers in APEX II devices share the same source for clear or preset. The designer can program preset and clear for each individual IOE. The registers can be programmed to power up high or low after configuration is complete. If programmed to power up low, an asynchronous clear can control the registers. If programmed to power up high, an asynchronous preset can control the registers. This feature prevents the inadvertent activation of another device's active-low input upon power-up. If one register in an IOE uses a preset or clear signal then all registers in the IOE must use that preset or clear signal.

Double Data Rate I/O

APEX II devices have six-register IOEs which support DDR interfacing by clocking data on both positive and negative clock edges. The IOEs in APEX II devices support DDR inputs, DDR outputs, and bidirectional DDR modes.

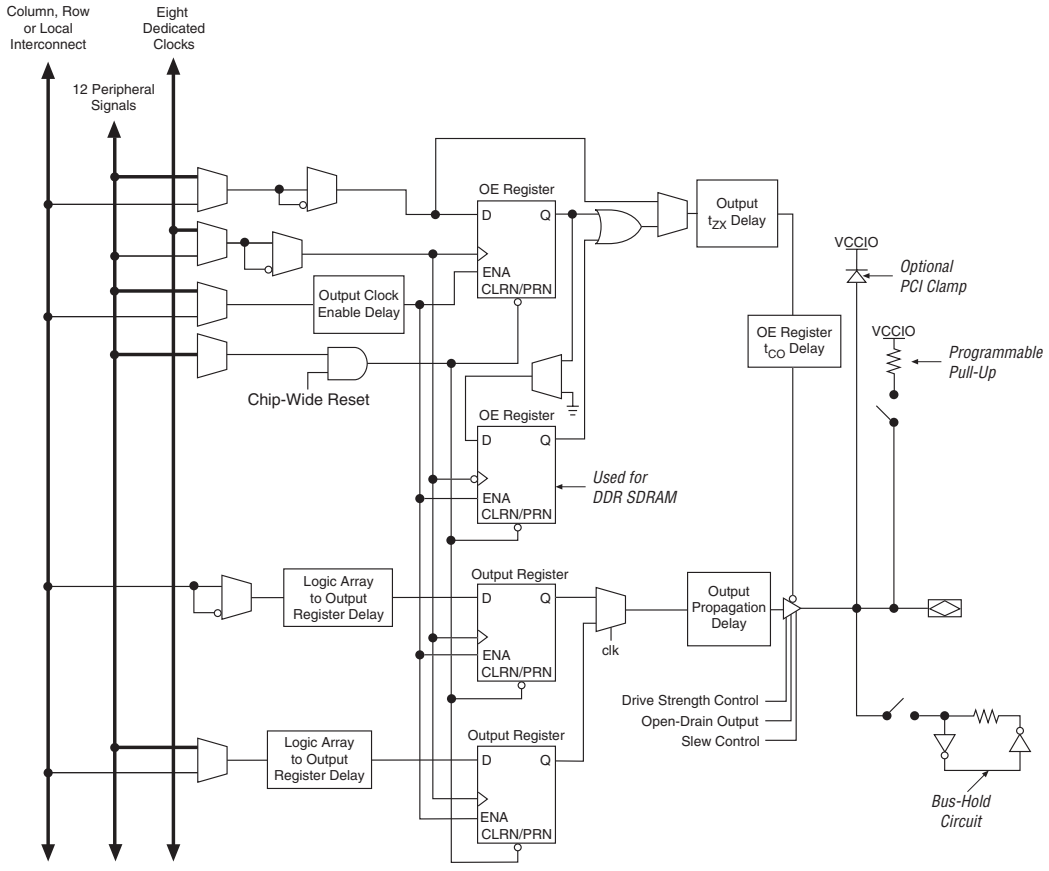
When using the IOE for DDR inputs, the two input registers are used to clock double rate input data on alternating edges. An input latch is also used within the IOE for DDR input acquisition. The latch holds the data that is present during the clock high times. This allows both bits of data to be synchronous to the same clock edge (either rising or falling). Figure 29 shows an IOE configured for DDR input.

Figure 29. APEX II IOE in DDR Input I/O Configuration



When using the IOE for DDR outputs, the two output registers are configured to clock two data paths from LEs on rising clock edges. These register outputs are multiplexed by the clock to drive the output pin at a ×2 rate. One output register clocks the first bit out on the clock high time, while the other output register clocks the second bit out on the clock low time. Figure 30 shows the IOE configured for DDR output.

Figure 30. APEX II IOE in DDR Output I/O Configuration



The APEX II IOE operates in bidirectional DDR mode by combining the DDR input and DDR output configurations.

APEX II I/O pins transfer data on a DDR bidirectional bus to support DDR SDRAM at 167 MHz (334 Mbps). The negative-edge-clocked OE register is used to hold the OE signal inactive until the falling edge of the clock. This is done to meet DDR SDRAM timing requirements. QDR SRAMs are also supported with DDR I/O pins on separate read and write ports.

Zero Bus Turnaround SRAM Interface Support

In addition to DDR SDRAM support, APEX II device I/O pins also support interfacing with ZBT SRAM devices at up to 200 MHz. ZBT SRAM blocks are designed to eliminate dead bus cycles when turning a bidirectional bus around between reads and writes, or writes and reads. ZBT allows for 100% bus utilization because ZBT SRAM can be read or written on every clock cycle.

To avoid bus contention, the output clock-to-low-impedance time (t_{ZX}) delay ensures that the t_{ZX} is greater than the clock-to-high-impedance time (t_{XZ}). Phase delay control of clocks to the OE/output and input registers using two general-purpose PLLs enable the APEX II device to meet ZBT t_{CO} and t_{SU} times.

Programmable Drive Strength

The output buffer for each APEX II device I/O pin has a programmable drive strength control for certain I/O standards. The LVTTL standard has several levels of drive strength that the user can control. SSTL-3 class I and II, SSTL-2 class I and II, HSTL class I and II, 3.3-V GTL+, PCI, and PCI-X support a minimum setting. The minimum setting is the lowest drive strength that guarantees the I_{OH}/I_{OL} of the standard. Using minimum settings provides signal slew rate control to reduce system noise and signal overshoot. Table 9 shows the possible settings for the I/O standards with drive strength control.

Table 9. Programmable Drive Strength	
I/O Standard	**I_{OH}/I_{OL} Current Strength Setting**
LVTTL (3.3 V)	4 mA
	12 mA
	24 mA (default)
LVTTL (2.5 V)	2 mA
	16 mA (default)
LVTTL (1.8 V)	2 mA
	8mA (default)
LVTTL (1.5 V)	2 mA (default)
SSTL-3 class I and II SSTL-2 class I and II HSTL class I and II GTL+ (3.3 V) PCI PCI-X	Minimum (default)

Open-Drain Output

APEX II devices provide an optional open-drain (equivalent to an open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (e.g., interrupt and write-enable signals) that can be asserted by any of several devices.

Slew-Rate Control

The output buffer for each APEX II device I/O pin has a programmable output slew rate control that can be configured for low-noise or high-speed performance. A faster slew rate provides high-speed transitions for high-performance systems. However, these fast transitions may introduce noise transients into the system. A slow slew rate reduces system noise, but adds a nominal delay to rising and falling edges. Each I/O pin has an individual slew rate control, allowing the designer to specify the slew rate on a pin-by-pin basis. The slew rate control affects both the rising and falling edges.

Bus Hold

Each APEX II device I/O pin provides an optional bus-hold feature. When this feature is enabled for an I/O pin, the bus-hold circuitry weakly holds the signal at its last driven state. By holding the last driven state of the pin until the next input signal is present, the bus-hold feature eliminates the need to add external pull-up or pull-down resistors to hold a signal level when the bus is tri-stated. The bus-hold circuitry also pulls undriven pins away from the input threshold voltage where noise can cause unintended high-frequency switching. This feature can be selected individually for each I/O pin. The bus-hold output will drive no higher than V_{CCIO} to prevent overdriving signals. If the bus-hold feature is enabled, the programmable pull-up option cannot be used. The bus-hold feature should also be disabled if open-drain outputs are used with the GTL+ I/O standard.

The bus-hold circuitry weakly pulls the signal level to the last driven state through a resistor with a nominal resistance (R_{BH}) of approximately 7 kΩ. Table 41 on page 74 gives specific sustaining current that will be driven through this resistor and overdrive current that will identify the next driven input level. This information is provided for each V_{CCIO} voltage level.

The bus-hold circuitry is active only after configuration. When going into user mode, the bus-hold circuit captures the value on the pin present at the end of configuration.

Programmable Pull-Up Resistor

Each APEX II device I/O pin provides an optional programmable pull-up resistor during user mode. When this feature is enabled for an I/O pin, the pull-up resistor (typically 25 kΩ) weakly holds the output to the V_{CCIO} level of the bank that the output pin resides in.

Dedicated Fast I/O Pins

APEX II devices incorporate dedicated bidirectional pins for signals with high internal fanout, such as PCI control signals. These pins are called dedicated fast I/O pins (FAST1, FAST2, FAST3, and FAST4) and can drive the four global fast lines throughout the device, ideal for fast clock, clock enable, preset, clear, or high fanout logic signal distribution. The dedicated fast I/O pins have one output register and one OE register, but they do not have input registers. The dedicated fast lines can also be driven by a LE local interconnect to generate internal global signals.

Advanced I/O Standard Support

APEX II device IOEs support the following I/O standards:

- LVTTL
- LVCMOS
- 1.5-V
- 1.8-V
- 2.5-V
- 3.3-V PCI
- 3.3-V PCI-X
- 3.3-V AGP (1×, 2×)
- LVDS
- LVPECL
- PCML
- HyperTransport
- GTL+
- HSTL class I and II
- SSTL-3 class I and II
- SSTL-2 class I and II
- CTT
- Differential HSTL

Table 10 describes the I/O standards supported by APEX II devices.

Table 10. APEX II Supported I/O Standards

I/O Standard	Type	Input Reference Voltage (V_{REF}) (V)	Output Supply Voltage (V_{CCIO}) (V)	Board Termination Voltage (V_{TT}) (V)
LVTTL	Single-ended	N/A	3.3	N/A
LVCMOS	Single-ended	N/A	3.3	N/A
2.5 V	Single-ended	N/A	2.5	N/A
1.8 V	Single-ended	N/A	1.8	N/A
1.5 V	Single-ended	N/A	1.5	N/A
3.3-V PCI	Single-ended	N/A	3.3	N/A
3.3-V PCI-X	Single-ended	N/A	3.3	N/A
LVDS	Differential	N/A	3.3	N/A
LVPECL	Differential	N/A	3.3	N/A
PCML	Differential	N/A	3.3	N/A
HyperTransport	Differential	N/A	2.5	N/A
Differential HSTL *(1)*	Differential	N/A	1.5	N/A
GTL+	Voltage referenced	1.0	N/A	1.5
HSTL class I and II	Voltage referenced	0.75	1.5	0.75
SSTL-2 class I and II	Voltage referenced	1.25	2.5	1.25
SSTL-3 class I and II	Voltage referenced	1.5	3.3	1.5
AGP (1× and 2×)	Voltage referenced	1.32	3.3	N/A
CTT	Voltage referenced	1.5	3.3	1.5

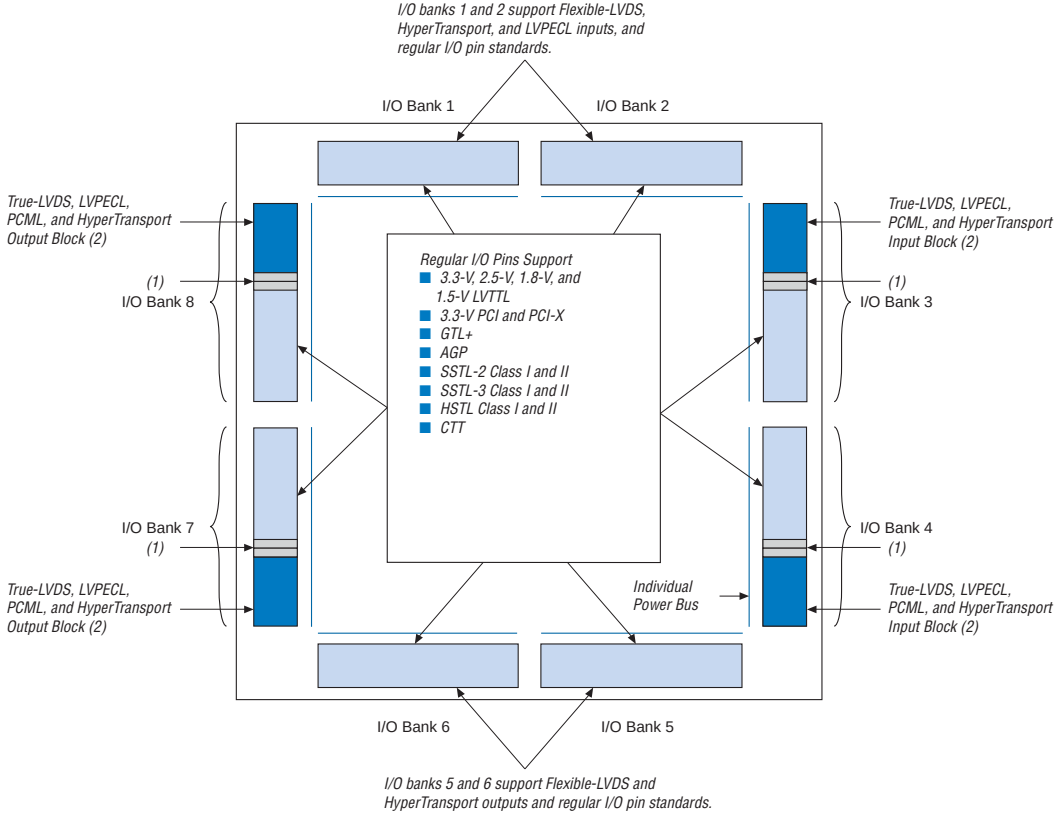
Note to Table 10:

(1) Differential HSTL is only supported on the eight dedicated global clock pins and four dedicated high-speed PLL clock pins.

For more information on I/O standards supported by APEX II devices, see *Application Note 117 (Using Selectable I/O Standards in Altera Devices)*.

APEX II devices contain eight I/O banks, as shown in Figure 31. Two blocks within the right I/O banks contain circuitry to support high-speed True-LVDS, LVPECL, PCML, and HyperTransport inputs, and another two blocks within the left I/O banks support high-speed True-LVDS, LVPECL, PCML, and HyperTransport outputs. All other standards are supported by all I/O banks.

Figure 31. APEX II I/O Banks



Notes to Figure 31:

(1) For more information on placing I/O pins within LVDS blocks, refer to the "High-Speed Interface Pin Location" section in *Application Note 166 (Using High-Speed I/O Standards in APEX II Devices)*.

(2) If the True-LVDS pins or the Flexible-LVDS pins are not used for high-speed differential signalling, they can support all of the I/O standards and can be used as input, output, or bidirectional pins with V_{CCIO} set to 3.3 V, 2.5 V, 1.8 V, or 1.5 V. However, True-LVDS pins do not support the HSTL Class II output.

Each I/O bank has its own VCCIO pins. A single device can support 1.5-V, 1.8-V, 2.5-V, and 3.3-V interfaces; each bank can support a different standard independently. Each bank can also use a separate V_{REF} level to support any one of the terminated standards (such as SSTL-3) independently.

Each bank can support multiple standards with the same V_{CCIO} for input and output pins. Each bank can support one voltage-referenced I/O standard, but it can support multiple I/O standards with the same V_{CCIO} voltage level. For example, when V_{CCIO} is 3.3 V, a bank can support LVTTL, LVCMOS, 3.3-V PCI, and SSTL-3 for inputs and outputs. When the True-LVDS banks are not used for LVDS I/O pins, they support all of the other I/O standards except HSTL Class II output.

True-LVDS Interface

APEX II devices contain dedicated circuitry for supporting differential standards at speeds up to 1.0 Gbps. APEX II devices have dedicated differential buffers and circuitry to support LVDS, LVPECL, HyperTransport, and PCML I/O standards. Four dedicated high-speed PLLs (separate from the general-purpose PLLs) multiply reference clocks and drive high-speed differential serializer/deserializer channels. In addition, CDS circuitry at each receiver channel corrects any fixed clock-to-data skew. All APEX II devices support 36 input channels, 36 output channels, two dedicated receiver PLLs, and two dedicated transmitter PLLs.

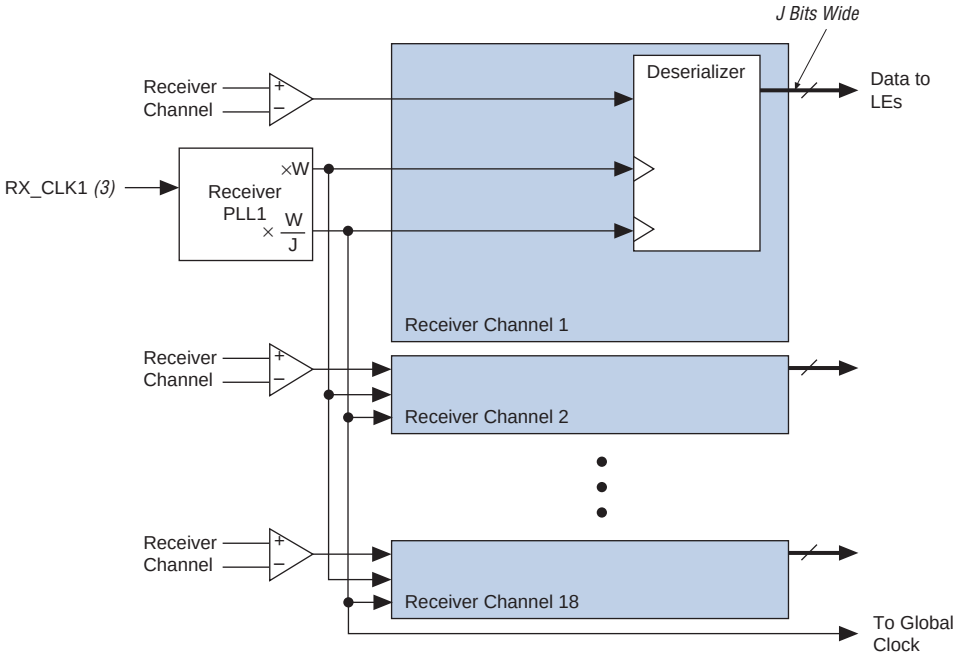
The True-LVDS circuitry supports the following standards and applications:

- RapidIO
- POS-PHY Level 4
- Utopia IV
- HyperTransport

APEX II devices support source-synchronous interfacing with LVDS, LVPECL,PCML, or HyperTransport signaling at up to 1 Gbps. Serial channels are transmitted and received along with a low-speed clock. The receiving device then multiplies the clock by a factor of 1, 2, or 4 to 10. The serialization/deserialization rate can be any number from 1, 2, or 4 to 10 and does not have to equal the clock multiplication value.

For example, an 840-Mbps LVDS channel can be received along with an 84-MHz clock. The 84-MHz clock is multiplied by 10 to drive the serial shift register, but the register can be clocked out in parallel at 8- or 10-bits wide at 84 or 105 MHz. See Figures 32 and 33.

Figure 32. True-LVDS Receiver Diagram *Notes (1), (2)*



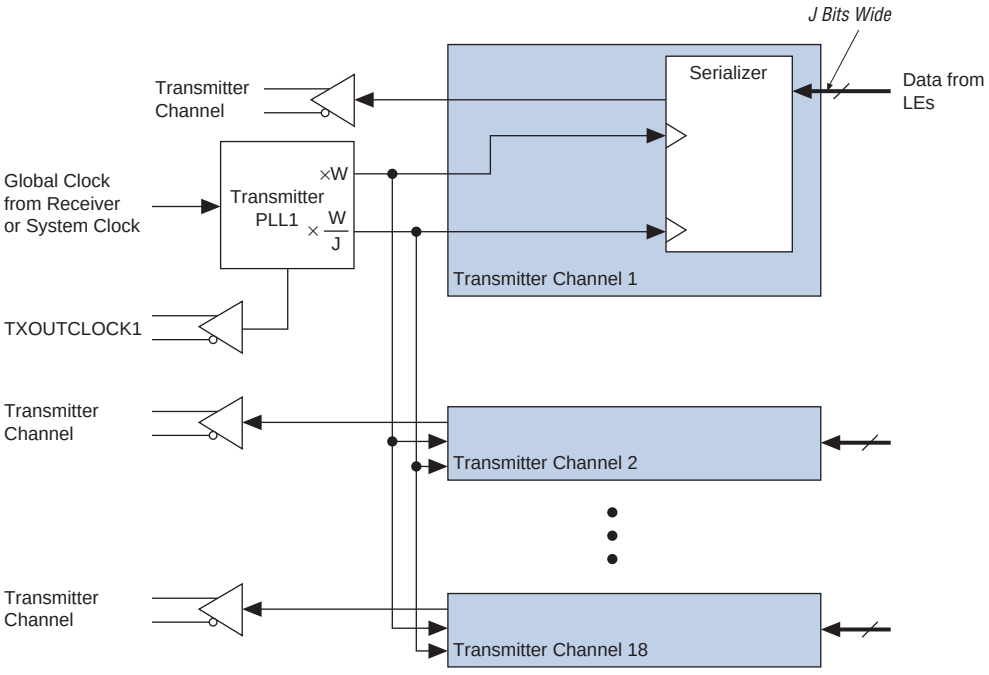
Notes to Figure 32:

(1) Two sets of 18 receiver channels are located in each APEX II device. Each set of 18 channels has one receiver PLL.

(2) *W* = 1, 2, 4 to 10
J = 1, 2, 4 to 10
W does not have to equal *J*. When *J* = 1 or 2, the deserializer is bypassed. When *J* = 2, DDR I/O registers are used.

(3) These clock pins drive receiver PLLs only. They do not drive directly to the logic array. However, the receiver PLL can drive the logic array via a global clock line.

Figure 33. True-LVDS Transmitter Diagram *Notes (1), (2)*



Notes to Figure 33:

(1) Two sets of 18 transmitter channels are located in each APEX II device. Each set of 18 channels has one transmitter PLL.

(2) *W* = 1, 2, 4 to 10
J = 1, 2, 4 to 10
W does not have to equal *J*. When *J* = 1 or 2, the deserializer is bypassed. When *J* = 2, DDR I/O registers are used.

Clock-Data Synchronization

In addition to dedicated serial-to-parallel converters, APEX II True-LVDS circuitry contains CDS circuitry in every receiver channel. The CDS feature can be turned on or off independently for each receiver channel. There are two modes for the CDS circuitry: single-bit mode, which corrects a fixed clock-to-data skew of up to ±50% of the data bit period, and multi-bit mode, which corrects any fixed clock-to-data skew.

Single-Bit Mode

Single-bit CDS corrects a fixed clock-to-data skew of up to ±50% of the data bit period, which allows receiver input skew margin (RSKM) to increase by 50% of the data period. To use single-bit CDS, the deserialization factor, *J*, must be equal to the multiplication factor, *W*. The combination of allowable *W* / *J* factors and the associated CDS training patterns automatically determine byte alignment (see Table 11).

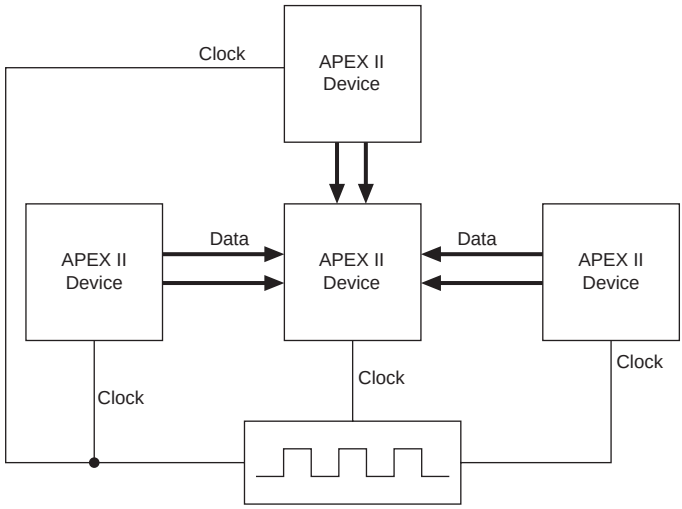
Table 11. Single-Bit CDS Training Patterns

W/J Factor	Single-Bit CDS Pattern
10	0000011111
9	000001111
8	00001111
7	0000111
6	000111
5	00011
4	0011

Multi-Bit Mode

Multi-bit CDS corrects any fixed clock-to-data skew. This feature enables flexible board topologies, such as an N:1 topology (see Figure 34), a switch topology, or a matrix topology. Multi-bit CDS corrects for the skews inherent with these topologies, making them possible to use.

Figure 34. Multi-Bit CDS Supports N:1 Topology



When using multi-bit CDS, the *J* and *W* factors do not need to be the same value. The byte boundary cannot be distinguished with multi-bit CDS patterns (see Table 12). Therefore, the byte must be aligned using internal logic. Table 12 shows the possible training patterns for multi-bit CDS. Either pattern can be used.

Table 12. Multi-Bit CDS Patterns

W Factor	J Factor	Multi-Bit CDS Pattern
1, 2, 4 to 10	4 to 10	3 × J-bits of `010101` pattern
1, 2, 4 to 10	4 to 10	3 × J-bits of `101010` pattern

Pre-Programmed CDS

When the fixed clock-to-data skew is known, CDS can be pre-programmed into the device during configuration. If CDS is pre-programmed into the device, the training patterns do not need to be transmitted to the receiver channels. The resolution of each pre-programmed setting is 25% of the data period, to compensate for skew up to ±50% of the data period.

Pre-programmed CDS may also be used to resolve clock-to-data skew greater than 50% of the bit period. However, internal logic must be used to implement the byte alignment circuitry for this operation.

Flexible-LVDS I/O Pins

A subset of pins in the top two I/O banks supports interfacing with Flexible-LVDS, LVPECL, and HyperTransport inputs. These Flexible-LVDS input pins include dedicated LVDS, LVPECL, and HyperTransport input buffers. A subset of pins in the bottom two I/O banks supports interfacing with Flexible-LVDS and HyperTransport outputs. These Flexible-LVDS output pins include dedicated LVDS and HyperTransport output buffers. The Flexible-LVDS pins do not require any external components except for 100-Ω termination resistors on receiver channels. These pins do not contain dedicated serialization / deserialization circuitry; therefore, internal logic is used to perform serialization / deserialization functions.

The EP2A15 and EP2A25 devices support 56 input and 56 output Flexible-LVDS channels. The EP2A40 and larger devices support 88 input and 88 output Flexible-LVDS channels. All APEX II devices support the Flexible-LVDS interface up to 400 Mbps (DDR) per channel. Flexible-LVDS pins along with the True-LVDS pins provide up to 144-Gbps total device bandwidth. Table 13 shows the Flexible-LVDS timing specification.

Table 13. APEX II Flexible-LVDS Timing Specification

Symbol	Timing Parameter Definition	Speed Grade						Unit
		-7		-8		-9		
		Min	Max	Min	Max	Min	Max	
Data Rate	Maximum operating speed		400		311		311	Mbps
TCCS	Transmitter channel-to-channel skew		700		900		900	ps
SW	Receiver sampling window	1,100		1,400		1,400		ps

MultiVolt I/O Interface

The APEX II architecture supports the MultiVolt I/O interface feature, which allows APEX II devices in all packages to interface with systems of different supply voltages. The devices have one set of V_{CC} pins for internal operation and input buffers (VCCINT), and another set for I/O output drivers (VCCIO).

The APEX II VCCINT pins must always be connected to a 1.5-V power supply. With a 1.5-V V_{CCINT} level, input pins are 1.5-V, 1.8-V, 2.5-V and 3.3-V tolerant. The VCCIO pins can be connected to either a 1.5-V, 1.8-V, 2.5-V or 3.3-V power supply, depending on the output requirements. The output levels are compatible with systems of the same voltage as the power supply (i.e., when VCCIO pins are connected to a 1.5-V power supply, the output levels are compatible with 1.5-V systems). When VCCIO pins are connected to a 3.3-V power supply, the output high is 3.3 V and is compatible with 3.3-V or 5.0-V systems.

Table 14 summarizes APEX II MultiVolt I/O support.

Table 14. APEX II MultiVolt I/O Support *Note (1)*

V_{CCIO} (V)	Input Signal					Output Signal				
	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V
1.5	✓	✓	✓	✓		✓				
1.8	✓ (2)	✓	✓	✓		✓ (3)	✓			
2.5	✓ (2)	✓ (2)	✓	✓		✓ (4)	✓ (4)	✓		
3.3	✓ (2)	✓ (2)	✓	✓	✓ (5)	✓ (6)	✓ (6)	✓ (6)	✓	✓

Notes to Table 14:

(1) The PCI clamping diode must be disabled to drive an input with voltages higher than V_{CCIO}, except for with a 5.0-V input.

(2) These input levels are only allowed if the input standard is set to any V_{REF} standard (i.e., SSTL-3, SSTL-2, HSTL, GTL+, and AGP 2×). The V_{REF} standard inputs are powered by V_{CCINT}. LVTTL, PCI, PCI-X, and AGP 1× standard inputs are powered by V_{CCIO}. As a result, input levels below the V_{CCIO} setting cannot drive these standards.

(3) When V_{CCIO} = 1.8 V, an APEX II device can drive a 1.5-V device with 1.8-V tolerant inputs.

(4) When V_{CCIO} = 2.5 V, an APEX II device can drive a 1.5-V or 1.8-V device with 2.5-V tolerant inputs.

(5) APEX II devices can be 5.0-V tolerant with the use of an external series resistor and enabling the PCI clamping diode.

(6) When V_{CCIO} = 3.3 V, an APEX II device can drive a 1.5-V, 1.8-V, or 2.5-V device with 3.3-V tolerant inputs.

Open-drain output pins with a pull-up resistor to the 5.0-V supply and a series register to the I/O pin can drive 5.0-V CMOS input pins that require a V_{IH} of 3.5 V. When the pin is inactive, the trace will be pulled up to 5.0 V by the resistor. The open-drain pin will only drive low or tri-state; it will never drive high. The rise time is dependent on the value of the pull-up resistor and load impedance. The I_{OL} current specification should be considered when selecting a pull-up resistor.

Power Sequencing & Hot Socketing

Because APEX II devices can be used in a mixed-voltage environment, they have been designed specifically for any possible power-up sequence. Therefore, the V_{CCIO} and V_{CCINT} power supplies may be powered in any order.

Signals can be driven into APEX II devices before and during power-up without damaging the device. In addition, APEX II devices do not drive out during power-up. Once operating conditions are reached and the device is configured, APEX II devices operate as specified by the user.

General-Purpose PLLs

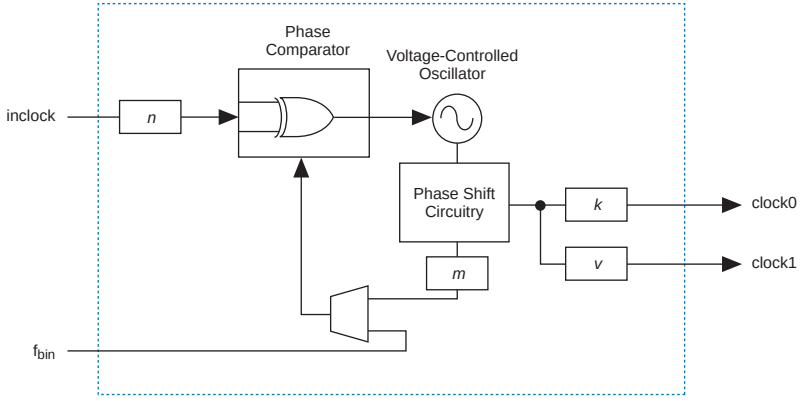
APEX II devices have ClockLock, ClockBoost, and ClockShift features, which use four general-purpose PLLs (separate from the four dedicated True-LVDS PLLs) to provide clock management and clock-frequency synthesis. These PLLs allow designers to increase performance and provide clock-frequency synthesis. The PLL reduces the clock delay within a device. This reduction minimizes clock-to-output and setup times while maintaining zero hold times. The PLLs, which provide programmable multiplication, allow the designer to distribute a low-speed clock and multiply that clock on-device. APEX II devices include a high-speed clock tree: unlike ASICs, the user does not have to design and optimize the clock tree. The PLLs work in conjunction with the APEX II device's high-speed clock to provide significant improvements in system performance and bandwidth.

The PLLs in APEX II devices are enabled through the Quartus II software. External devices are not required to use these features. Table 15 shows the general-purpose PLL features for APEX II devices. Figure 35 shows an APEX II general-purpose PLL.

Table 15. APEX II General-Purpose PLL Features

Number of PLLs	ClockBoost Feature	Number of External Clock Outputs	Number of Feedback Inputs
4	$m/(n \times k, v)$	8	2

Figure 35. APEX II General-Purpose PLL *Note (1)*



Note to Figure 35:

(1) *n* represents the prescale divider for the PLL input. *m* represents the multiplier. *k* and *v* represent the different post scale dividers for the two possible PLL outputs. *m* and *k* are integers that range from 1 to 160. *n* and *v* are integers that range from 1 to 16.

Advanced ClockBoost Multiplication & Division

APEX II PLLs include circuitry that provides clock synthesis for eight internal outputs and two external outputs using $m / (n \times \text{output divider})$ scaling. When a PLL is locked, the locked output clock aligns to the rising edge of the input clock. The closed loop equation for Figure 35 gives an output frequency $f_{clock0} = (m / (n \times k))f_{IN}$ and $f_{clock1} = (m / (n \times v))f_{IN}$. These equations allow the multiplication or division of clocks by a programmable number. The Quartus II software automatically chooses the appropriate scaling factors according to the frequency, multiplication, and division values entered.

A single PLL in an APEX II device allows for multiple user-defined multiplication and division ratios that are not possible even with multiple delay-locked loops (DLLs). For example, if a frequency scaling factor of 3.75 is needed for a given input clock, a multiplication factor of 15 and a division factor of 4 can be entered. This advanced multiplication scaling can be performed with a single PLL, making it unnecessary to cascade PLL outputs.

External Clock Outputs

APEX II devices have two low-jitter external clocks available for external clock sources. Other devices on the board can use these outputs as clock sources.

There are three modes for external clock outputs.

- Zero Delay Buffer: The external clock output pin is phase aligned with the clock input pin for zero delay. Multiplication, programmable phase shift, and time delay shift are not allowed in this configuration. The MegaWizard interface for `altclklock` should be used to verify possible clock settings.
- External Feedback: The external feedback input pin is phase aligned with clock input pin. By aligning these clocks, you can actively remove clock delay and skew between devices. This mode has the same restrictions as zero delay buffer mode.
- Normal Mode: The external clock output pin will have phase delay relative to the clock input pin. If an internal clock is used in this mode, the IOE register clock will be phase aligned to the input clock pin. Multiplication is allowed with the normal mode.

ClockShift Circuitry

General-purpose PLLs in APEX II devices have ClockShift circuitry that provides programmable phase shift. Users can enter a phase shift (in degrees or time units) that affects all PLL outputs. Phase shifts of 90°, 180°, and 270° can be implemented exactly. Other values of phase shifting, or delay shifting in time units, are allowed with a resolution range of 0.5 ns to 1.0 ns. This resolution varies with frequency input and the user-entered multiplication and division factors. The phase shift ability is only possible on a multiplied or divided clock if the input and output frequency have an integer multiple relationship (i.e., f_{IN}/f_{OUT} or f_{OUT}/f_{IN} must be an integer).

Clock Enable Signal

APEX II PLLs have a CLKLK_ENA pin for enabling/disabling all device PLLs. When the CLKLK_ENA pin is high, the PLL drives a clock to all its output ports. When the CLKLK_ENA pin is low, the clock0, clock1, and extclock ports are driven by GND and all of the PLLs go out of lock. When the CLKLK_ENA pin goes high again, the PLL relocks.

The individual enable port for each PLL is programmable. If more than one PLL is instantiated, each one does not have to use the clock enable. To enable/disable the device PLLs with the CLKLK_ENA pin, the inclocken port on the altclklock instance must be connected to the CLKLK_ENA input pin.

Lock Signals

The APEX II device PLL circuits support individual LOCK signals. The LOCK signal drives high when the PLL has locked onto the input clock. LOCK remains high as long as the input remains within specification. It will go low if the input is out of specification. A LOCK pin is optional for each PLL used in the APEX II devices; when not used, they are I/O pins. This signal is not available internally; if it is used in the logic array, it must be fed back in with an input pin.

SignalTap Embedded Logic Analyzer

APEX II devices include device enhancements to support the SignalTap embedded logic analyzer. By including this circuitry, the APEX II device provides the ability to monitor design operation over a period of time through the IEEE Std. 1149.1 (JTAG) circuitry; a designer can analyze internal logic at speed without bringing internal signals to the I/O pins. This feature is particularly important for advanced packages such as FineLine BGA packages because adding a connection to a pin during the debugging process can be difficult after a board is designed and manufactured.

IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

All APEX II devices provide JTAG BST circuitry that complies with the IEEE Std. 1149.1-1990 specification. JTAG boundary-scan testing can be performed before or after configuration, but not during configuration. APEX II devices can also use the JTAG port for configuration with the Quartus II software or with hardware using either Jam™ Standard Test and Programming Language (STAPL) Files (**.jam**) or Jam Byte-Code Files (**.jbc**). Finally, APEX II devices use the JTAG port to monitor the logic operation of the device with the SignalTap embedded logic analyzer. APEX II devices support the JTAG instructions shown in Table 16.

Table 16. APEX II JTAG Instructions

JTAG Instruction	Description
SAMPLE/PRELOAD	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins. Also used by the SignalTap embedded logic analyzer.
EXTEST *(1)*	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation.
USERCODE	Selects the 32-bit USERCODE register and places it between the TDI and TDO pins, allowing the USERCODE to be serially shifted out of TDO.
IDCODE	Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO.
HIGHZ *(1)*	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation, while tri-stating all of the I/O pins.
CLAMP *(1)*	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation while holding I/O pins to a state defined by the data in the boundary-scan register.
ICR instructions	Used when configuring an APEX II device via the JTAG port with a MasterBlaster™ or ByteBlasterMV™ download cable, or when using a Jam File or Jam Byte-Code File via an embedded processor.
SignalTap instructions	Monitors internal device operation with the SignalTap embedded logic analyzer.

Note to Table 16:

(1) Bus hold and weak pull-up features override the high-impedance state of HIGHZ, CLAMP, and EXTEST.

The APEX II device instruction register length is 10 bits. The APEX II device USERCODE register length is 32 bits. Tables 17 and 18 show the boundary-scan register length and device IDCODE information for APEX II devices.

Table 17. APEX II JTAG Boundary-Scan Register Length

Device	Boundary-Scan Register Length
EP2A15	1,524
EP2A25	1,884
EP2A40	2,328
EP2A70	3,228

Table 18. 32-Bit APEX II Device IDCODE

Device	IDCODE (32 Bits) *(1)*			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer Identity (11 Bits)	1 (1 Bit) *(2)*
EP2A15	0000	1100 0100 0000 0000	000 0110 1110	1
EP2A25	0000	1100 0110 0000 0000	000 0110 1110	1
EP2A40	0000	1101 0000 0000 0000	000 0110 1110	1
EP2A70	0000	1110 0000 0000 0000	000 0110 1110	1

Notes to Tables 17 and 18:

(1) The most significant bit (MSB) is on the left.

(2) The IDCODE's least significant bit (LSB) is always 1.

Figure 36 shows the timing requirements for the JTAG signals.

Figure 36. APEX II JTAG Waveforms

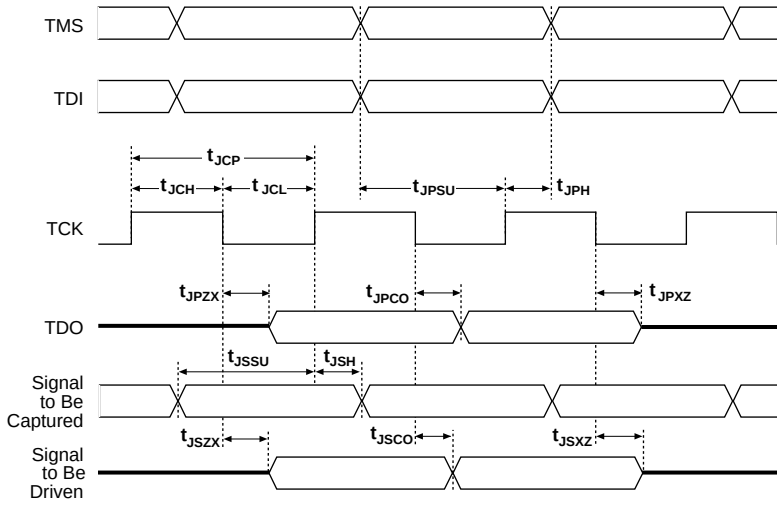


Table 19 shows the JTAG timing parameters and values for APEX II devices.

Table 19. APEX II JTAG Timing Parameters & Values

Symbol	Parameter	Min	Max	Unit
t_{JCP}	TCK clock period	100		ns
t_{JCH}	TCK clock high time	50		ns
t_{JCL}	TCK clock low time	50		ns
t_{JPSU}	JTAG port setup time	20		ns
t_{JPH}	JTAG port hold time	45		ns
t_{JPCO}	JTAG port clock to output		25	ns
t_{JPZX}	JTAG port high impedance to valid output		25	ns
t_{JPXZ}	JTAG port valid output to high impedance		25	ns
t_{JSSU}	Capture register setup time	20		ns
t_{JSH}	Capture register hold time	45		ns
t_{JSCO}	Update register clock to output		35	ns
t_{JSZX}	Update register high impedance to valid output		35	ns
t_{JSXZ}	Update register valid output to high impedance		35	ns

For more information, see the following documents:

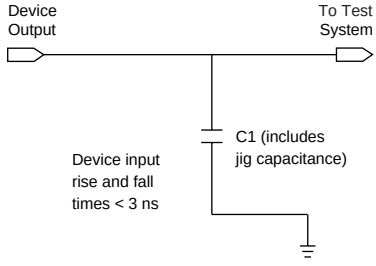
- *Application Note 39 (IEEE Std. 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)*
- *Jam Programming & Test Language Specification*

Generic Testing

Each APEX II device is functionally tested. Complete testing of each configurable static random access memory (SRAM) bit and all logic functionality ensures 100% yield. AC test measurements for APEX II devices are made under conditions equivalent to those shown in Figure 37. Multiple test patterns can be used to configure devices during all stages of the production flow. AC test criteria include:

- Power supply transients can affect AC measurements.
- Simultaneous transitions of multiple outputs should be avoided for accurate measurement.
- Threshold tests must not be performed under AC conditions.
- Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result.

Figure 37. APEX II AC Test Conditions



Operating Conditions

APEX II devices are offered in both commercial and industrial grades. However, industrial-grade devices may have limited speed-grade availability.

Tables 20 through 41 provide information on absolute maximum ratings, recommended operating conditions, and DC operating conditions for 1.5-V APEX II devices.

Table 20. APEX II Device Absolute Maximum Ratings *Notes (1), (2)*

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCINT}	Supply voltage	With respect to ground *(3)*	–0.5	2.4	V
V_{CCIO}			–0.5	4.6	V
V_I	DC input voltage		–0.5	4.6	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	BGA packages under bias		135	° C

Table 21. APEX II Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	*(4)*	1.425	1.575	V
V_{CCIO}	Supply voltage for output buffers, 3.3-V operation	*(4)*, *(5)*	3.00 (3.135)	3.60 (3.465)	V
	Supply voltage for output buffers, 2.5-V operation	*(4)*	2.375	2.625	V
	Supply voltage for output buffers, 1.8-V operation	*(4)*	1.71	1.89	V
	Supply voltage for output buffers, 1.5-V operation	*(4)*	1.4	1.6	V
V_I	Input voltage	*(3)*, *(6)*	–0.5	4.1	V
V_O	Output voltage		0	V_{CCIO}	V
T_J	Operating junction temperature	For commercial use	0	85	° C
		For industrial use	–40	100	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

Table 22. APEX II Device DC Operating Conditions *Note (7)*

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
I_I	Input pin leakage current	$V_I = V_{CCIO}$ to 0 V *(8)*	–10		10	µA
I_{OZ}	Tri-stated I/O pin leakage current	$V_O = V_{CCIO}$ to 0 V *(8)*	–10		10	µA
I_{CC0}	V_{CC} supply current (standby) (All ESBs in power-down mode)	V_I = ground, no load, no toggling inputs, -7 speed grade		10		mA
		V_I = ground, no load, no toggling inputs, -8, -9 speed grades		5		mA
R_{CONF}	Value of I/O pin pull-up resistor before and during configuration	V_{CCIO} = 3.0 V *(9)*	20		50	kΩ
		V_{CCIO} = 2.375 V *(9)*	30		80	kΩ
		V_{CCIO} = 1.71 V *(9)*	60		150	kΩ

Table 23. LVTTL Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO}	Output supply voltage		3.0	3.6	V
V_{IH}	High-level input voltage		1.7	4.1	V
V_{IL}	Low-level input voltage		–0.5	0.8	V
I_I	Input pin leakage current	V_{IN} = 0 V or V_{CCIO}	–5	5	µA
V_{OH}	High-level output voltage	I_{OH} = –4 to –24 mA *(10)*	2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4 to 24 mA *(10)*		0.45	V

Table 24. LVCMOS Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO}	Output supply voltage		3.0	3.6	V
V_{IH}	High-level input voltage		1.7	4.1	V
V_{IL}	Low-level input voltage		–0.5	0.7	V
I_I	Input pin leakage current	V_{IN} = 0 V or V_{CCIO}	–10	10	µA
V_{OH}	High-level output voltage	V_{CCIO} = 3.0, I_{OH} = –0.1 mA	V_{CCIO} – 0.2		V
V_{OL}	Low-level output voltage	V_{CCIO} = 3.0, I_{OL} = 0.1 mA		0.2	V

Table 25. 2.5-V I/O Specifications *Note (10)*

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO}	Output supply voltage		2.375	2.625	V
V_{IH}	High-level input voltage		1.7	4.1	V
V_{IL}	Low-level input voltage		–0.5	0.7	V
I_I	Input pin leakage current	V_{IN} = 0 V or V_{CCIO}	–10	10	µA
V_{OH}	High-level output voltage	I_{OH} = –0.1 mA	2.1		V
		I_{OH} = –1 mA	2.0		V
		I_{OH} = –2 to –16 mA	1.7		V
V_{OL}	Low-level output voltage	I_{OL} = 0.1 mA		0.2	V
		I_{OL} = 1 mA		0.4	V
		I_{OL} = 2 to 16 mA		0.7	V

Table 26. 1.8-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO}	Output supply voltage		1.65	1.95	V
V_{IH}	High-level input voltage		$0.65 \times V_{CCIO}$	4.1	V
V_{IL}	Low-level input voltage		–0.5	$0.35 \times V_{CCIO}$	V
I_I	Input pin leakage current	V_{IN} = 0 V or V_{CCIO}	–10	10	µA
V_{OH}	High-level output voltage	I_{OH} = –2 to –8 mA *(10)*	V_{CCIO} – 0.45		V
V_{OL}	Low-level output voltage	I_{OL} = 2 to 8 mA *(10)*		0.45	V

Table 27. 1.5-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO}	Output supply voltage		1.4	1.6	V
V_{IH}	High-level input voltage		$0.65 \times V_{CCIO}$	4.1	V
V_{IL}	Low-level input voltage		–0.5	$0.35 \times V_{CCIO}$	V
I_I	Input pin leakage current	V_{IN} = 0 V or V_{CCIO}	–10	10	µA
V_{OH}	High-level output voltage	I_{OH} = –2 mA *(10)*	$0.75 \times V_{CCIO}$		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA *(10)*		$0.25 \times V_{CCIO}$	V

Table 28. 3.3-V PCI Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		3.0	3.3	3.6	V
V_{IH}	High-level input voltage		0.5 × V_{CCIO}		V_{CCIO} + 0.5	V
V_{IL}	Low-level input voltage		–0.5		0.3 × V_{CCIO}	V
I_I	Input pin leakage current	$0 < V_{IN} < V_{CCIO}$	–10		10	µA
V_{OH}	High-level output voltage	I_{OUT} = –500 µA	0.9 × V_{CCIO}			V
V_{OL}	Low-level output voltage	I_{OUT} = 1,500 µA			0.1 × V_{CCIO}	V

Table 29. PCI-X Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		3.0		3.6	V
V_{IH}	High-level input voltage		0.5 × V_{CCIO}		V_{CCIO} + 0.5	V
V_{IL}	Low-level input voltage		–0.5		0.35 × V_{CCIO}	V
V_{IPU}	Input pull-up voltage		0.7 × V_{CCIO}			V
I_{IL}	Input leakage current	$0 < V_{IN} < V_{CCIO}$	–10		10	µA
V_{OH}	High-level output voltage	I_{OUT} = –500 µA	0.9 × V_{CCIO}			V
V_{OL}	Low-level output voltage	I_{OUT} = 1,500 µA			0.1 × V_{CCIO}	V
L_{PIN}	Pin inductance				15	nH

Table 30. GTL+ I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{TT}	Termination voltage		1.35	1.5	1.65	V
V_{REF}	Reference voltage		0.88	1.0	1.12	V
V_{IH}	High-level input voltage		V_{REF} + 0.1			V
V_{IL}	Low-level input voltage				V_{REF} – 0.1	V
V_{OL}	Low-level output voltage	I_{OL} = 36 mA *(10)*			0.65	V

Table 31. SSTL-2 Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		2.375	2.5	2.625	V
V_{TT}	Termination voltage		V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
V_{REF}	Reference voltage		1.15	1.25	1.35	V
V_{IH}	High-level input voltage		V_{REF} + 0.18		3.0	V
V_{IL}	Low-level input voltage		–0.3		V_{REF} – 0.18	V
V_{OH}	High-level output voltage	I_{OH} = –7.6 mA *(10)*	V_{TT} + 0.57			V
V_{OL}	Low-level output voltage	I_{OL} = 7.6 mA *(10)*			V_{TT} – 0.57	V

Table 32. SSTL-2 Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		2.3	2.5	2.7	V
V_{TT}	Termination voltage		V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
V_{REF}	Reference voltage		1.15	1.25	1.35	V
V_{IH}	High-level input voltage		V_{REF} + 0.18		V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		V_{REF} – 0.18	V
V_{OH}	High-level output voltage	I_{OH} = –15.2 mA *(10)*	V_{TT} + 0.76			V
V_{OL}	Low-level output voltage	I_{OL} = 15.2 mA *(10)*			V_{TT} – 0.76	V

Table 33. SSTL-3 Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		3.0	3.3	3.6	V
V_{TT}	Termination voltage		V_{REF} – 0.05	V_{REF}	V_{REF} + 0.05	V
V_{REF}	Reference voltage		1.3	1.5	1.7	V
V_{IH}	High-level input voltage		V_{REF} + 0.2		V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = –8 mA *(10)*	V_{TT} + 0.6			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA *(10)*			V_{TT} – 0.6	V

Table 34. SSTL-3 Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		3.0	3.3	3.6	V
V_{TT}	Termination voltage		V_{REF} – 0.05	V_{REF}	V_{REF} + 0.05	V
V_{REF}	Reference voltage		1.3	1.5	1.7	V
V_{IH}	High-level input voltage		V_{REF} + 0.2		V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = –16 mA *(10)*	V_{TT} + 0.8			V
V_{OL}	Low-level output voltage	I_{OL} = 16 mA *(10)*			V_{TT} – 0.8	V

Table 35. 3.3-V AGP 2× Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		3.15	3.3	3.45	V
V_{REF}	Reference voltage		$0.39 \times V_{CCIO}$		$0.41 \times V_{CCIO}$	V
V_{IH}	High-level input voltage *(11)*		$0.5 \times V_{CCIO}$		V_{CCIO} + 0.5	V
V_{IL}	Low-level input voltage *(11)*				$0.3 \times V_{CCIO}$	V
V_{OH}	High-level output voltage	I_{OUT} = –20 µA	$0.9 \times V_{CCIO}$		3.6	V
V_{OL}	Low-level output voltage	I_{OUT} = 20 µA			$0.1 \times V_{CCIO}$	V
I_I	Input pin leakage current	$0 < V_{IN} < V_{CCIO}$	–10		10	µA

Table 36. 3.3-V AGP 1× Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		3.15	3.3	3.45	V
V_{IH}	High-level input voltage *(11)*		$0.5 \times V_{CCIO}$		V_{CCIO} + 0.5	V
V_{IL}	Low-level input voltage *(11)*				$0.3 \times V_{CCIO}$	V
V_{OH}	High-level output voltage	I_{OUT} = –20 µA	$0.9 \times V_{CCIO}$		3.6	V
V_{OL}	Low-level output voltage	I_{OUT} = 20 µA			$0.1 \times V_{CCIO}$	V
I_I	Input pin leakage current	$0 < V_{IN} < V_{CCIO}$	–10		10	µA

Table 37. 1.5-V HSTL Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		1.4	1.5	1.6	V
V_{REF}	Input reference voltage		0.68	0.75	0.9	V
V_{TT}	Termination voltage		0.7	0.75	0.8	V
V_{IH} (DC)	DC high-level input voltage		V_{REF} + 0.1			V
V_{IL} (DC)	DC low-level input voltage		–0.3		V_{REF} – 0.1	V
V_{IH} (AC)	AC high-level input voltage		V_{REF} + 0.2			V
V_{IL} (AC)	AC low-level input voltage				V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = 8 mA *(10)*	V_{CCIO} – 0.4			V
V_{OL}	Low-level output voltage	I_{OL} = –8 mA *(10)*			0.4	V

Table 38. 1.5-V HSTL Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		1.4	1.5	1.6	V
V_{REF}	Input reference voltage		0.68	0.75	0.9	V
V_{TT}	Termination voltage		0.7	0.75	0.8	V
V_{IH} (DC)	DC high-level input voltage		V_{REF} + 0.1			V
V_{IL} (DC)	DC low-level input voltage		–0.3		V_{REF} – 0.1	V
V_{IH} (AC)	AC high-level input voltage		V_{REF} + 0.2			V
V_{IL} (AC)	AC low-level input voltage				V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = 16 mA *(10)*	V_{CCIO} – 0.4			V
V_{OL}	Low-level output voltage	I_{OL} = –16 mA *(10)*			0.4	V

Table 39. 1.5-V Differential HSTL Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		1.4	1.5	1.6	V
V_{DIF} (DC)	DC input differential voltage		0.2			V
V_{CM} (DC)	DC common mode input voltage		0.68		0.9	V
V_{DIF} (AC)	AC differential input voltage		0.4			V

Table 40. CTT I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		3.0	3.3	3.6	V
V_{TT}/V_{REF}	Termination and input reference voltage		1.35	1.5	1.65	V
V_{IH}	High-level input voltage		V_{REF} + 0.2			V
V_{IL}	Low-level input voltage				V_{REF} – 0.2	V
I_I	Input pin leakage current	$0 < V_{IN} < V_{CCIO}$	–10		10	µA
V_{OH}	High-level output voltage	I_{OH} = –8 mA	V_{REF} + 0.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA			V_{REF} – 0.4	V
I_O	Output leakage current (when output is high *Z*)	GND ð V_{OUT} ð V_{CCIO}	–10		10	µA

Table 41. Bus Hold Parameters

Parameter	Conditions	V_{CCIO} Level								Units
		1.5 V		1.8 V		2.5 V		3.3 V		
		Min	Max	Min	Max	Min	Max	Min	Max	
Low sustaining current	$V_{IN} > V_{IL}$ (maximum)			30		50		70		µA
High sustaining current	$V_{IN} < V_{IH}$ (minimum)			–30		–50		–70		µA
Low overdrive current	$0 V < V_{IN} < V_{CCIO}$				200		300		500	µA
High overdrive current	$0 V < V_{IN} < V_{CCIO}$				–200		–300		–500	µA

Notes to Tables 20 – 41:

(1) See the *Operating Requirements for Altera Devices Data Sheet*.
(2) Conditions beyond those listed in Table 20 may cause permanent damage to a device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse affects on the device.
(3) Minimum DC input is –0.5 V. During transitions, the inputs may undershoot to - 2 V or overshoot to 4.6 V for input currents less than 100 mA and periods shorter than 20 ns.
(4) Maximum V_{CC} rise time is 100 ms, and V_{CC} must rise monotonically.
(5) V_{CCIO} maximum and minimum conditions for LVPECL, LVDS, RapidIO, and PCML are shown in parentheses.
(6) All pins, including dedicated inputs, clock, I/O, and JTAG pins, may be driven before V_{CCINT} and V_{CCIO} are powered.
(7) Typical values are for T_A = 25° C, V_{CCINT} = 1.5 V, and V_{CCIO} = 1.5 V, 1.8 V, 2.5 V, and 3.3 V.
(8) This value is specified for normal device operation. The value may vary during power-up.
(9) Pin pull-up resistance values will lower if an external source drives the pin higher than V_{CCIO}.
(10) Drive strength is programmable according to values in Table 9 on page 48.
(11) V_{REF} specifies the center point of the switching range.

Figures 38 and 39 show receiver input and transmitter output waveforms, respectively, for all differential I/O standards (LVDS, 3.3-V PCML, LVPECL, and HyperTransport technology).

Figure 38. Receiver Input Waveforms for Differential I/O Standards

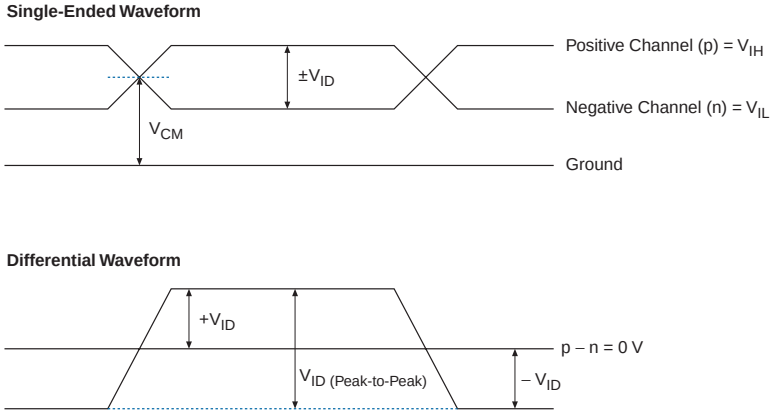
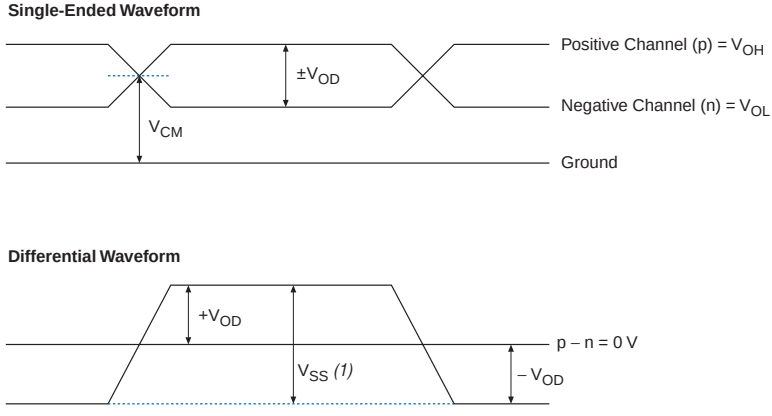


Figure 39. Transmitter Output Waveforms for Differential I/O Standards



Note to Figure 39:
(1) V_{SS}: steady-state differential output voltage.

Tables 42 through 45 provide information on absolute maximum ratings, recommended operating conditions, and DC operating conditions for 1.5-V APEX II devices.

Table 42. 3.3-V LVDS I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		3.135	3.3	3.465	V
V_{OD}	Differential output voltage	R_L = 100 Ω	250		850 *(1)*	mV
ΔV_{OD}	Change in V_{OD} between high and low	R_L = 100 Ω			50	mV
V_{OS}	Output Offset voltage	R_L = 100 Ω	1.125	1.25	1.375	V
ΔV_{OS}	Change in V_{OS} between high and low	R_L = 100 Ω			50	mV
V_{TH}	Differential input threshold	V_{CM} = 1.2 V	–100		100	mV
V_{IN}	Receiver input voltage range		0.0		2.4	V
R_L	Receiver differential input resistor (external to APEX II devices)		90	100	110	Ω

Table 43. 3.3-V PCML Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		3.135	3.3	3.465	V
V_{IL}	Low-level input voltage				V_{CCIO} – 0.3	V
V_{IH}	High-level input voltage		V_{CCIO}			V
V_{OL}	Low-level output voltage		V_{CCIO} – 0.6		V_{CCIO} – 0.3	V
V_{OH}	High-level output voltage		V_{CCIO}		V_{CCIO} – 0.3	V
V_T	Output termination voltage			V_{CCIO}		V
V_{OD}	Differential output voltage		300	450	600	mV
t_R	Rise time (20 to 80%)		85		325	ps
t_F	Fall time (20 to 80%)		85		325	ps
R_O	Output load			100		Ω
R_L	Receiver differential input resistor		45	50	55	Ω

Table 44. LVPECL Specifications *Note (2)*

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		3.135	3.3	3.465	V
V_{IL}	Low-level input voltage		800		2,000	mV
V_{IH}	High-level input voltage		2,100		V_{CCIO}	mV
V_{OL}	Low-level output voltage		1,450		1,650	mV
V_{OH}	High-level output voltage		2,275		2,420	mV
V_{ID}	Differential input voltage		100	600	2,500	mV
V_{OD}	Differential output voltage		625	800	970	mV
t_R	Rise time (20 to 80%)		85		325	ps
t_F	Fall time (20 to 80%)		85		325	ps

Table 45. HyperTransport Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		2.375	2.5	2.625	V
V_{OD}	Differential output voltage		380	600	820	mV
V_{OCM}	Output common mode voltage	R_{TT} = 100 Ω	500	600	700	mV
V_{ID}	Differential input voltage		300	600	900	mV
V_{ICM}	Input common mode voltage		450	600	750	mV
R_L	Receiver differential input resistor		90	100	110	Ω

Notes to Tables 42 – 45:

(1) Maximum V_{OD} is measured under static conditions.

(2) When APEX II devices drive LVPECL signals, the APEX II LVPECL outputs must be terminated with a resistor network.

Capacitance

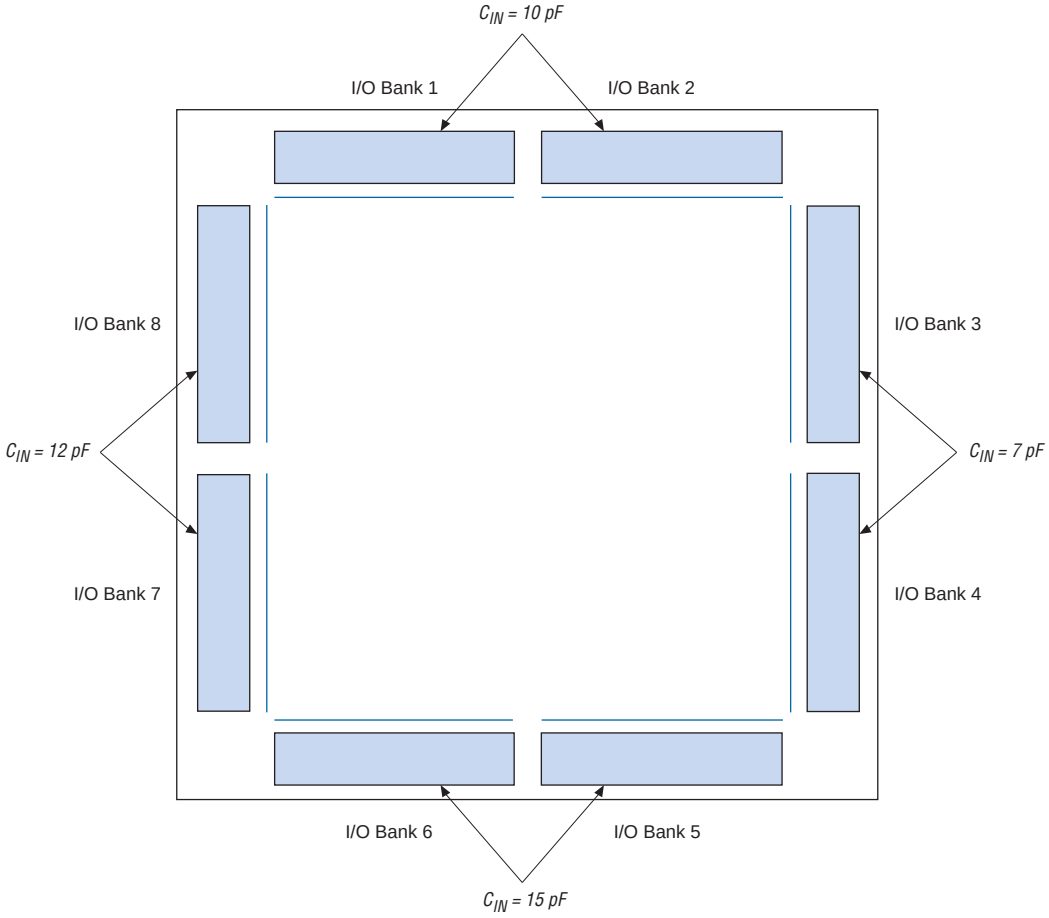
Table 46 and Figure 40 provide information on APEX II device capacitance.

Table 46. APEX II Device Capacitance

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		*(1)*	pF
C_{INCLK}	Input capacitance on dedicated clock pin	V_{IN} = 0 V, f = 1.0 MHz		12	pF
C_{OUT}	Output capacitance	V_{IN} = 0 V, f = 1.0 MHz		*(1)*	pF

Note to Table 46:
(1) See Figure 40.

Figure 40. APEX II Maximum Input & Output Pin Capacitance



Timing Model

The high-performance FastTrack and MegaLAB interconnect routing structures ensure predictable performance, and accurate simulation and timing analysis. In contrast, the unpredictable performance of FPGAs is caused by their segmented connection scheme.

All specifications are always representative of worst-case supply voltage and junction temperature conditions. All output-pin-timing specifications are reported for maximum drive strength.

Figure 41 shows the f_{MAX} timing model for APEX II devices. These parameters can be used to estimate f_{MAX} for multiple levels of logic. However, the Quartus II software timing analysis provides more accurate timing information because the Quartus II software usually has more up-to-date timing information than the data sheet until the timing model is final. Also, the Quartus II software can model delays caused by loading and distance effects more accurately than by using the numbers in this data sheet.

Figure 41. f_{MAX} Timing Model

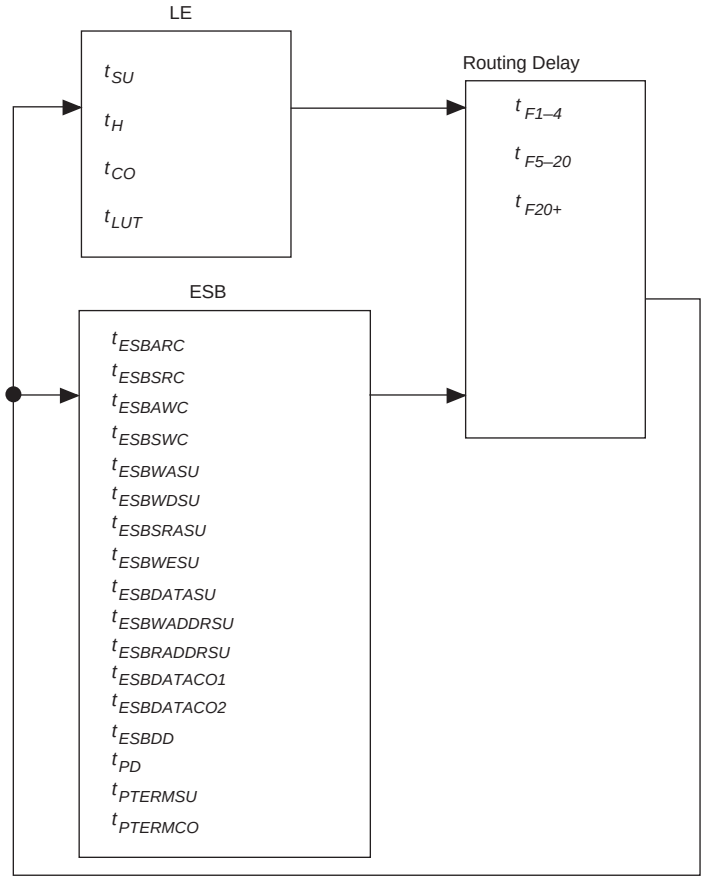
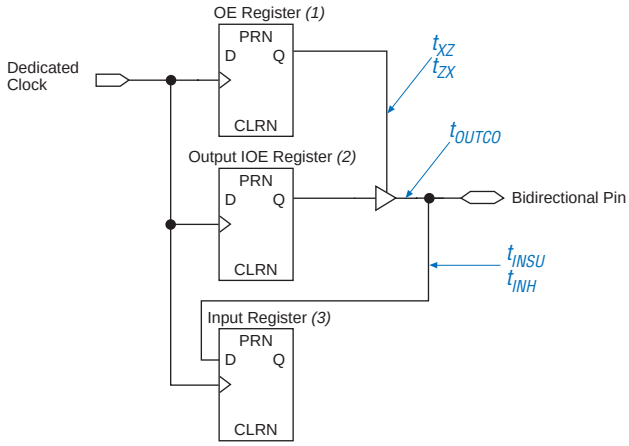


Figure 42 shows the timing model for bi-directional, input, and output IOE timing.

Figure 42. Synchronous External TIming Model



Notes to Figure 42:

(1) The output enable register is in the IOE and is controlled by the "Fast Output Enable Register = ON" option in the Quartus II software.

(2) The output register is in the IOE and is controlled by the "Fast Output Register = ON" option in the Quartus II software.

(3) The input register is in the IOE and is controlled by the "Fast Input Register = ON" option in the Quartus II software.

Tables 47 through 50 show APEX II LE, ESB, and routing delays and minimum pulse-width timing parameters for the f_{MAX} timing model.

Table 47. APEX II f_{MAX} LE Timing Parameters

Symbol	Parameter
t_{SU}	LE register setup time before clock
t_{H}	LE register hold time before clock
t_{CO}	LE register clock-to-output delay
t_{LUT}	LUT delay for data-in to data-out

Table 48. APEX II f_{MAX} ESB Timing Parameters	
Symbol	**Parameter**
t_{ESBARC}	ESB asynchronous read cycle time
t_{ESBSRC}	ESB synchronous read cycle time
t_{ESBAWC}	ESB asynchronous write cycle time
t_{ESBSWC}	ESB synchronous write cycle time
$t_{ESBWASU}$	ESB write address setup time with respect to WE
t_{ESBWAH}	ESB write address hold time with respect to WE
$t_{ESBWDSU}$	ESB data setup time with respect to WE
t_{ESBWDH}	ESB data hold time with respect to WE
$t_{ESBRASU}$	ESB read address setup time with respect to RE
t_{ESBRAH}	ESB read address hold time with respect to RE
$t_{ESBWESU}$	ESB WE setup time before clock when using input register
$t_{ESBDATASU}$	ESB data setup time before clock when using input register
$t_{ESBWADDRSU}$	ESB write address setup time before clock when using input registers
$t_{ESBRADDRSU}$	ESB read address setup time before clock when using input registers
$t_{ESBDATACO1}$	ESB clock-to-output delay when using output registers
$t_{ESBDATACO2}$	ESB clock-to-output delay without output registers
t_{ESBDD}	ESB data-in to data-out delay for RAM mode
t_{PD}	ESB macrocell input to non-registered output
$t_{PTERMSU}$	ESB macrocell register setup time before clock
$t_{PTERMCO}$	ESB macrocell register clock-to-output delay

Figure shows the dual-port RAM timing microparameter waveform.

Figure 43. Dual-Port RAM Timing Microparameter Waveform

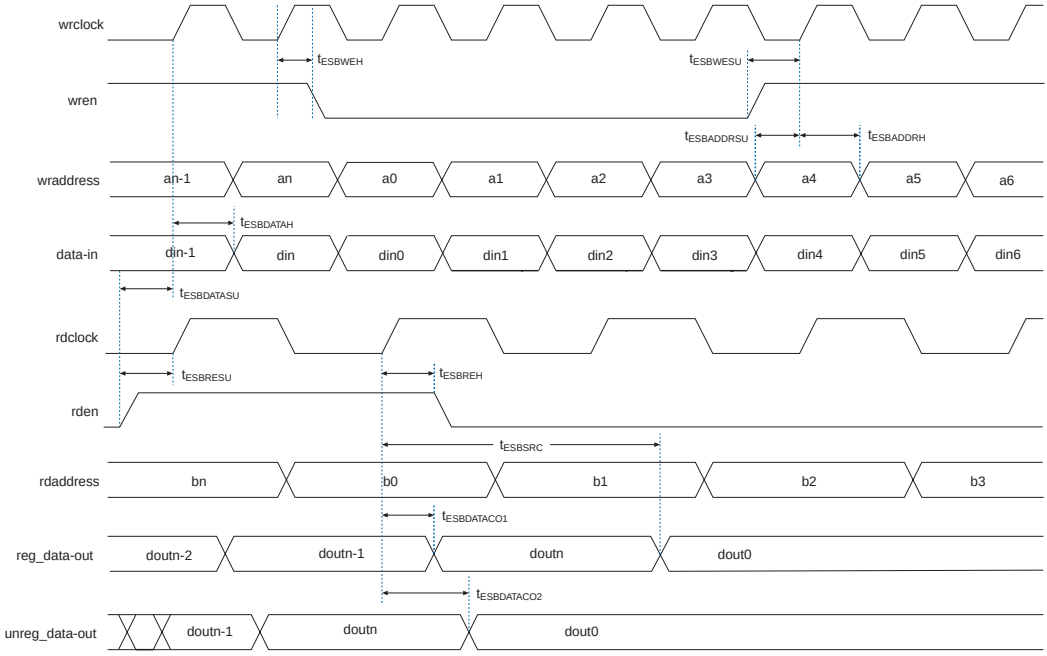


Table 49. APEX II f_{MAX} Routing Delays	
Symbol	**Parameter**
t_{F1-4}	Fan-out delay estimate using local interconnect; use to estimate routing delay for a signal with fan-out of 1 to 4
t_{F5-20}	Fan-out delay estimate using MegaLab interconnect; use to estimate routing delay for a signal with fan-out of 5 to 20
t_{F20+}	Fan-out delay estimate using FastTrack interconnect; use to estimate routing delay for a signal with fan-out greater than 20

Table 50. APEX II Minimum Pulse Width Timing Parameters	
Symbol	**Parameter**
t_{CH}	Minimum clock high time from clock pin
t_{CL}	Minimum clock low time from clock pin
t_{CLRP}	LE clear pulse width
t_{PREP}	LE preset pulse width
t_{ESBCH}	Clock high time
t_{ESBCL}	Clock low time
t_{ESBWP}	Write pulse width
t_{ESBRP}	Read pulse width

Table 51. APEX II External Timing Parameters *Note (1)*		
Symbol	**Parameter**	**Conditions**
t_{INSU}	Setup time with global clock at IOE input register	
t_{INH}	Hold time with global clock at IOE input register	
t_{OUTCO}	Clock-to-output delay with global clock at IOE output register	C1 = 35 pF
t_{XZ}	Clock-to-output buffer disable delay	
t_{ZX}	Clock-to-output buffer enable delay	Slow slew rate = OFF
$t_{INSUPLL}$	Setup time with PLL clock at IOE input register	
t_{INHPLL}	Hold time with PLL clock at IOE input register	
$t_{OUTCOPLL}$	Clock-to-output delay with PLL clock at IOE output register	C1 = 35 pF
t_{XZPLL}	PLL clock-to-output buffer disable delay	
t_{ZXPLL}	PLL clock-to-output buffer enable delay	Slow slew rate = OFF

Note to Table 51:

(1) External timing parameters are factory tested, worst-case values specified by Altera. These timing parameters are sample-tested only.

Tables 52 through 67 show the APEX II device f_{MAX} and functional timing parameters.

Table 52. EP2A15 f_{MAX} LE Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.25		0.29		0.33		ns
t_{H}	0.25		0.29		0.33		ns
t_{CO}		0.18		0.20		0.23	ns
t_{LUT}		0.53		0.61		0.70	ns

Table 53. EP2A15 f_{MAX} ESB Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.28		1.47		1.69	ns
t_{ESBSRC}		2.49		2.86		3.29	ns
t_{ESBAWC}		2.20		2.53		2.91	ns
t_{ESBSWC}		3.02		3.47		3.99	ns
$t_{ESBWASU}$	– 0.55		– 0.64		– 0.73		ns
t_{ESBWAH}	0.15		0.18		0.20		ns
$t_{ESBWDSU}$	0.37		0.43		0.49		ns
t_{ESBWDH}	0.16		0.18		0.21		ns
$t_{ESBRASU}$	0.84		0.96		1.11		ns
t_{ESBRAH}	0.00		0.00		0.00		ns
$t_{ESBWESU}$	0.14		0.16		0.19		ns
$t_{ESBDATASU}$	– 0.02		– 0.03		– 0.03		ns
$t_{ESBWADDRSU}$	– 0.40		– 0.46		– 0.53		ns
$t_{ESBRADDRSU}$	– 0.38		– 0.44		– 0.51		ns
$t_{ESBDATACO1}$		1.30		1.50		1.72	ns
$t_{ESBDATACO2}$		1.84		2.12		2.44	ns
t_{ESBDD}		2.42		2.78		3.19	ns
t_{PD}		1.69		1.94		2.23	ns
$t_{PTERMSU}$	1.10		1.26		1.45		ns
$t_{PTERMCO}$		0.82		0.94		1.08	ns

Table 54. EP2A15 f_{MAX} Routing Delays

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}	0.19		0.21		0.25		ns
t_{F5-20}	0.64		0.73		0.84		ns
t_{F20+}	1.18		1.35		1.56		ns

Table 55. EP2A15 Minimum Pulse Width Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{CH}	1.00		1.15		1.32		ns
t_{CL}	1.00		1.15		1.32		ns
t_{CLRP}	0.13		0.15		0.17		ns
t_{PREP}	0.13		0.15		0.17		ns
t_{ESBCH}	1.00		1.15		1.32		ns
t_{ESBCL}	1.00		1.15		1.32		ns
t_{ESBWP}	1.12		1.28		1.48		ns
t_{ESBRP}	0.88		1.02		1.17		ns

Table 56. EP2A25 f_{MAX} LE Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.25		0.29		0.33		ns
t_{H}	0.25		0.29		0.33		ns
t_{CO}		0.18		0.20		0.23	ns
t_{LUT}		0.53		0.61		0.70	ns

Table 57. EP2A25 f_{MAX} ESB Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.28		1.47		1.69	ns
t_{ESBSRC}		2.49		2.86		3.29	ns
t_{ESBAWC}		2.20		2.53		2.91	ns
t_{ESBSWC}		3.02		3.47		3.99	ns
$t_{ESBWASU}$	0.07		0.07		0.09		ns
t_{ESBWAH}	0.15		0.18		0.20		ns
$t_{ESBWDSU}$	0.37		0.43		0.49		ns
t_{ESBWDH}	0.16		0.18		0.21		ns
$t_{ESBRASU}$	0.84		0.96		1.11		ns
t_{ESBRAH}	0.00		0.00		0.00		ns
$t_{ESBWESU}$	0.14		0.16		0.19		ns
$t_{ESBDATASU}$	– 0.02		– 0.03		– 0.03		ns
$t_{ESBWADDRSU}$	– 0.40		– 0.46		– 0.53		ns
$t_{ESBRADDRSU}$	– 0.38		– 0.44		– 0.51		ns
$t_{ESBDATACO1}$		1.30		1.50		1.72	ns
$t_{ESBDATACO2}$		1.84		2.12		2.44	ns
t_{ESBDD}		2.42		2.78		3.19	ns
t_{PD}		1.69		1.94		2.23	ns
$t_{PTERMSU}$	1.10		1.26		1.45		ns
$t_{PTERMCO}$		0.82		0.94		1.08	ns

Table 58. EP2A25 f_{MAX} Routing Delays

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}	0.19		0.21		0.25		ns
t_{F5-20}	0.65		0.75		0.86		ns
t_{F20+}	1.11		1.27		1.46		ns

Table 59. EP2A25 Minimum Pulse Width Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{CH}	1.00		1.50		2.12		ns
t_{CL}	1.00		1.50		2.12		ns
t_{CLRP}	0.13		0.15		0.17		ns
t_{PREP}	0.13		0.15		0.17		ns
t_{ESBCH}	1.00		1.50		2.12		ns
t_{ESBCL}	1.00		1.50		2.12		ns
t_{ESBWP}	1.12		1.28		1.48		ns
t_{ESBRP}	0.88		1.02		1.17		ns

Table 60. EP2A40 f_{MAX} LE Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.22		0.26		0.29		ns
t_{H}	0.22		0.26		0.29		ns
t_{CO}		0.16		0.18		0.21	ns
t_{LUT}		0.48		0.55		0.63	ns

Table 61. EP2A40 f_{MAX} ESB Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		2.28		2.62		3.01	ns
t_{ESBSRC}		2.23		2.56		2.95	ns
t_{ESBAWC}		3.13		3.60		4.13	ns
t_{ESBSWC}		2.76		3.18		3.65	ns
$t_{ESBWASU}$	1.19		1.37		1.57		ns
t_{ESBWAH}	0.00		0.00		0.00		ns
$t_{ESBWDSU}$	1.44		1.66		1.91		ns
t_{ESBWDH}	0.00		0.00		0.00		ns
$t_{ESBRASU}$	1.88		2.17		2.49		ns
t_{ESBRAH}	0.00		0.00		0.00		ns
$t_{ESBWESU}$	1.60		1.85		2.12		ns
$t_{ESBDATASU}$	0.74		0.85		0.98		ns
$t_{ESBWADDRSU}$	0.82		0.94		1.08		ns
$t_{ESBRADDRSU}$	0.73		0.84		.97		ns
$t_{ESBDATACO1}$		1.09		1.25		1.44	ns
$t_{ESBDATACO2}$		1.73		1.99		2.29	ns
t_{ESBDD}		3.26		3.75		4.32	ns
t_{PD}		1.55		1.78		2.05	ns
$t_{PTERMSU}$	0.99		1.13		1.30		ns
$t_{PTERMCO}$		0.79		0.90		1.04	ns

Table 62. EP2A40 f_{MAX} Routing Delays

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}	0.17		0.19		0.22		ns
t_{F5-20}	1.12		1.28		1.48		ns
t_{F20+}	1.49		1.72		1.98		ns

Table 63. EP2A40 Minimum Pulse Width Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{CH}	0.89		1.33		1.88		ns
t_{CL}	0.89		1.33		1.88		ns
t_{CLRP}	0.12		0.14		0.16		ns
t_{PREP}	0.12		0.14		0.16		ns
t_{ESBCH}	0.89		1.33		1.88		ns
t_{ESBCL}	0.89		1.33		1.88		ns
t_{ESBWP}	1.05		1.20		1.38		ns
t_{ESBRP}	0.78		0.90		1.03		ns

Table 64. EP2A70 f_{MAX} LE Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.30		0.34		0.39		ns
t_{H}	0.30		0.34		0.39		ns
t_{CO}		0.22		0.25		0.29	ns
t_{LUT}		0.66		0.76		0.87	ns

Table 65. EP2A70 f_{MAX} ESB Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		3.12		3.58		4.12	ns
t_{ESBSRC}		3.11		3.58		4.11	ns
t_{ESBAWC}		4.41		5.07		5.83	ns
t_{ESBSWC}		3.82		4.39		5.05	ns
$t_{ESBWASU}$	1.73		1.99		2.28		ns
t_{ESBWAH}	0.00		0.00		0.00		ns
$t_{ESBWDSU}$	1.87		2.15		2.47		ns
t_{ESBWDH}	0.00		0.00		0.00		ns
$t_{ESBRASU}$	2.76		3.17		3.65		ns
t_{ESBRAH}	0.00		0.00		0.00		ns
$t_{ESBWESU}$	1.98		2.27		2.61		ns
$t_{ESBDATASU}$	1.06		1.22		1.40		ns
$t_{ESBWADDRSU}$	1.17		1.34		1.54		ns
$t_{ESBRADDRSU}$	1.02		1.17		1.35		ns
$t_{ESBDATACO1}$		1.52		1.75		2.01	ns
$t_{ESBDATACO2}$		2.35		2.71		3.11	ns
t_{ESBDD}		4.43		5.10		5.87	ns
t_{PD}		2.17		2.49		2.87	ns
$t_{PTERMSU}$	1.40		1.62		1.86		ns
$t_{PTERMCO}$		1.08		1.24		1.42	ns

Table 66. EP2A70 f_{MAX} Routing Delays

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}	0.15		0.18		0.20		ns
t_{F5-20}	1.21		1.39		1.60		ns
t_{F20+}	1.87		2.15		2.55		ns

Table 67. EP2A70 Minimum Pulse Width Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{CH}	1.19		1.78		2.53		ns
t_{CL}	1.19		1.78		2.53		ns
t_{CLRP}	0.16		0.19		0.21		ns
t_{PREP}	0.16		0.19		0.21		ns
t_{ESBCH}	1.19		1.78		2.53		ns
t_{ESBCL}	1.19		1.78		2.53		ns
t_{ESBWP}	1.35		1.56		1.79		ns
t_{ESBRP}	1.13		1.30		1.50		ns

Tables 68 through 77 show the IOE external timing parameter values for APEX II devices.

Table 68. EP2A15 External Timing Parameters for Row I/O Pins

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.06		2.25		2.46		ns
t_{INH}	0.00		0.00		0.00		ns
t_{OUTCO}	2.00	4.05	2.00	4.45	2.00	4.90	ns
t_{XZ}		4.98		5.59		6.26	ns
t_{ZX}		4.98		5.59		6.26	ns
$t_{INSUPLL}$	1.15		1.28		1.42		ns
t_{INHPLL}	0.00		0.00		0.00		ns
$t_{OUTCOPLL}$	0.50	2.60	0.50	2.87	0.50	3.16	ns
t_{XZPLL}		3.53		4.00		4.52	ns
t_{ZXPLL}		3.53		4.00		4.52	ns

Table 69. EP2A15 External Timing Parameters for Column I/O Pins

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.16		2.34		2.53		ns
t_{INH}	0.00		0.00		0.00		ns
t_{OUTCO}	2.00	4.36	2.00	4.75	2.00	5.18	ns
t_{XZ}		5.57		6.24		6.97	ns
t_{ZX}		5.57		6.24		6.97	ns
$t_{INSUPLL}$	1.24		1.37		1.52		ns
t_{INHPLL}	0.00		0.00		0.00		ns
$t_{OUTCOPLL}$	0.50	2.90	0.50	3.16	0.50	3.45	ns
t_{XZPLL}		4.12		4.65		5.23	ns
t_{ZXPLL}		4.12		4.65		5.23	ns

Table 70. EP2A25 External Timing Parameters for Row I/O Pins

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	1.92		2.08		2.26		ns
t_{INH}	0.00		0.00		0.00		ns
t_{OUTCO}	2.00	4.29	2.00	4.62	2.00	4.98	ns
t_{XZ}		5.24		5.73		6.26	ns
t_{ZX}		5.24		5.73		6.26	ns
$t_{INSUPLL}$	1.17		1.27		1.40		ns
t_{INHPLL}	0.00		0.00		0.00		ns
$t_{OUTCOPLL}$	0.50	2.61	0.50	2.83	0.50	3.07	ns
t_{XZPLL}		3.55		3.93		4.35	ns
t_{ZXPLL}		3.55		3.93		4.35	ns

Table 71. EP2A25 External Timing Parameters for Column I/O Pins

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.27		2.45		2.64		ns
t_{INH}	0.00		0.00		0.00		ns
t_{OUTCO}	2.00	4.57	2.00	4.89	2.00	5.24	ns
t_{XZ}		5.87		6.42		7.01	ns
t_{ZX}		5.87		6.42		7.01	ns
$t_{INSUPLL}$	1.23		1.35		1.47		ns
t_{INHPLL}	0.00		0.00		0.00		ns
$t_{OUTCOPLL}$	0.50	2.89	0.50	3.10	0.50	3.33	ns
t_{XZPLL}		4.18		4.62		5.09	ns
t_{ZXPLL}		4.18		4.62		5.09	ns

Table 72. EP2A40 External Timing Parameters for Row I/O Pins

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	1.57		1.72		1.88		ns
t_{INH}	0.00		0.00		0.00		ns
t_{OUTCO}	2.00	4.90	2.00	5.24	2.00	5.61	ns
t_{XZ}		6.47		6.98		7.53	ns
t_{ZX}		6.47		6.98		7.53	ns
$t_{INSUPLL}$	1.15		1.26		1.38		ns
t_{INHPLL}	0.00		0.00		0.00		ns
$t_{OUTCOPLL}$	0.50	2.60	0.50	2.82	0.50	3.06	ns
t_{XZPLL}		4.17		4.56		4.97	ns
t_{ZXPLL}		4.17		4.56		4.97	ns

Table 73. EP2A40 External Timing Parameters for Column I/O Pins

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.00		2.16		2.33		ns
t_{INH}	0.00		0.00		0.00		ns
t_{OUTCO}	2.00	4.96	2.00	5.29	2.00	5.64	ns
t_{XZ}		7.04		7.59		8.19	ns
t_{ZX}		7.04		7.59		8.19	ns
$t_{INSUPLL}$	1.20		1.31		1.43		ns
t_{INHPLL}	0.00		0.00		0.00		ns
$t_{OUTCOPLL}$	0.50	2.66	0.50	2.87	0.50	3.09	ns
t_{XZPLL}		4.74		5.17		5.64	ns
t_{ZXPLL}		4.74		5.17		5.64	ns

Table 74. EP2A70 External Timing Parameters for Row I/O Pins

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.48		2.68		2.90		ns
t_{INH}	0.00		0.00		0.00		ns
t_{OUTCO}	2.00	4.76	2.00	5.12	2.00	5.51	ns
t_{XZ}		5.68		6.19		6.76	ns
t_{ZX}		5.68		6.19		6.76	ns
$t_{INSUPLL}$	1.19		1.30		1.43		ns
t_{INHPLL}	0.00		0.00		0.00		ns
$t_{OUTCOPLL}$	0.50	2.52	0.50	2.74	0.50	2.98	ns
t_{XZPLL}		3.44		3.82		4.23	ns
t_{ZXPLL}		3.44		3.82		4.23	ns

Table 75. EP2A70 External Timing Parameters for Column I/O Pins

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.79		2.99		3.22		ns
t_{INH}	0.00		0.00		0.00		ns
t_{OUTCO}	2.00	4.91	2.00	5.24	2.00	5.60	ns
t_{XZ}		6.16		6.71		7.32	ns
t_{ZX}		6.16		6.71		7.32	ns
$t_{INSUPLL}$	1.19		1.30		1.43		ns
t_{INHPLL}	0.00		0.00		0.00		ns
$t_{OUTCOPLL}$	0.50	2.67	0.50	2.86	0.50	3.08	ns
t_{XZPLL}		3.92		4.34		4.79	ns
t_{ZXPLL}		3.92		4.34		4.79	ns

Table 76. APEX II Selectable I/O Standards Input Adder Delays

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
LVCMOS		0.00		0.00		0.00	ns
LVTTL		0.00		0.00		0.00	ns
1.5 V		0.10		0.11		0.12	ns
1.8 V		0.00		0.00		0.00	ns
2.5 V		0.00		0.00		0.00	ns
3.3-V PCI		0.00		0.00		0.00	ns
3.3-V PCI-X		0.00		0.00		0.00	ns
GTL+		– 0.20		– 0.22		– 0.24	ns
SSTL-3 Class I		– 0.17		– 0.19		– 0.20	ns
SSTL-3 Class II		– 0.17		– 0.19		– 0.20	ns
SSTL-2 Class I		– 0.24		– 0.26		– 0.29	ns
SSTL-2 Class II		– 0.24		– 0.26		– 0.29	ns
HSTL Class I		– 0.03		– 0.03		– 0.03	ns
HSTL Class II		– 0.03		– 0.03		– 0.03	ns
LVDS		– 0.23		– 0.26		– 0.28	ns
LVPECL		– 0.23		– 0.26		– 0.28	ns
PCML		– 0.23		– 0.26		– 0.28	ns
CTT		0.00		0.00		0.00	ns
3.3-V AGP 1×		0.00		0.00		0.00	ns
3.3-V AGP 2×		0.00		0.00		0.00	ns
HyperTransport		– 0.23		– 0.26		– 0.28	ns
Differential HSTL		– 0.23		– 0.26		– 0.28	ns

Table 77. APEX II Selectable I/O Standards Output Adder Delays

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
LVCMOS		0.00		0.00		0.00	ns
LVTTL		0.00		0.00		0.00	ns
1.5 V		3.32		3.82		4.20	ns
1.8 V		2.65		3.05		3.36	ns
2.5 V		1.20		1.38		1.52	ns
3.3-V PCI		– 0.68		– 0.78		– 0.85	ns
3.3-V PCI-X		– 0.68		– 0.78		– 0.85	ns
GTL+		– 0.45		– 0.52		– 0.57	ns
SSTL-3 Class I		– 0.52		– 0.60		– 0.66	ns
SSTL-3 Class II		– 0.52		– 0.60		– 0.66	ns
SSTL-2 Class I		– 0.68		– 0.78		– 0.86	ns
SSTL-2 Class II		– 0.81		– 0.93		– 1.02	ns
HSTL Class I		– 0.08		– 0.09		– 0.10	ns
HSTL Class II		– 0.23		– 0.27		– 0.30	ns
LVDS		– 1.41		– 1.62		– 1.79	ns
LVPECL		– 1.38		– 1.58		– 1.74	ns
PCML		– 1.30		– 1.50		– 1.65	ns
CTT		0.00		0.00		0.00	ns
3.3-V AGP 1×		0.00		0.00		0.00	ns
3.3-V AGP 2×		0.00		0.00		0.00	ns
HyperTransport		– 1.22		– 1.41		– 1.55	ns
Differential HSTL		– 1.41		– 1.62		– 1.79	ns

Power Consumption

Detailed power consumption information for APEX II devices will be released via a future interactive power estimator on the Altera web site.

Device Pin-Outs

See the Altera web site (**http://www.altera.com**) or the ***Altera Digital Library*** for pin-out information.

Revision History

The information contained in the *APEX II Programmable Logic Device Family Data Sheet* version 3.0 supersedes information published in previous versions. The following changes were made to the *APEX II Programmable Logic Device Family Data Sheet* version 3.0:

- Changed the value from 624 to 400 Mbps throughout the document.
- Deleted the pin count (612) for the EP2A25 device in the 1,020-pin FineLine BGA package (see Table 3).
- Added Table 13.
- Changed the maximum value of 3.6 to 2.4 in Table 20.
- Updated Tables 60 through 67 and Tables 72 through 75.
- Updated Figures 25, 28, and 30.
- Added *Note (1)* to Figure 13.
- Added Figure 43.

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