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1. Device Datasheet for Arria II Devices

AIIGX53001-4.4

This chapter describes the electrical and switching characteristics of the Arria® II device family. The Arria II device family includes the Arria II GX and GZ devices. Electrical characteristics include operating conditions and power consumption. Switching characteristics include transceiver specifications, core, and periphery performance. This chapter also describes I/O timing, including programmable I/O element (IOE) delay and programmable output buffer delay.

 For information regarding the densities and packages of devices in the Arria II device family, refer to *Overview for the Arria II Device Family* chapter.

This chapter contains the following sections:

- “Electrical Characteristics” on page 1–1
- “Transceiver Performance Specifications” on page 1–21
- “Glossary” on page 1–74


Electrical Characteristics

The following sections describe the electrical characteristics.

Operating Conditions

Arria II devices are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of Arria II devices, you must consider the operating requirements described in this chapter.

Arria II devices are offered in both commercial and industrial grades. Arria II GX devices are offered in –4 (fastest), –5, and –6 (slowest) commercial speed grades and –3 and –5 industrial speed grades. Arria II GZ devices are offered in –3 and –4 speed grades for both commercial and industrial grades.

 In this chapter, a prefix associated with the operating temperature range is attached to the speed grades; commercial with the “C” prefix and industrial with the “I” prefix. Commercial devices are indicated as C4, C5, and C6 speed grade, and the industrial devices are indicated as I3 and I5.

Absolute Maximum Ratings

Absolute maximum ratings define the maximum operating conditions for Arria II devices. The values are based on experiments conducted with the device and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied under these conditions. [Table 1–1](#) lists the absolute maximum ratings for Arria II GX devices. [Table 1–2](#) lists the absolute maximum ratings for Arria II GZ devices.

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Conditions beyond those listed in [Table 1-1](#) and [Table 1-2](#) may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

[Table 1-1](#) lists the absolute maximum ratings for Arria II GX devices.

Table 1-1. Absolute Maximum Ratings for Arria II GX Devices

| Symbol | Description | Minimum | Maximum | Unit |
|----------------|---|---------|---------|------|
| V_{CC} | Supplies power to the core, periphery, I/O registers, PCI Express® (PIPE) (PCIe) HIP block, and transceiver PCS | -0.5 | 1.35 | V |
| V_{CCCB} | Supplies power for the configuration RAM bits | -0.5 | 1.8 | V |
| V_{CCBAT} | Battery back-up power supply for design security volatile key register | -0.5 | 3.75 | V |
| V_{CCPD} | Supplies power to the I/O pre-drivers, differential input buffers, and MSEL circuitry | -0.5 | 3.75 | V |
| V_{CCIO} | Supplies power to the I/O banks | -0.5 | 3.9 | V |
| V_{CCD_PLL} | Supplies power to the digital portions of the PLL | -0.5 | 1.35 | V |
| V_{CCA_PLL} | Supplies power to the analog portions of the PLL and device-wide power management circuitry | -0.5 | 3.75 | V |
| V_I | DC input voltage | -0.5 | 4.0 | V |
| I_{OUT} | DC output current, per pin | -25 | 40 | mA |
| V_{CCA} | Supplies power to the transceiver PMA regulator | — | 3.75 | V |
| V_{CCL_GXB} | Supplies power to the transceiver PMA TX, PMA RX, and clocking | — | 1.21 | V |
| V_{CCH_GXB} | Supplies power to the transceiver PMA output (TX) buffer | — | 1.8 | V |
| T_J | Operating junction temperature | -55 | 125 | °C |
| T_{STG} | Storage temperature (no bias) | -65 | 150 | °C |

[Table 1-2](#) lists the absolute maximum ratings for Arria II GZ devices.

Table 1-2. Absolute Maximum Ratings for Arria II GZ Devices (Part 1 of 2)

| Symbol | Description | Minimum | Maximum | Unit |
|-----------------|---|---------|---------|------|
| V_{CC} | Supplies power to the core, periphery, I/O registers, PCIe HIP block, and transceiver PCS | -0.5 | 1.35 | V |
| V_{CCCB} | Power supply to the configuration RAM bits | -0.5 | 1.8 | V |
| V_{CCPGM} | Supplies power to the configuration pins | -0.5 | 3.75 | V |
| V_{CCAUX} | Auxiliary supply | -0.5 | 3.75 | V |
| V_{CCBAT} | Supplies battery back-up power for design security volatile key register | -0.5 | 3.75 | V |
| V_{CCPD} | Supplies power to the I/O pre-drivers, differential input buffers, and MSEL circuitry | -0.5 | 3.75 | V |
| V_{CCIO} | Supplies power to the I/O banks | -0.5 | 3.9 | V |
| V_{CC_CLKIN} | Supplies power to the differential clock input | -0.5 | 3.75 | V |
| V_{CCD_PLL} | Supplies power to the digital portions of the PLL | -0.5 | 1.35 | V |
| V_{CCA_PLL} | Supplies power to the analog portions of the PLL and device-wide power management circuitry | -0.5 | 3.75 | V |
| V_I | DC input voltage | -0.5 | 4.0 | V |
| I_{OUT} | DC output current, per pin | -25 | 40 | mA |

Table 1–2. Absolute Maximum Ratings for Arria II GZ Devices (Part 2 of 2)

| Symbol | Description | Minimum | Maximum | Unit |
|-------------------------------|---|---------|---------|------|
| V _{CCA_L} | Supplies transceiver high voltage power (left side) | -0.5 | 3.75 | V |
| V _{CCA_R} | Supplies transceiver high voltage power (right side) | -0.5 | 3.75 | V |
| V _{CCHIP_L} | Supplies transceiver HIP digital power (left side) | -0.5 | 1.35 | V |
| V _{CCR_L} | Supplies receiver power (left side) | -0.5 | 1.35 | V |
| V _{CCR_R} | Supplies receiver power (right side) | -0.5 | 1.35 | V |
| V _{CCT_L} | Supplies transmitter power (left side) | -0.5 | 1.35 | V |
| V _{CCT_R} | Supplies transmitter power (right side) | -0.5 | 1.35 | V |
| V _{CCL_GXBLn} (1) | Supplies power to the transceiver PMA TX, PMA RX, and clocking (left side) | -0.5 | 1.35 | V |
| V _{CCL_GXBRn} (1) | Supplies power to the transceiver PMA TX, PMA RX, and clocking (right side) | -0.5 | 1.35 | V |
| V _{CCH_GXBLn} (1) | Supplies power to the transceiver PMA output (TX) buffer (left side) | -0.5 | 1.8 | V |
| V _{CCH_GXBRn} (1) | Supplies power to the transceiver PMA output (TX) buffer (right side) | -0.5 | 1.8 | V |
| T _J | Operating junction temperature | -55 | 125 | °C |
| T _{STG} | Storage temperature (no bias) | -65 | 150 | °C |

Note to Table 1–2:

(1) n = 0, 1, or 2.

Maximum Allowed Overshoot and Undershoot Voltage

During transitions, input signals may overshoot to the voltage shown in [Table 1–3](#) and undershoot to –2.0 V for magnitude of currents less than 100 mA and periods shorter than 20 ns.

[Table 1–3](#) lists the Arria II GX and GZ maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage over the device lifetime. The maximum allowed overshoot duration is specified as a percentage of high-time over the lifetime of the device. A DC signal is equivalent to 100% duty cycle. For example, a signal that overshoots to 4.3 V can only be at 4.3 V for 5.41% over the lifetime of the device; for a device lifetime of 10 years, this amounts to 5.41/10ths of a year.

Table 1-3. Maximum Allowed Overshoot During Transitions for Arria II Devices

| Symbol | Description | Condition (V) | Overshoot Duration as % of High Time | Unit |
|---------------------|------------------|---------------|--------------------------------------|------|
| V _I (AC) | AC Input Voltage | 4.0 | 100.000 | % |
| | | 4.05 | 79.330 | % |
| | | 4.1 | 46.270 | % |
| | | 4.15 | 27.030 | % |
| | | 4.2 | 15.800 | % |
| | | 4.25 | 9.240 | % |
| | | 4.3 | 5.410 | % |
| | | 4.35 | 3.160 | % |
| | | 4.4 | 1.850 | % |
| | | 4.45 | 1.080 | % |
| | | 4.5 | 0.630 | % |
| | | 4.55 | 0.370 | % |
| | | 4.6 | 0.220 | % |

Maximum Allowed I/O Operating Frequency

Table 1-4 lists the maximum allowed I/O operating frequency for Arria II GX I/Os using the specified I/O standards to ensure device reliability.

Table 1-4. Maximum Allowed I/O Operating Frequency for Arria II GX Devices

| I/O Standard | I/O Frequency (MHz) |
|---------------------------------------|---------------------|
| HSTL-18 and HSTL-15 | 333 |
| SSTL -15 | 400 |
| SSTL-18 | 333 |
| 2.5-V LVCMOS | 260 |
| 3.3-V and 3.0-V LVTTTL | 250 |
| 3.3-V, 3.0-V, 1.8-V, and 1.5-V LVCMOS | |
| PCI and PCI-X | |
| SSTL-2 | |
| 1.2-V LVCMOS HSTL-12 | 200 |

Recommended Operating Conditions

This section lists the functional operation limits for AC and DC parameters for Arria II GX and GZ devices. All supplies are required to monotonically reach their full-rail values without plateaus within t_{RAMP} .

Table 1–5 lists the recommended operating conditions for Arria II GX devices.

Table 1–5. Recommended Operating Conditions for Arria II GX Devices (Note 1) (Part 1 of 2)

| Symbol | Description | Condition | Minimum | Typical | Maximum | Unit |
|--------------------|---|------------|---------|---------|------------|------|
| V_{CC} | Supplies power to the core, periphery, I/O registers, PCIe HIP block, and transceiver PCS | — | 0.87 | 0.90 | 0.93 | V |
| V_{CCCB} | Supplies power to the configuration RAM bits | — | 1.425 | 1.50 | 1.575 | V |
| V_{CCBAT} (2) | Battery back-up power supply for design security volatile key registers | — | 1.2 | — | 3.3 | V |
| V_{CCPD} (3) | Supplies power to the I/O pre-drivers, differential input buffers, and MSEL circuitry | — | 3.135 | 3.3 | 3.465 | V |
| | | — | 2.85 | 3.0 | 3.15 | V |
| | | — | 2.375 | 2.5 | 2.625 | V |
| V_{CCIO} | Supplies power to the I/O banks (4) | — | 3.135 | 3.3 | 3.465 | V |
| | | — | 2.85 | 3.0 | 3.15 | V |
| | | — | 2.375 | 2.5 | 2.625 | V |
| | | — | 1.71 | 1.8 | 1.89 | V |
| | | — | 1.425 | 1.5 | 1.575 | V |
| | | — | 1.14 | 1.2 | 1.26 | V |
| V_{CCD_PLL} | Supplies power to the digital portions of the PLL | — | 0.87 | 0.90 | 0.93 | V |
| V_{CCA_PLL} | Supplies power to the analog portions of the PLL and device-wide power management circuitry | — | 2.375 | 2.5 | 2.625 | V |
| V_I | DC Input voltage | — | -0.5 | — | 3.6 | V |
| V_O | Output voltage | — | 0 | — | V_{CCIO} | V |
| V_{CCA} | Supplies power to the transceiver PMA regulator | — | 2.375 | 2.5 | 2.625 | V |
| V_{CCL_GXB} | Supplies power to the transceiver PMA TX, PMA RX, and clocking | — | 1.045 | 1.1 | 1.155 | V |
| V_{CCH_GXB} | Supplies power to the transceiver PMA output (TX) buffer | — | 1.425 | 1.5 | 1.575 | V |
| T_J | Operating junction temperature | Commercial | 0 | — | 85 | °C |
| | | Industrial | -40 | — | 100 | °C |

Table 1-5. Recommended Operating Conditions for Arria II GX Devices (Note 1) (Part 2 of 2)

| Symbol | Description | Condition | Minimum | Typical | Maximum | Unit |
|-------------------|------------------------|------------|---------|---------|---------|------|
| t_{RAMP} | Power Supply Ramp time | Normal POR | 0.05 | — | 100 | ms |
| | | Fast POR | 0.05 | — | 4 | ms |

Notes to Table 1-5:

- (1) For more information about supply pin connections, refer to the *Arria II Device Family Pin Connection Guidelines*.
- (2) Altera recommends a 3.0-V nominal battery voltage when connecting V_{CCBAT} to a battery for volatile key backup. If you do not use the volatile security key, you may connect the V_{CCBAT} to either GND or a 3.0-V power supply.
- (3) V_{CCPD} must be 2.5-V for I/O banks with 2.5-V and lower V_{CCIO} , 3.0-V for 3.0-V V_{CCIO} , and 3.3-V for 3.3-V V_{CCIO} .
- (4) V_{CCIO} for 3C and 8C I/O banks where the configuration pins reside only supports 3.3-, 3.0-, 2.5-, or 1.8-V voltage levels.

Table 1-6 lists the recommended operating conditions for Arria II GZ devices.

Table 1-6. Recommended Operating Conditions for Arria II GZ Devices (Note 6) (Part 1 of 2)

| Symbol | Description | Condition | Minimum | Typical | Maximum | Unit |
|------------------------|--|-----------|------------|-------------|-------------------|------|
| V_{CC} | Core voltage and periphery circuitry power supply | — | 0.87 | 0.90 | 0.93 | V |
| V_{CCCB} | Supplies power for the configuration RAM bits | — | 1.45 | 1.50 | 1.55 | V |
| V_{CCAUX} | Auxiliary supply | — | 2.375 | 2.5 | 2.625 | V |
| V_{CCPD} (2) | I/O pre-driver (3.0 V) power supply | — | 2.85 | 3.0 | 3.15 | V |
| | I/O pre-driver (2.5 V) power supply | — | 2.375 | 2.5 | 2.625 | V |
| V_{CCIO} | I/O buffers (3.0 V) power supply | — | 2.85 | 3.0 | 3.15 | V |
| | I/O buffers (2.5 V) power supply | — | 2.375 | 2.5 | 2.625 | V |
| | I/O buffers (1.8 V) power supply | — | 1.71 | 1.8 | 1.89 | V |
| | I/O buffers (1.5 V) power supply | — | 1.425 | 1.5 | 1.575 | V |
| | I/O buffers (1.2 V) power supply | — | 1.14 | 1.2 | 1.26 | V |
| V_{CCPGM} | Configuration pins (3.0 V) power supply | — | 2.85 | 3.0 | 3.15 | V |
| | Configuration pins (2.5 V) power supply | — | 2.375 | 2.5 | 2.625 | V |
| | Configuration pins (1.8 V) power supply | — | 1.71 | 1.8 | 1.89 | V |
| $V_{\text{CCA_PLL}}$ | PLL analog voltage regulator power supply | — | 2.375 | 2.5 | 2.625 | V |
| $V_{\text{CCD_PLL}}$ | PLL digital voltage regulator power supply | — | 0.87 | 0.90 | 0.93 | V |
| $V_{\text{CC_CLKIN}}$ | Differential clock input power supply | — | 2.375 | 2.5 | 2.625 | V |
| V_{CCBAT} (1) | Battery back-up power supply (For design security volatile key register) | — | 1.2 | — | 3.3 | V |
| V_{I} | DC input voltage | — | -0.5 | — | 3.6 | V |
| V_{O} | Output voltage | — | 0 | — | V_{CCIO} | V |
| $V_{\text{CCA_L}}$ | Transceiver high voltage power (left side) | — | 2.85/2.375 | 3.0/2.5 (4) | 3.15/2.625 | V |
| $V_{\text{CCA_R}}$ | Transceiver high voltage power (right side) | | | | | |
| $V_{\text{CCHIP_L}}$ | Transceiver HIP digital power (left side) | — | 0.87 | 0.9 | 0.93 | V |
| $V_{\text{CCR_L}}$ | Receiver power (left side) | — | 1.05 | 1.1 | 1.15 | V |
| $V_{\text{CCR_R}}$ | Receiver power (right side) | — | 1.05 | 1.1 | 1.15 | V |
| $V_{\text{CCT_L}}$ | Transmitter power (left side) | — | 1.05 | 1.1 | 1.15 | V |
| $V_{\text{CCT_R}}$ | Transmitter power (right side) | — | 1.05 | 1.1 | 1.15 | V |

Table 1-6. Recommended Operating Conditions for Arria II GZ Devices (Note 6) (Part 2 of 2)

| Symbol | Description | Condition | Minimum | Typical | Maximum | Unit |
|-------------------------|--|-----------------------|------------|-------------|---------|------|
| V_{CCL_GXBLn} (3) | Transceiver clock power (left side) | — | 1.05 | 1.1 | 1.15 | V |
| V_{CCL_GXBRn} (3) | Transceiver clock power (right side) | — | 1.05 | 1.1 | 1.15 | V |
| V_{CCH_GXBLn} (3) | Transmitter output buffer power (left side) | — | 1.33/1.425 | 1.4/1.5 (5) | 1.575 | V |
| V_{CCH_GXBRn} (3) | Transmitter output buffer power (right side) | — | | | | |
| T_J | Operating junction temperature | Commercial | 0 | — | 85 | °C |
| | | Industrial | -40 | — | 100 | °C |
| t_{RAMP} | Power supply ramp time | Normal POR (PORSEL=0) | 0.05 | — | 100 | ms |
| | | Fast POR (PORSEL=1) | 0.05 | — | 4 | ms |

Notes to Table 1-6:

- (1) Altera recommends a 3.0-V nominal battery voltage when connecting V_{CCBAT} to a battery for volatile key backup. If you do not use the volatile security key, you may connect the V_{CCBAT} to either GND or a 3.0-V power supply.
- (2) V_{CCPD} must be 2.5 V when V_{CCIO} is 2.5, 1.8, 1.5, or 1.2 V. V_{CCPD} must be 3.0 V when V_{CCIO} is 3.0 V.
- (3) $n = 0, 1, \text{ or } 2$.
- (4) $V_{CCA_L/R}$ must be connected to a 3.0-V supply if the clock multiplier unit (CMU) phase-locked loop (PLL), receiver clock data recovery (CDR), or both, are configured at a base data rate > 4.25 Gbps. For data rates up to 4.25 Gbps, you can connect $V_{CCA_L/R}$ to either 3.0 V or 2.5 V.
- (5) $V_{CCH_GXBL/R}$ must be connected to a 1.4-V supply if the transmitter channel data rate is > 6.5 Gbps. For data rates up to 6.5 Gbps, you can connect $V_{CCH_GXBL/R}$ to either 1.4 V or 1.5 V.
- (6) Transceiver power supplies do not have power-on-reset (POR) circuitry. After initial power-up, violating the transceiver power supply operating conditions could lead to unpredictable link behavior.

DC Characteristics

This section lists the supply current, I/O pin leakage current, on-chip termination (OCT) accuracy and variation, input pin capacitance, internal weak pull-up and pull-down resistance, hot socketing, and Schmitt trigger input specifications.

Supply Current

Standby current is the current the device draws after the device is configured with no inputs or outputs toggling and no activity in the device. Because these currents vary largely with the resources used, use the Microsoft Excel-based Early Power Estimator (EPE) to get supply current estimates for your design.



For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter.

I/O Pin Leakage Current

Table 1-7 lists the Arria II GX I/O pin leakage current specifications.

Table 1-7. I/O Pin Leakage Current for Arria II GX Devices

| Symbol | Description | Conditions | Min | Typ | Max | Unit |
|----------|--------------------|--|-----|-----|-----|---------------|
| I_I | Input pin | $V_I = 0\text{ V to }V_{CCIO\text{MAX}}$ | -10 | — | 10 | μA |
| I_{OZ} | Tri-stated I/O pin | $V_O = 0\text{ V to }V_{CCIO\text{MAX}}$ | -10 | — | 10 | μA |

Table 1-8 lists the Arria II GZ I/O pin leakage current specifications.

Table 1-8. I/O Pin Leakage Current for Arria II GZ Devices

| Symbol | Description | Conditions | Min | Typ | Max | Unit |
|----------|--------------------|--|-----|-----|-----|---------------|
| I_I | Input pin | $V_I = 0\text{ V to }V_{CCIO\text{MAX}}$ | -20 | — | 20 | μA |
| I_{OZ} | Tri-stated I/O pin | $V_O = 0\text{ V to }V_{CCIO\text{MAX}}$ | -20 | — | 20 | μA |

Bus Hold

Bus hold retains the last valid logic state after the source driving it either enters the high impedance state or is removed. Each I/O pin has an option to enable bus hold in user mode. Bus hold is always disabled in configuration mode.

Table 1-9 lists bus hold specifications for Arria II GX devices.

Table 1-9. Bus Hold Parameters for Arria II GX Devices (Note 1)

| Parameter | Symbol | Cond. | $V_{CCIO}\text{ (V)}$ | | | | | | | | | | | | Unit |
|-----------------------------------|------------|----------------------------------|-----------------------|------|-------|-------|------|------|-----|------|-----|------|-----|------|---------------|
| | | | 1.2 | | 1.5 | | 1.8 | | 2.5 | | 3.0 | | 3.3 | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| Bus-hold low, sustaining current | I_{SUSL} | $V_{IN} > V_{IL}$ (max.) | 8 | — | 12 | — | 30 | — | 50 | — | 70 | — | 70 | — | μA |
| Bus-hold high, sustaining current | I_{SUSH} | $V_{IN} < V_{IL}$ (min.) | -8 | — | -12 | — | -30 | — | -50 | — | -70 | — | -70 | — | μA |
| Bus-hold low, overdrive current | I_{ODL} | $0\text{ V} < V_{IN} < V_{CCIO}$ | — | 125 | — | 175 | — | 200 | — | 300 | — | 500 | — | 500 | μA |
| Bus-hold high, overdrive current | I_{ODH} | $0\text{ V} < V_{IN} < V_{CCIO}$ | — | -125 | — | -175 | — | -200 | — | -300 | — | -500 | — | -500 | μA |
| Bus-hold trip point | V_{TRIP} | — | 0.3 | 0.9 | 0.375 | 1.125 | 0.68 | 1.07 | 0.7 | 1.7 | 0.8 | 2 | 0.8 | 2 | V |

Note to Table 1-9:

(1) The bus-hold trip points are based on calculated input voltages from the JEDEC standard.

Table 1-10 lists the bus hold specifications for Arria II GZ devices.

Table 1-10. Bus Hold Parameters for Arria II GZ Devices

| Parameter | Symbol | Cond. | V_{CCIO} (V) | | | | | | | | | | Unit |
|----------------------------------|------------|-----------------------------|----------------|------|-------|------|-------|------|-------|------|-------|------|---------|
| | | | 1.2 | | 1.5 | | 1.8 | | 2.5 | | 3.0 | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| Bus-hold Low sustaining current | I_{SUSL} | $V_{IN} > V_{IL}$ (max.) | 22.5 | — | 25.0 | — | 30.0 | — | 50.0 | — | 70.0 | — | μ A |
| Bus-hold High sustaining current | I_{SUSH} | $V_{IN} < V_{IH}$ (min.) | -22.5 | — | -25.0 | — | -30.0 | — | -50.0 | — | -70.0 | — | μ A |
| Bus-hold Low overdrive current | I_{ODL} | $0V < V_{IN} < V_{CCIO}$ | — | 120 | — | 160 | — | 200 | — | 300 | — | 500 | μ A |
| Bus-hold High overdrive current | I_{ODH} | $0V < V_{IN} < V_{CCIO}$ | — | -120 | — | -160 | — | -200 | — | -300 | — | -500 | μ A |
| Bus-hold trip point | V_{TRIP} | — | 0.45 | 0.95 | 0.50 | 1.00 | 0.68 | 1.07 | 0.70 | 1.70 | 0.80 | 2.00 | V |

OCT Specifications

Table 1-11 lists the Arria II GX device and differential OCT with and without calibration accuracy.

Table 1-11. OCT With and Without Calibration Specification for Arria II GX Device I/Os (Note 1) (Part 1 of 2)

| Symbol | Description | Conditions (V) | Calibration Accuracy | | Unit |
|---|---|--------------------------------------|----------------------|------------|------|
| | | | Commercial | Industrial | |
| 25- Ω R_S 3.0, 2.5 | 25- Ω series OCT without calibration | $V_{CCIO} = 3.0, 2.5$ | ± 30 | ± 40 | % |
| 50- Ω R_S 3.0, 2.5 | 50- Ω series OCT without calibration | $V_{CCIO} = 3.0, 2.5$ | ± 30 | ± 40 | % |
| 25- Ω R_S 1.8 | 25- Ω series OCT without calibration | $V_{CCIO} = 1.8$ | ± 40 | ± 50 | % |
| 50- Ω R_S 1.8 | 50- Ω series OCT without calibration | $V_{CCIO} = 1.8$ | ± 40 | ± 50 | % |
| 25- Ω R_S 1.5, 1.2 | 25- Ω series OCT without calibration | $V_{CCIO} = 1.5, 1.2$ | ± 50 | ± 50 | % |
| 50- Ω R_S 1.5, 1.2 | 50- Ω series OCT without calibration | $V_{CCIO} = 1.5, 1.2$ | ± 50 | ± 50 | % |
| 25- Ω R_S 3.0, 2.5, 1.8, 1.5, 1.2 | 25- Ω series OCT with calibration | $V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2$ | ± 10 | ± 10 | % |

Table 1-11. OCT With and Without Calibration Specification for Arria II GX Device I/Os (Note 1) (Part 2 of 2)

| Symbol | Description | Conditions (V) | Calibration Accuracy | | Unit |
|---|--|--|----------------------|------------|------|
| | | | Commercial | Industrial | |
| 50-Ω R _S 3.0, 2.5, 1.8, 1.5, 1.2 | 50-Ω series OCT with calibration | V _{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2 | ± 10 | ± 10 | % |
| 100-Ω R _D 2.5 | 100-Ω differential OCT without calibration | V _{CCIO} = 2.5 | ± 30 | ± 30 | % |

Note to Table 1-11:

(1) OCT with calibration accuracy is valid at the time of calibration only.

Table 1-12 lists the OCT termination calibration accuracy specifications for Arria II GZ devices.

Table 1-12. OCT with Calibration Accuracy Specifications for Arria II GZ Devices (Note 1)

| Symbol | Description | Conditions (V) | Calibration Accuracy | | | Unit |
|--|--|--|----------------------|-------|-------|------|
| | | | C2 | C3,I3 | C4,I4 | |
| 25-Ω R _S 3.0, 2.5, 1.8, 1.5, 1.2 (2) | 25-Ω series OCT with calibration | V _{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2 | ± 8 | ± 8 | ± 8 | % |
| 50-Ω R _S 3.0, 2.5, 1.8, 1.5, 1.2 | 50-Ω internal series OCT with calibration | V _{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2 | ± 8 | ± 8 | ± 8 | % |
| 50-Ω R _T 2.5, 1.8, 1.5, 1.2 | 50-Ω internal parallel OCT with calibration | V _{CCIO} = 2.5, 1.8, 1.5, 1.2 | ± 10 | ± 10 | ± 10 | % |
| 20-Ω, 40-Ω, and 60-Ω R _S 3.0, 2.5, 1.8, 1.5, 1.2 (3) | 20-Ω, 40-Ω and 60-Ω R _S expanded range for internal series OCT with calibration | V _{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2 | ± 10 | ± 10 | ± 10 | % |
| 25-Ω R _{S, left, shift} 3.0, 2.5, 1.8, 1.5, 1.2 | 25-Ω R _{S, left, shift} internal left shift series OCT with calibration | V _{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2 | ± 10 | ± 10 | ± 10 | % |

Notes to Table 1-12:

- (1) OCT calibration accuracy is valid at the time of calibration only.
- (2) 25-Ω R_S is not supported for 1.5 V and 1.2 V in Row I/O.
- (3) 20-Ω R_S is not supported for 1.5 V and 1.2 V in Row I/O.

The calibration accuracy for calibrated series and parallel OCTs are applicable at the moment of calibration. When process, voltage, and temperature (PVT) conditions change after calibration, the tolerance may change.

Table 1-13 lists the Arria II GZ OCT without calibration resistance tolerance to PVT changes.

Table 1-13. OCT Without Calibration Resistance Tolerance Specifications for Arria II GZ Devices

| Symbol | Description | Conditions (V) | Resistance Tolerance | | Unit |
|------------------------------------|--|------------------------------|----------------------|-------|------|
| | | | C3,I3 | C4,I4 | |
| 25-Ω R _S 3.0 and 2.5 | 25-Ω internal series OCT without calibration | V _{CCIO} = 3.0, 2.5 | ± 40 | ± 40 | % |
| 25-Ω R _S 1.8 and 1.5 | 25-Ω internal series OCT without calibration | V _{CCIO} = 1.8, 1.5 | ± 40 | ± 40 | % |
| 25-Ω R _S 1.2 | 25-Ω internal series OCT without calibration | V _{CCIO} = 1.2 | ± 50 | ± 50 | % |
| 50-Ω R _S 3.0 and 2.5 | 50-Ω internal series OCT without calibration | V _{CCIO} = 3.0, 2.5 | ± 40 | ± 40 | % |
| 50-Ω R _S 1.8 and 1.5 | 50-Ω internal series OCT without calibration | V _{CCIO} = 1.8, 1.5 | ± 40 | ± 40 | % |
| 50-Ω R _S 1.2 | 50-Ω internal series OCT without calibration | V _{CCIO} = 1.2 | ± 50 | ± 50 | % |
| 100-Ω R _D 2.5 | 100-Ω internal differential OCT | V _{CCIO} = 2.5 | ± 25 | ± 25 | % |

OCT calibration is automatically performed at power up for OCT-enabled I/Os. When voltage and temperature conditions change after calibration, the resistance may change. Use Equation 1-1 and Table 1-14 to determine the OCT variation when voltage and temperature vary after power-up calibration for Arria II GX and GZ devices.

Equation 1-1. OCT Variation (Note 1)

$$R_{OCT} = R_{SCAL} \left(1 + \left\langle \frac{dR}{dT} \times \Delta T \right\rangle \pm \left\langle \frac{dR}{dV} \times \Delta V \right\rangle \right)$$

Notes to Equation 1-1:

- (1) R_{OCT} value calculated from Equation 1-1 shows the range of OCT resistance with the variation of temperature and V_{CCIO}.

Use the following with [Equation 1-1](#):

- R_{SCAL} is the OCT resistance value at power up.
- ΔT is the variation of temperature with respect to the temperature at power up.
- ΔV is the variation of voltage with respect to the V_{CCIO} at power up.
- dR/dT is the percentage change of R_{SCAL} with temperature.
- dR/dV is the percentage change of R_{SCAL} with voltage.

[Table 1-14](#) lists the OCT variation with temperature and voltage after power-up calibration for Arria II GX devices.

Table 1-14. OCT Variation after Power-up Calibration for Arria II GX Devices

| Nominal Voltage V_{CCIO} (V) | dR/dT (%/°C) | dR/dV (%/mV) |
|--------------------------------|----------------|----------------|
| 3.0 | 0.262 | 0.035 |
| 2.5 | 0.234 | 0.039 |
| 1.8 | 0.219 | 0.086 |
| 1.5 | 0.199 | 0.136 |
| 1.2 | 0.161 | 0.288 |

[Table 1-15](#) lists the OCT variation with temperature and voltage after power-up calibration for Arria II GZ devices.

Table 1-15. OCT Variation after Power-Up Calibration for Arria II GZ Devices (Note 1)

| Nominal Voltage, V_{CCIO} (V) | dR/dT (%/°C) | dR/dV (%/mV) |
|---------------------------------|----------------|----------------|
| 3.0 | 0.189 | 0.0297 |
| 2.5 | 0.208 | 0.0344 |
| 1.8 | 0.266 | 0.0499 |
| 1.5 | 0.273 | 0.0744 |
| 1.2 | 0.317 | 0.1241 |

Note to Table 1-15:

(1) Valid for V_{CCIO} range of $\pm 5\%$ and temperature range of 0° to 85°C .

Pin Capacitance

[Table 1-16](#) lists the pin capacitance for Arria II GX devices.

Table 1-16. Pin Capacitance for Arria II GX Devices

| Symbol | Description | Typical | Unit |
|----------|--|---------|------|
| C_{IO} | Input capacitance on I/O pins, dual-purpose pins (differential I/O, clock, R_{up} , R_{dn}), and dedicated clock input pins | 7 | pF |

Table 1-17 lists the pin capacitance for Arria II GZ devices.

Table 1-17. Pin Capacitance for Arria II GZ Devices

| Symbol | Description | Typical | Unit |
|---|--|---------|------|
| C_{IOTB} | Input capacitance on the top and bottom I/O pins | 4 | pF |
| C_{IOLR} | Input capacitance on the left and right I/O pins | 4 | pF |
| C_{CLKTB} | Input capacitance on the top and bottom non-dedicated clock input pins | 4 | pF |
| C_{CLKLR} | Input capacitance on the left and right non-dedicated clock input pins | 4 | pF |
| C_{OUTFB} | Input capacitance on the dual-purpose clock output and feedback pins | 5 | pF |
| C_{CLK1} , C_{CLK3} , C_{CLK8} , and C_{CLK10} | Input capacitance for dedicated clock input pins | 2 | pF |

Internal Weak Pull-Up and Weak Pull-Down Resistors

Table 1-18 lists the weak pull-up and pull-down resistor values for Arria II GX devices.

Table 1-18. Internal Weak Pull-up and Weak Pull-Down Resistors for Arria II GX Devices (Note 1)

| Symbol | Description | Conditions | Min | Typ | Max | Unit |
|----------|---|---------------------------------------|-----|-----|-----|------------|
| R_{PU} | Value of I/O pin pull-up resistor before and during configuration, as well as user mode if the programmable pull-up resistor option is enabled. | $V_{CCIO} = 3.3\text{ V} \pm 5\%$ (2) | 7 | 25 | 41 | k Ω |
| | | $V_{CCIO} = 3.0\text{ V} \pm 5\%$ (2) | 7 | 28 | 47 | k Ω |
| | | $V_{CCIO} = 2.5\text{ V} \pm 5\%$ (2) | 8 | 35 | 61 | k Ω |
| | | $V_{CCIO} = 1.8\text{ V} \pm 5\%$ (2) | 10 | 57 | 108 | k Ω |
| | | $V_{CCIO} = 1.5\text{ V} \pm 5\%$ (2) | 13 | 82 | 163 | k Ω |
| R_{PD} | Value of TCK pin pull-down resistor | $V_{CCIO} = 3.3\text{ V} \pm 5\%$ | 6 | 19 | 29 | k Ω |
| | | $V_{CCIO} = 3.0\text{ V} \pm 5\%$ | 6 | 22 | 32 | k Ω |
| | | $V_{CCIO} = 2.5\text{ V} \pm 5\%$ | 6 | 25 | 42 | k Ω |
| | | $V_{CCIO} = 1.8\text{ V} \pm 5\%$ | 7 | 35 | 70 | k Ω |
| | | $V_{CCIO} = 1.5\text{ V} \pm 5\%$ | 8 | 50 | 112 | k Ω |

Notes to Table 1-18:

- (1) All I/O pins have an option to enable weak pull-up except configuration, test, and JTAG pins. The weak pull-down feature is only available for JTAG TCK.
- (2) Pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO} .

Table 1-19 lists the weak pull-up resistor values for Arria II GZ devices.

Table 1-19. Internal Weak Pull-Up Resistor for Arria II GZ Devices (Note 1), (2)

| Symbol | Description | Conditions | Min | Typ | Max | Unit |
|-----------------|---|-----------------------------------|-----|-----|-----|------|
| R _{PU} | Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if the programmable pull-up resistor option is enabled. | V _{CCIO} = 3.0 V ±5% (3) | — | 25 | — | kΩ |
| | | V _{CCIO} = 2.5 V ±5% (3) | — | 25 | — | kΩ |
| | | V _{CCIO} = 1.8 V ±5% (3) | — | 25 | — | kΩ |
| | | V _{CCIO} = 1.5 V ±5% (3) | — | 25 | — | kΩ |
| | | V _{CCIO} = 1.2 V ±5% (3) | — | 25 | — | kΩ |

Notes to Table 1-19:

- All I/O pins have an option to enable weak pull-up except configuration, test, and JTAG pins.
- The internal weak pull-down feature is only available for the JTAG TCK pin. The typical value for this internal weak pull-down resistor is approximately 25 kΩ.
- Pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO}.

Hot Socketing

Table 1-20 lists the hot-socketing specification for Arria II GX and GZ devices.

Table 1-20. Hot Socketing Specifications for Arria II Devices

| Symbol | Description | Maximum |
|-------------------------|-----------------------------------|----------|
| I _{IOPIN(DC)} | DC current per I/O pin | 300 μA |
| I _{IOPIN(AC)} | AC current per I/O pin | 8 mA (1) |
| I _{XCVRTX(DC)} | DC current per transceiver TX pin | 100 mA |
| I _{XCVRRX(DC)} | DC current per transceiver RX pin | 50 mA |

Note to Table 1-20:

- The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns, |I_{IOPIN}| = C dv/dt, in which “C” is I/O pin capacitance and “dv/dt” is slew rate.

Schmitt Trigger Input

The Arria II GX device supports Schmitt trigger input on the TDI, TMS, TCK, nSTATUS, nCONFIG, nCE, CONF_DONE, and DCLK pins. A Schmitt trigger feature introduces hysteresis to the input signal for improved noise immunity, especially for signals with slow edge rates.

Table 1-21 lists the hysteresis specifications across the supported V_{CCIO} range for Schmitt trigger inputs in Arria II GX devices.

Table 1-21. Schmitt Trigger Input Hysteresis Specifications for Arria II GX Devices

| Symbol | Description | Condition (V) | Minimum | Unit |
|----------------------|--------------------------------------|-------------------------|---------|------|
| V _{Schmitt} | Hysteresis for Schmitt trigger input | V _{CCIO} = 3.3 | 220 | mV |
| | | V _{CCIO} = 2.5 | 180 | mV |
| | | V _{CCIO} = 1.8 | 110 | mV |
| | | V _{CCIO} = 1.5 | 70 | mV |

I/O Standard Specifications

Table 1–22 through Table 1–35 list input voltage (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}) for various I/O standards supported by the Arria II device family. They also show the Arria II device family I/O standard specifications. V_{OL} and V_{OH} values are valid at the corresponding I_{OH} and I_{OL} , respectively.



For an explanation of terms used in Table 1–22 through Table 1–35, refer to “Glossary” on page 1–74.

Table 1–22 lists the single-ended I/O standards for Arria II GX devices.

Table 1–22. Single-Ended I/O Standards for Arria II GX Devices

| I/O Standard | V_{CCIO} (V) | | | V_{IL} (V) | | V_{IH} (V) | | V_{OL} (V) | V_{OH} (V) | I_{OL} (mA) | I_{OH} (mA) |
|--------------|----------------|-----|-------|--------------|------------------------|------------------------|------------------|------------------------|------------------------|---------------|---------------|
| | Min | Typ | Max | Min | Max | Min | Max | Max | Min | | |
| 3.3 V LVTTTL | 3.135 | 3.3 | 3.465 | -0.3 | 0.8 | 1.7 | 3.6 | 0.45 | 2.4 | 4 | -4 |
| 3.3 V LVCMOS | 3.135 | 3.3 | 3.465 | -0.3 | 0.8 | 1.7 | 3.6 | 0.2 | $V_{CCIO} - 0.2$ | 2 | -2 |
| 3.0 V LVTTTL | 2.85 | 3 | 3.15 | -0.3 | 0.8 | 1.7 | $V_{CCIO} + 0.3$ | 0.45 | 2.4 | 4 | -4 |
| 3.0 V LVCMOS | 2.85 | 3 | 3.15 | -0.3 | 0.8 | 1.7 | $V_{CCIO} + 0.3$ | 0.2 | $V_{CCIO} - 0.2$ | 0.1 | -0.1 |
| 2.5 V LVCMOS | 2.375 | 2.5 | 2.625 | -0.3 | 0.7 | 1.7 | $V_{CCIO} + 0.3$ | 0.4 | 2 | 1 | -1 |
| 1.8 V LVCMOS | 1.71 | 1.8 | 1.89 | -0.3 | $0.35 \times V_{CCIO}$ | $0.65 \times V_{CCIO}$ | $V_{CCIO} + 0.3$ | 0.45 | $V_{CCIO} - 0.45$ | 2 | -2 |
| 1.5 V LVCMOS | 1.425 | 1.5 | 1.575 | -0.3 | $0.35 \times V_{CCIO}$ | $0.65 \times V_{CCIO}$ | $V_{CCIO} + 0.3$ | $0.25 \times V_{CCIO}$ | $0.75 \times V_{CCIO}$ | 2 | -2 |
| 1.2 V LVCMOS | 1.14 | 1.2 | 1.26 | -0.3 | $0.35 \times V_{CCIO}$ | $0.65 \times V_{CCIO}$ | $V_{CCIO} + 0.3$ | $0.25 \times V_{CCIO}$ | $0.75 \times V_{CCIO}$ | 2 | -2 |
| 3.0-V PCI | 2.85 | 3 | 3.15 | — | $0.3 \times V_{CCIO}$ | $0.5 \times V_{CCIO}$ | $V_{CCIO} + 0.3$ | $0.1 \times V_{CCIO}$ | $0.9 \times V_{CCIO}$ | 1.5 | -0.5 |
| 3.0-V PCI-X | 2.85 | 3 | 3.15 | — | $0.35 \times V_{CCIO}$ | $0.5 \times V_{CCIO}$ | $V_{CCIO} + 0.3$ | $0.1 \times V_{CCIO}$ | $0.9 \times V_{CCIO}$ | 1.5 | -0.5 |

Table 1–23 lists the single-ended I/O standards for Arria II GZ devices.

Table 1–23. Single-Ended I/O Standards for Arria II GZ Devices (Part 1 of 2)

| I/O Standard | V_{CCIO} (V) | | | V_{IL} (V) | | V_{IH} (V) | | V_{OL} (V) | V_{OH} (V) | I_{OL} (mA) | I_{OH} (mA) |
|--------------|----------------|-----|-------|--------------|------------------------|------------------------|------------------|------------------------|------------------------|---------------|---------------|
| | Min | Typ | Max | Min | Max | Min | Max | Max | Min | | |
| LVTTTL | 2.85 | 3 | 3.15 | -0.3 | 0.8 | 1.7 | 3.6 | 0.4 | 2.4 | 2 | -2 |
| LVCMOS | 2.85 | 3 | 3.15 | -0.3 | 0.8 | 1.7 | 3.6 | 0.2 | $V_{CCIO} - 0.2$ | 0.1 | -0.1 |
| 2.5 V | 2.375 | 2.5 | 2.625 | -0.3 | 0.7 | 1.7 | 3.6 | 0.4 | 2 | 1 | -1 |
| 1.8 V | 1.71 | 1.8 | 1.89 | -0.3 | $0.35 \times V_{CCIO}$ | $0.65 \times V_{CCIO}$ | $V_{CCIO} + 0.3$ | 0.45 | $V_{CCIO} - 0.45$ | 2 | -2 |
| 1.5 V | 1.425 | 1.5 | 1.575 | -0.3 | $0.35 \times V_{CCIO}$ | $0.65 \times V_{CCIO}$ | $V_{CCIO} + 0.3$ | $0.25 \times V_{CCIO}$ | $0.75 \times V_{CCIO}$ | 2 | -2 |

Table 1-23. Single-Ended I/O Standards for Arria II GZ Devices (Part 2 of 2)

| I/O Standard | V _{CCIO} (V) | | | V _{IL} (V) | | V _{IH} (V) | | V _{OL} (V) | V _{OH} (V) | I _{OL} (mA) | I _{OH} (mA) |
|--------------|-----------------------|-----|------|---------------------|--------------------------|--------------------------|-------------------------|--------------------------|--------------------------|----------------------|----------------------|
| | Min | Typ | Max | Min | Max | Min | Max | Max | Min | | |
| 1.2 V | 1.14 | 1.2 | 1.26 | -0.3 | 0.35 × V _{CCIO} | 0.65 × V _{CCIO} | V _{CCIO} + 0.3 | 0.25 × V _{CCIO} | 0.75 × V _{CCIO} | 2 | -2 |
| 3.0-V PCI | 2.85 | 3 | 3.15 | — | 0.3 × V _{CCIO} | 0.5 × V _{CCIO} | 3.6 | 0.1 × V _{CCIO} | 0.9 × V _{CCIO} | 1.5 | -0.5 |
| 3.0-V PCI-X | 2.85 | 3 | 3.15 | — | 0.35 × V _{CCIO} | 0.5 × V _{CCIO} | — | 0.1 × V _{CCIO} | 0.9 × V _{CCIO} | 1.5 | -0.5 |

Table 1-24 lists the single-ended SSTL and HSTL I/O reference voltage specifications for Arria II GX devices.

Table 1-24. Single-Ended SSTL and HSTL I/O Reference Voltage Specifications for Arria II GX Devices

| I/O Standard | V _{CCIO} (V) | | | V _{REF} (V) | | | V _{TT} (V) | | |
|---------------------|-----------------------|-----|-------|--------------------------|-------------------------|--------------------------|--------------------------|-------------------------|--------------------------|
| | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max |
| SSTL-2 Class I, II | 2.375 | 2.5 | 2.625 | 0.49 × V _{CCIO} | 0.5 × V _{CCIO} | 0.51 × V _{CCIO} | V _{REF} - 0.04 | V _{REF} | V _{REF} + 0.04 |
| SSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.833 | 0.9 | 0.969 | V _{REF} - 0.04 | V _{REF} | V _{REF} + 0.04 |
| SSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.47 × V _{CCIO} | 0.5 × V _{CCIO} | 0.53 × V _{CCIO} | 0.47 × V _{CCIO} | 0.5 × V _{CCIO} | 0.53 × V _{CCIO} |
| HSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.85 | 0.9 | 0.95 | 0.85 | 0.9 | 0.95 |
| HSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.71 | 0.75 | 0.79 | 0.71 | 0.75 | 0.79 |
| HSTL-12 Class I, II | 1.14 | 1.2 | 1.26 | 0.48 × V _{CCIO} | 0.5 × V _{CCIO} | 0.52 × V _{CCIO} | — | V _{CCIO} /2 | — |

Table 1-25 lists the single-ended SSTL and HSTL I/O reference voltage specifications for Arria II GZ devices.

Table 1-25. Single-Ended SSTL and HSTL I/O Reference Voltage Specifications for Arria II GZ Devices

| I/O Standard | V _{CCIO} (V) | | | V _{REF} (V) | | | V _{TT} (V) | | |
|---------------------|-----------------------|-----|-------|--------------------------|-------------------------|--------------------------|--------------------------|----------------------|--------------------------|
| | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max |
| SSTL-2 Class I, II | 2.375 | 2.5 | 2.625 | 0.49 × V _{CCIO} | 0.5 × V _{CCIO} | 0.51 × V _{CCIO} | V _{REF} - 0.04 | V _{REF} | V _{REF} + 0.04 |
| SSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.833 | 0.9 | 0.969 | V _{REF} - 0.04 | V _{REF} | V _{REF} + 0.04 |
| SSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.47 × V _{CCIO} | 0.5 × V _{CCIO} | 0.53 × V _{CCIO} | 0.47 × V _{CCIO} | V _{REF} | 0.53 × V _{CCIO} |
| HSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.85 | 0.9 | 0.95 | — | V _{CCIO} /2 | — |
| HSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.68 | 0.75 | 0.9 | — | V _{CCIO} /2 | — |
| HSTL-12 Class I, II | 1.14 | 1.2 | 1.26 | 0.47 × V _{CCIO} | 0.5 × V _{CCIO} | 0.53 × V _{CCIO} | — | V _{CCIO} /2 | — |

Table 1-26 lists the single-ended SSTL and HSTL I/O standard signal specifications for Arria II GX devices.

Table 1-26. Single-Ended SSTL and HSTL I/O Standard Signal Specifications for Arria II GX Devices

| I/O Standard | $V_{IL(DC)} (V)$ | | $V_{IH(DC)} (V)$ | | $V_{IL(AC)} (V)$ | $V_{IH(AC)} (V)$ | $V_{OL} (V)$ | $V_{OH} (V)$ | $I_{OL} (mA)$ | $I_{OH} (mA)$ |
|------------------|------------------|-------------------|-------------------|-------------------|-------------------|-------------------|------------------------|------------------------|---------------|---------------|
| | Min | Max | Min | Max | Max | Min | Max | Min | | |
| SSTL-2 Class I | -0.3 | $V_{REF} - 0.18$ | $V_{REF} + 0.18$ | $V_{CCIO} + 0.3$ | $V_{REF} - 0.35$ | $V_{REF} + 0.35$ | $V_{TT} - 0.57$ | $V_{TT} + 0.57$ | 8.1 | -8.1 |
| SSTL-2 Class II | -0.3 | $V_{REF} - 0.18$ | $V_{REF} + 0.18$ | $V_{CCIO} + 0.3$ | $V_{REF} - 0.35$ | $V_{REF} + 0.35$ | $V_{TT} - 0.76$ | $V_{TT} + 0.76$ | 16.4 | -16.4 |
| SSTL-18 Class I | -0.3 | $V_{REF} - 0.125$ | $V_{REF} + 0.125$ | $V_{CCIO} + 0.3$ | $V_{REF} - 0.25$ | $V_{REF} + 0.25$ | $V_{TT} - 0.475$ | $V_{TT} + 0.475$ | 6.7 | -6.7 |
| SSTL-18 Class II | -0.3 | $V_{REF} - 0.125$ | $V_{REF} + 0.125$ | $V_{CCIO} + 0.3$ | $V_{REF} - 0.25$ | $V_{REF} + 0.25$ | 0.28 | $V_{CCIO} - 0.28$ | 13.4 | -13.4 |
| SSTL-15 Class I | -0.3 | $V_{REF} - 0.1$ | $V_{REF} + 0.1$ | $V_{CCIO} + 0.3$ | $V_{REF} - 0.175$ | $V_{REF} + 0.175$ | $0.2 \times V_{CCIO}$ | $0.8 \times V_{CCIO}$ | 8 | -8 |
| SSTL-15 Class II | -0.3 | $V_{REF} - 0.1$ | $V_{REF} + 0.1$ | $V_{CCIO} + 0.3$ | $V_{REF} - 0.175$ | $V_{REF} + 0.175$ | $0.2 \times V_{CCIO}$ | $0.8 \times V_{CCIO}$ | 16 | -16 |
| HSTL-18 Class I | -0.3 | $V_{REF} - 0.1$ | $V_{REF} + 0.1$ | $V_{CCIO} + 0.3$ | $V_{REF} - 0.2$ | $V_{REF} + 0.2$ | 0.4 | $V_{CCIO} - 0.4$ | 8 | -8 |
| HSTL-18 Class II | -0.3 | $V_{REF} - 0.1$ | $V_{REF} + 0.1$ | $V_{CCIO} + 0.3$ | $V_{REF} - 0.2$ | $V_{REF} + 0.2$ | 0.4 | $V_{CCIO} - 0.4$ | 16 | -16 |
| HSTL-15 Class I | -0.3 | $V_{REF} - 0.1$ | $V_{REF} + 0.1$ | $V_{CCIO} + 0.3$ | $V_{REF} - 0.2$ | $V_{REF} + 0.2$ | 0.4 | $V_{CCIO} - 0.4$ | 8 | -8 |
| HSTL-15 Class II | -0.3 | $V_{REF} - 0.1$ | $V_{REF} + 0.1$ | $V_{CCIO} + 0.3$ | $V_{REF} - 0.2$ | $V_{REF} + 0.2$ | 0.4 | $V_{CCIO} - 0.4$ | 16 | -16 |
| HSTL-12 Class I | -0.15 | $V_{REF} - 0.08$ | $V_{REF} + 0.08$ | $V_{CCIO} + 0.15$ | $V_{REF} - 0.15$ | $V_{REF} + 0.15$ | $0.25 \times V_{CCIO}$ | $0.75 \times V_{CCIO}$ | 8 | -8 |
| HSTL-12 Class II | -0.15 | $V_{REF} - 0.08$ | $V_{REF} + 0.08$ | $V_{CCIO} + 0.15$ | $V_{REF} - 0.15$ | $V_{REF} + 0.15$ | $0.25 \times V_{CCIO}$ | $0.75 \times V_{CCIO}$ | 14 | -14 |

Table 1-27 lists the single-ended SSTL and HSTL I/O standard signal specifications for Arria II GZ devices.

Table 1-27. Single-Ended SSTL and HSTL I/O Standards Signal Specifications for Arria II GZ Devices (Part 1 of 2)

| I/O Standard | $V_{IL(DC)} (V)$ | | $V_{IH(DC)} (V)$ | | $V_{IL(AC)} (V)$ | $V_{IH(AC)} (V)$ | $V_{OL} (V)$ | $V_{OH} (V)$ | $I_{OL} (mA)$ | $I_{OH} (mA)$ |
|------------------|------------------|-------------------|-------------------|------------------|-------------------|-------------------|-----------------------|-----------------------|---------------|---------------|
| | Min | Max | Min | Max | Max | Min | Max | Min | | |
| SSTL-2 Class I | -0.3 | $V_{REF} - 0.15$ | $V_{REF} + 0.15$ | $V_{CCIO} + 0.3$ | $V_{REF} - 0.31$ | $V_{REF} + 0.31$ | $V_{TT} - 0.57$ | $V_{TT} + 0.57$ | 8.1 | -8.1 |
| SSTL-2 Class II | -0.3 | $V_{REF} - 0.15$ | $V_{REF} + 0.15$ | $V_{CCIO} + 0.3$ | $V_{REF} - 0.31$ | $V_{REF} + 0.31$ | $V_{TT} - 0.76$ | $V_{TT} + 0.76$ | 16.2 | -16.2 |
| SSTL-18 Class I | -0.3 | $V_{REF} - 0.125$ | $V_{REF} + 0.125$ | $V_{CCIO} + 0.3$ | $V_{REF} - 0.25$ | $V_{REF} + 0.25$ | $V_{TT} - 0.475$ | $V_{TT} + 0.475$ | 6.7 | -6.7 |
| SSTL-18 Class II | -0.3 | $V_{REF} - 0.125$ | $V_{REF} + 0.125$ | $V_{CCIO} + 0.3$ | $V_{REF} - 0.25$ | $V_{REF} + 0.25$ | 0.28 | $V_{CCIO} - 0.28$ | 13.4 | -13.4 |
| SSTL-15 Class I | — | $V_{REF} - 0.1$ | $V_{REF} + 0.1$ | — | $V_{REF} - 0.175$ | $V_{REF} + 0.175$ | $0.2 \times V_{CCIO}$ | $0.8 \times V_{CCIO}$ | 8 | -8 |

Table 1-27. Single-Ended SSTL and HSTL I/O Standards Signal Specifications for Arria II GZ Devices (Part 2 of 2)

| I/O Standard | $V_{IL(DC)}$ (V) | | $V_{IH(DC)}$ (V) | | $V_{IL(AC)}$ (V) | $V_{IH(AC)}$ (V) | V_{OL} (V) | V_{OH} (V) | I_{OL} (mA) | I_{OH} (mA) |
|------------------|------------------|------------------|------------------|-------------------|-------------------|-------------------|------------------------|------------------------|---------------|---------------|
| | Min | Max | Min | Max | Max | Min | Max | Min | | |
| SSTL-15 Class II | — | $V_{REF} - 0.1$ | $V_{REF} + 0.1$ | — | $V_{REF} - 0.175$ | $V_{REF} + 0.175$ | $0.2 \times V_{CCIO}$ | $0.8 \times V_{CCIO}$ | 16 | -16 |
| HSTL-18 Class I | — | $V_{REF} - 0.1$ | $V_{REF} + 0.1$ | — | $V_{REF} - 0.2$ | $V_{REF} + 0.2$ | 0.4 | $V_{CCIO} - 0.4$ | 8 | -8 |
| HSTL-18 Class II | — | $V_{REF} - 0.1$ | $V_{REF} + 0.1$ | — | $V_{REF} - 0.2$ | $V_{REF} + 0.2$ | 0.4 | $V_{CCIO} - 0.4$ | 16 | -16 |
| HSTL-15 Class I | — | $V_{REF} - 0.1$ | $V_{REF} + 0.1$ | — | $V_{REF} - 0.2$ | $V_{REF} + 0.2$ | 0.4 | $V_{CCIO} - 0.4$ | 8 | -8 |
| HSTL-15 Class II | — | $V_{REF} - 0.1$ | $V_{REF} + 0.1$ | — | $V_{REF} - 0.2$ | $V_{REF} + 0.2$ | 0.4 | $V_{CCIO} - 0.4$ | 16 | -16 |
| HSTL-12 Class I | -0.15 | $V_{REF} - 0.08$ | $V_{REF} + 0.08$ | $V_{CCIO} + 0.15$ | $V_{REF} - 0.15$ | $V_{REF} + 0.15$ | $0.25 \times V_{CCIO}$ | $0.75 \times V_{CCIO}$ | 8 | -8 |
| HSTL-12 Class II | -0.15 | $V_{REF} - 0.08$ | $V_{REF} + 0.08$ | $V_{CCIO} + 0.15$ | $V_{REF} - 0.15$ | $V_{REF} + 0.15$ | $0.25 \times V_{CCIO}$ | $0.75 \times V_{CCIO}$ | 16 | -16 |

Table 1-28 lists the differential SSTL I/O standards for Arria II GX devices.

Table 1-28. Differential SSTL I/O Standards for Arria II GX Devices

| I/O Standard | V_{CCIO} (V) | | | $V_{SWING(DC)}$ (V) | | $V_{X(AC)}$ (V) | | | $V_{SWING(AC)}$ (V) | | $V_{OX(AC)}$ (V) | | |
|---------------------|----------------|-----|-------|---------------------|------------|----------------------|--------------|----------------------|---------------------|------------|----------------------|--------------|----------------------|
| | Min | Typ | Max | Min | Max | Min | Typ | Max | Min | Max | Min | Typ | Max |
| SSTL-2 Class I, II | 2.375 | 2.5 | 2.625 | 0.36 | V_{CCIO} | $V_{CCIO}/2 - 0.2$ | — | $V_{CCIO}/2 + 0.2$ | 0.7 | V_{CCIO} | $V_{CCIO}/2 - 0.15$ | — | $V_{CCIO}/2 + 0.15$ |
| SSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.25 | V_{CCIO} | $V_{CCIO}/2 - 0.175$ | — | $V_{CCIO}/2 + 0.175$ | 0.5 | V_{CCIO} | $V_{CCIO}/2 - 0.125$ | — | $V_{CCIO}/2 + 0.125$ |
| SSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.2 | — | — | $V_{CCIO}/2$ | — | 0.35 | — | — | $V_{CCIO}/2$ | — |

Table 1-29 lists the differential SSTL I/O standards for Arria II GZ devices

Table 1-29. Differential SSTL I/O Standards for Arria II GZ Devices

| I/O Standard | V_{CCIO} (V) | | | $V_{SWING(DC)}$ (V) | | $V_{X(AC)}$ (V) | | | $V_{SWING(AC)}$ (V) | | $V_{OX(AC)}$ (V) | | |
|---------------------|----------------|-----|-------|---------------------|------------------|----------------------|--------------|----------------------|---------------------|------------------|----------------------|--------------|----------------------|
| | Min | Typ | Max | Min | Max | Min | Typ | Max | Min | Max | Min | Typ | Max |
| SSTL-2 Class I, II | 2.375 | 2.5 | 2.625 | 0.3 | $V_{CCIO} + 0.6$ | $V_{CCIO}/2 - 0.2$ | — | $V_{CCIO}/2 + 0.2$ | 0.62 | $V_{CCIO} + 0.6$ | $V_{CCIO}/2 - 0.15$ | — | $V_{CCIO}/2 + 0.15$ |
| SSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.25 | $V_{CCIO} + 0.6$ | $V_{CCIO}/2 - 0.175$ | — | $V_{CCIO}/2 + 0.175$ | 0.5 | $V_{CCIO} + 0.6$ | $V_{CCIO}/2 - 0.125$ | — | $V_{CCIO}/2 + 0.125$ |
| SSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.2 | — | — | $V_{CCIO}/2$ | — | 0.35 | — | — | $V_{CCIO}/2$ | — |

Table 1-30 lists the HSTL I/O standards for Arria II GX devices.

Table 1-30. Differential HSTL I/O Standards for Arria II GX Devices

| I/O Standard | V_{CCIO} (V) | | | $V_{DIF(DC)}$ (V) | | $V_{X(AC)}$ (V) | | | $V_{CM(DC)}$ (V) | | | $V_{DIF(AC)}$ (V) | |
|---------------------|----------------|-----|-------|-------------------|-----|-----------------|-----------------------|------|------------------------|-----------------------|------------------------|-------------------|-----|
| | Min | Typ | Max | Min | Max | Min | Typ | Max | Min | Typ | Max | Min | Max |
| HSTL-18 Class I | 1.71 | 1.8 | 1.89 | 0.2 | — | 0.85 | — | 0.95 | 0.88 | — | 0.95 | 0.4 | — |
| HSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.2 | — | 0.71 | — | 0.79 | 0.71 | — | 0.79 | 0.4 | — |
| HSTL-12 Class I, II | 1.14 | 1.2 | 1.26 | 0.16 | — | — | $0.5 \times V_{CCIO}$ | — | $0.48 \times V_{CCIO}$ | $0.5 \times V_{CCIO}$ | $0.52 \times V_{CCIO}$ | 0.3 | — |

Table 1-31 lists the HSTL I/O standards for Arria II GZ devices.

Table 1-31. Differential HSTL I/O Standards for Arria II GZ Devices

| I/O Standard | V_{CCIO} (V) | | | $V_{DIF(DC)}$ (V) | | $V_{X(AC)}$ (V) | | | $V_{CM(DC)}$ (V) | | | $V_{DIF(AC)}$ (V) | |
|---------------------|----------------|-----|-------|-------------------|------------------|-----------------|-----------------------|------|-----------------------|-----------------------|-----------------------|-------------------|-------------------|
| | Min | Typ | Max | Min | Max | Min | Typ | Max | Min | Typ | Max | Min | Max |
| HSTL-18 Class I | 1.71 | 1.8 | 1.89 | 0.2 | — | 0.78 | — | 1.12 | 0.78 | — | 1.12 | 0.4 | — |
| HSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.2 | — | 0.68 | — | 0.9 | 0.68 | — | 0.9 | 0.4 | — |
| HSTL-12 Class I, II | 1.14 | 1.2 | 1.26 | 0.16 | $V_{CCIO} + 0.3$ | — | $0.5 \times V_{CCIO}$ | — | $0.4 \times V_{CCIO}$ | $0.5 \times V_{CCIO}$ | $0.6 \times V_{CCIO}$ | 0.3 | $V_{CCIO} + 0.48$ |

Table 1-32 lists the differential I/O standard specifications for Arria II GX devices.

Table 1-32. Differential I/O Standard Specifications for Arria II GX Devices (Note 1)

| I/O Standard | V_{CCIO} (V) | | | V_{ID} (mV) | | | V_{ICM} (V) (2) | | V_{OD} (V) (3) | | | V_{OCM} (V) | | |
|---------------|----------------|-----|-------|---------------|-------------------|-----|-------------------|------|------------------|-----|-----|---------------|------|-------|
| | Min | Typ | Max | Min | Cond. | Max | Min | Max | Min | Typ | Max | Min | Typ | Max |
| 2.5 V LVDS | 2.375 | 2.5 | 2.625 | 100 | $V_{CM} = 1.25$ V | — | 0.05 | 1.80 | 0.247 | — | 0.6 | 1.125 | 1.25 | 1.375 |
| RSDS (4) | 2.375 | 2.5 | 2.625 | — | — | — | — | — | 0.1 | 0.2 | 0.6 | 0.5 | 1.2 | 1.4 |
| Mini-LVDS (4) | 2.375 | 2.5 | 2.625 | — | — | — | — | — | 0.25 | — | 0.6 | 1 | 1.2 | 1.4 |
| LVPECL (5) | 2.375 | 2.5 | 2.625 | 300 | — | — | 0.6 | 1.8 | — | — | — | — | — | — |
| BLVDS (6) | 2.375 | 2.5 | 2.625 | 100 | — | — | — | — | — | — | — | — | — | — |

Notes to Table 1-32:

- (1) The 1.5 V PCML transceiver I/O standard specifications are described in "Transceiver Performance Specifications" on page 1-21.
- (2) V_{IN} range: $0 \leq V_{IN} \leq 1.85$ V.
- (3) R_L range: $90 \leq R_L \leq 110 \Omega$.
- (4) The RSDS and mini-LVDS I/O standards are only supported for differential outputs.
- (5) The LVPECL input standard is supported at the dedicated clock input pins (GCLK) only.
- (6) There are no fixed V_{ICM} , V_{OD} , and V_{OCM} specifications for BLVDS. These specifications depend on the system topology.

Table 1-33 lists the differential I/O standard specifications for Arria II GZ devices.

Table 1-33. Differential I/O Standard Specifications for Arria II GZ Devices (Note 1)

| I/O Standard (2) | V _{CCIO} (V) | | | V _{ID} (mV) | | | V _{ICM(DC)} (V) | | V _{OD} (V) (3) | | | V _{OCM} (V) (3) | | |
|------------------|-----------------------|-----|-------|----------------------|--------------------------|-----|--------------------------|-------|-------------------------|-----|-----|--------------------------|------|-------|
| | Min | Typ | Max | Min | Cond. | Max | Min | Max | Min | Typ | Max | Min | Typ | Max |
| 2.5 V LVDS (HIO) | 2.375 | 2.5 | 2.625 | 100 | V _{CM} = 1.25 V | — | 0.05 | 1.8 | 0.247 | — | 0.6 | 1.125 | 1.25 | 1.375 |
| 2.5 V LVDS (VIO) | 2.375 | 2.5 | 2.625 | 100 | V _{CM} = 1.25 V | — | 0.05 | 1.8 | 0.247 | — | 0.6 | 1 | 1.25 | 1.5 |
| RSDS (HIO) | 2.375 | 2.5 | 2.625 | 100 | V _{CM} = 1.25 V | — | 0.3 | 1.4 | 0.1 | 0.2 | 0.6 | 0.5 | 1.2 | 1.4 |
| RSDS (VIO) | 2.375 | 2.5 | 2.625 | 100 | V _{CM} = 1.25 V | — | 0.3 | 1.4 | 0.1 | 0.2 | 0.6 | 0.5 | 1.2 | 1.5 |
| Mini-LVDS (HIO) | 2.375 | 2.5 | 2.625 | 200 | — | 600 | 0.4 | 1.325 | 0.25 | — | 0.6 | 1 | 1.2 | 1.4 |
| Mini-LVDS (VIO) | 2.375 | 2.5 | 2.625 | 200 | — | 600 | 0.4 | 1.325 | 0.25 | — | 0.6 | 1 | 1.2 | 1.5 |
| LVPECL | 2.375 | 2.5 | 2.625 | 300 | — | — | 0.6 | 1.8 | — | — | — | — | — | — |
| BLVDS (4) | 2.375 | 2.5 | 2.625 | 100 | — | — | — | — | — | — | — | — | — | — |

Notes to Table 1-33:

- (1) 1.4-V/1.5-V PCML transceiver I/O standard specifications are described in “Transceiver Performance Specifications” on page 1-21.
- (2) Vertical I/O (VIO) is top and bottom I/Os; horizontal I/O (HIO) is left and right I/Os.
- (3) R_L range: 90 ≤ R_L ≤ 110 Ω.
- (4) There are no fixed V_{ICM}, V_{OD}, and V_{OCM} specifications for BLVDS. These specifications depend on the system topology.

Power Consumption for the Arria II Device Family

Altera offers two ways to estimate power for a design:

- Using the Microsoft Excel-based Early Power Estimator
- Using the Quartus® II PowerPlay Power Analyzer feature

The interactive Microsoft Excel-based Early Power Estimator is typically used prior to designing the FPGA in order to get a magnitude estimate of the device power. The Quartus II PowerPlay Power Analyzer provides better quality estimates based on the specifics of the design after place-and-route is complete. The PowerPlay Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities which, when combined with detailed circuit models, can yield very accurate power estimates.



For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in volume 3 of the *Quartus II Handbook*.

Switching Characteristics

This section provides performance characteristics of the Arria II GX and GZ core and periphery blocks for commercial grade devices. The following tables are considered final and are based on actual silicon characterization and testing. These numbers reflect the actual performance of the device under worst-case silicon process, voltage, and junction temperature conditions.

Transceiver Performance Specifications

Table 1–34 lists the Arria II GX transceiver specifications.

Table 1–34. Transceiver Specifications for Arria II GX Devices (Note 1) (Part 1 of 7)

| Symbol/ Description | Condition | I3 | | | C4 | | | C5 and I5 | | | C6 | | | Unit |
|--|---|------|-----|--------|------|-----|--------|-----------|-----|--------|------|-----|--------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Reference Clock | | | | | | | | | | | | | | |
| Supported I/O Standards | 1.2-V PCML, 1.5-V PCML, 2.5-V PCML, Differential LVPECL, LVDS, and HCSL | | | | | | | | | | | | | |
| Input frequency from REFCLK input pins | — | 50 | — | 622.08 | 50 | — | 622.08 | 50 | — | 622.08 | 50 | — | 622.08 | MHz |
| Input frequency from PLD input | — | 50 | — | 200 | 50 | — | 200 | 50 | — | 200 | 50 | — | 200 | MHz |
| Absolute V_{MAX} for a REFCLK pin | — | — | — | 2.2 | — | — | 2.2 | — | — | 2.2 | — | — | 2.2 | V |
| Absolute V_{MIN} for a REFCLK pin | — | –0.3 | — | — | –0.3 | — | — | –0.3 | — | — | –0.3 | — | — | V |
| Rise/fall time (2) | — | — | — | 0.2 | — | — | 0.2 | — | — | 0.2 | — | — | 0.2 | UI |
| Duty cycle | — | 45 | — | 55 | 45 | — | 55 | 45 | — | 55 | 45 | — | 55 | % |
| Peak-to-peak differential input voltage | — | 200 | — | 2000 | 200 | — | 2000 | 200 | — | 2000 | 200 | — | 2000 | mV |
| Spread-spectrum modulating clock frequency | PCIe | 30 | — | 33 | 30 | — | 33 | 30 | — | 33 | 30 | — | 33 | kHz |

Table 1–34. Transceiver Specifications for Arria II GX Devices (Note 1) (Part 2 of 7)

| Symbol/ Description | Condition | I3 | | | C4 | | | C5 and I5 | | | C6 | | | Unit |
|--|--|-----------|---------------|------|-----------|---------------|------|-----------|---------------|------|-----------|---------------|------|--------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Spread-spectrum downspread | PCIe | — | 0 to –0.5% | — | — | 0 to –0.5% | — | — | 0 to –0.5% | — | — | 0 to –0.5% | — | — |
| On-chip termination resistors | — | — | 100 | — | — | 100 | — | — | 100 | — | — | 100 | — | Ω |
| V _{ICM} (AC coupled) | — | 1100 ± 5% | | | 1100 ± 5% | | | 1100 ± 5% | | | 1100 ± 5% | | | mV |
| V _{ICM} (DC coupled) | HCSL I/O standard for PCIe reference clock | 250 | — | 550 | 250 | — | 550 | 250 | — | 550 | 250 | — | 550 | mV |
| Transmitter REFCLK Phase Noise | 10 Hz | — | — | -50 | — | — | -50 | — | — | -50 | — | — | -50 | dBc/Hz |
| | 100 Hz | — | — | -80 | — | — | -80 | — | — | -80 | — | — | -80 | dBc/Hz |
| | 1 KHz | — | — | -110 | — | — | -110 | — | — | -110 | — | — | -110 | dBc/Hz |
| | 10 KHz | — | — | -120 | — | — | -120 | — | — | -120 | — | — | -120 | dBc/Hz |
| | 100 KHz | — | — | -120 | — | — | -120 | — | — | -120 | — | — | -120 | dBc/Hz |
| | ≥ 1 MHz | — | — | -130 | — | — | -130 | — | — | -130 | — | — | -130 | dBc/Hz |
| Transmitter REFCLK Phase Jitter (rms) for 100 MHz REFCLK (3) | 10 KHz to 20 MHz | — | — | 3 | — | — | 3 | — | — | 3 | — | — | 3 | ps |
| R _{ref} | — | — | 2000 ± 1% | — | — | 2000 ± 1% | — | — | 2000 ± 1% | — | — | 2000 ± 1% | — | Ω |
| Transceiver Clocks | | | | | | | | | | | | | | |
| Calibration block clock frequency (cal_blk_clk) | — | 10 | — | 125 | 10 | — | 125 | 10 | — | 125 | 10 | — | 125 | MHz |

Table 1-34. Transceiver Specifications for Arria II GX Devices (Note 1) (Part 3 of 7)

| Symbol/ Description | Condition | I3 | | | C4 | | | C5 and I5 | | | C6 | | | Unit |
|--|--|---------------------|-----|------|---------------------|-----|------|---------------------|-----|------|---------------------|-----|------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| fixedclk clock frequency | PCIe Receiver Detect | — | 125 | — | — | 125 | — | — | 125 | — | — | 125 | — | MHz |
| reconfig_clk clock frequency | Dynamic reconfig. clock frequency | 2.5/ 37.5 (4) | — | 50 | 2.5/ 37.5 (4) | — | 50 | 2.5/ 37.5 (4) | — | 50 | 2.5/ 37.5 (4) | — | 50 | MHz |
| Delta time between reconfig_clks (5) | — | — | — | 2 | — | — | 2 | — | — | 2 | — | — | 2 | ms |
| Transceiver block minimum power-down pulse width | — | — | 1 | — | — | 1 | — | — | 1 | — | — | 1 | — | μs |
| Receiver | | | | | | | | | | | | | | |
| Supported I/O Standards | 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, 2.5-V PCML, LVPECL, and LVDS | | | | | | | | | | | | | |
| Data rate (13) | — | 600 | — | 6375 | 600 | — | 3750 | 600 | — | 3750 | 600 | — | 3125 | Mbps |
| Absolute V _{MAX} for a receiver pin (6) | — | — | — | 1.5 | — | — | 1.5 | — | — | 1.5 | — | — | 1.5 | V |
| Absolute V _{MIN} for a receiver pin | — | -0.4 | — | — | -0.4 | — | — | -0.4 | — | — | -0.4 | — | — | V |
| Maximum peak-to-peak differential input voltage V _{ID} (diff p-p) | V _{ICM} = 0.82 V setting | — | — | 2.7 | — | — | 2.7 | — | — | 2.7 | — | — | 2.7 | V |
| | V _{ICM} = 1.1 V setting (7) | — | — | 1.6 | — | — | 1.6 | — | — | 1.6 | — | — | 1.6 | V |

Table 1–34. Transceiver Specifications for Arria II GX Devices (Note 1) (Part 4 of 7)

| Symbol/ Description | Condition | I3 | | | C4 | | | C5 and I5 | | | C6 | | | Unit |
|---|-------------------------------|--|------|-----|-----|------|-----|-----------|------|-----|-----|------|-----|----------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Minimum peak-to-peak differential input voltage V_{ID} (diff p-p) | — | 100 | — | — | 100 | — | — | 100 | — | — | 100 | — | — | mV |
| V_{ICM} | $V_{ICM} = 0.82$ V setting | — | 820 | — | — | 820 | — | — | 820 | — | — | 820 | — | mV |
| | $V_{ICM} = 1.1$ V setting (7) | — | 1100 | — | — | 1100 | — | — | 1100 | — | — | 1100 | — | mV |
| Differential on-chip termination resistors | 100- Ω setting | — | 100 | — | — | 100 | — | — | 100 | — | — | 100 | — | Ω |
| Return loss differential mode | PCIe | 50 MHz to 1.25 GHz: -10dB | | | | | | | | | | | | |
| | XAUI | 100 MHz to 2.5 GHz: -10dB | | | | | | | | | | | | |
| Return loss common mode | PCIe | 50 MHz to 1.25 GHz: -6dB | | | | | | | | | | | | |
| | XAUI | 100 MHz to 2.5 GHz: -6dB | | | | | | | | | | | | |
| Programmable PPM detector (8) | — | $\pm 62.5, 100, 125, 200, 250, 300, 500, 1000$ | | | | | | | | | | | | ppm |
| Run length | — | — | 80 | — | — | 80 | — | — | 80 | — | — | 80 | — | UI |
| Programmable equalization | — | — | — | 7 | — | — | 7 | — | — | 7 | — | — | 7 | dB |
| Signal detect/loss threshold | PCIe Mode | 65 | — | 175 | 65 | — | 175 | 65 | — | 175 | 65 | — | 175 | mV |
| CDR LTR time (9) | — | — | — | 75 | — | — | 75 | — | — | 75 | — | — | 75 | μ s |
| CDR minimum T1b (10) | — | 15 | — | — | 15 | — | — | 15 | — | — | 15 | — | — | μ s |

Table 1–34. Transceiver Specifications for Arria II GX Devices (Note 1) (Part 5 of 7)

| Symbol/ Description | Condition | I3 | | | C4 | | | C5 and I5 | | | C6 | | | Unit |
|---|------------------------|---|-----|------|-----|-----|------|-----------|-----|------|-----|-----|------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| LTD lock time (11) | — | 0 | 100 | 4000 | 0 | 100 | 4000 | 0 | 100 | 4000 | 0 | 100 | 4000 | ns |
| Data lock time from rx_ freqlocked (12) | — | — | — | 4000 | — | — | 4000 | — | — | 4000 | — | — | 4000 | ns |
| Programmable DC gain | DC Gain Setting = 0 | — | 0 | — | — | 0 | — | — | 0 | — | — | 0 | — | dB |
| | DC Gain Setting = 1 | — | 3 | — | — | 3 | — | — | 3 | — | — | 3 | — | dB |
| | DC Gain Setting = 2 | — | 6 | — | — | 6 | — | — | 6 | — | — | 6 | — | dB |
| Transmitter | | | | | | | | | | | | | | |
| Supported I/O Standards | 1.5-V PCML | | | | | | | | | | | | | |
| Data rate | — | 600 | — | 6375 | 600 | — | 3750 | 600 | — | 3750 | 600 | — | 3125 | Mbps |
| V _{OCM} | 0.65 V setting | — | 650 | — | — | 650 | — | — | 650 | — | — | 650 | — | mV |
| Differential on-chip termination resistors | 100-Ω setting | — | 100 | — | — | 100 | — | — | 100 | — | — | 100 | — | Ω |
| Return loss differential mode | PCIe | 50 MHz to 1.25 GHz: -10dB | | | | | | | | | | | | |
| | XAUI | 312 MHz to 625 MHz: -10dB 625 MHz to 3.125 GHz: -10dB/decade slope | | | | | | | | | | | | |
| Return loss common mode | PCIe | 50 MHz to 1.25 GHz: -6dB | | | | | | | | | | | | |
| Rise time (2) | — | 50 | — | 200 | 50 | — | 200 | 50 | — | 200 | 50 | — | 200 | ps |
| Fall time | — | 50 | — | 200 | 50 | — | 200 | 50 | — | 200 | 50 | — | 200 | ps |

Table 1–34. Transceiver Specifications for Arria II GX Devices (Note 1) (Part 6 of 7)

| Symbol/ Description | Condition | I3 | | | C4 | | | C5 and I5 | | | C6 | | | Unit |
|---|-----------|-----|-----|-----|-----|-----|-----|-----------|-----|-----|-----|-----|-----|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Intra-differential pair skew | — | — | — | 15 | — | — | 15 | — | — | 15 | — | — | 15 | ps |
| Intra-transceiver block skew | PCIe x4 | — | — | 120 | — | — | 120 | — | — | 120 | — | — | 120 | ps |
| Inter-transceiver block skew | PCIe x8 | — | — | 300 | — | — | 300 | — | — | 300 | — | — | 300 | ps |
| CMU PLL0 and CMU PLL1 | | | | | | | | | | | | | | |
| CMU PLL lock time from CMUPLL_reset deassertion | — | — | — | 100 | — | — | 100 | — | — | 100 | — | — | 100 | μs |
| PLD-Transceiver Interface | | | | | | | | | | | | | | |
| Interface speed | — | 25 | — | 320 | 25 | — | 240 | 25 | — | 240 | 25 | — | 200 | MHz |

Table 1–34. Transceiver Specifications for Arria II GX Devices (Note 1) (Part 7 of 7)

| Symbol/ Description | Condition | I3 | | | C4 | | | C5 and I5 | | | C6 | | | Unit |
|---------------------------|-----------|------------------------------------|-----|-----|-----|-----|-----|-----------|-----|-----|-----|-----|-----|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Digital reset pulse width | — | Minimum is 2 parallel clock cycles | | | | | | | | | | | | |

Notes to Table 1–34:

- (1) For AC-coupled links, the on-chip biasing circuit is switched off before and during configuration. Ensure that input specifications are not violated during this period.
- (2) The rise/fall time is specified from 20% to 80%.
- (3) To calculate the REFCLK rms phase jitter requirement at reference clock frequencies other than 100 MHz, use the following formula:
REFCLK rms phase jitter at f (MHz) = REFCLK rms phase jitter at 100 MHz * 100/f.
- (4) The minimum `reconfig_clk` frequency is 2.5 MHz if the transceiver channel is configured in **Transmitter only** mode. The minimum `reconfig_clk` frequency is 37.5 MHz if the transceiver channel is configured in **Receiver only** or **Receiver and Transmitter** mode. For more information, refer to [AN 558: Implementing Dynamic Reconfiguration in Arria II Devices](#).
- (5) If your design uses more than one dynamic reconfiguration controller instances (`altgx_reconfig`) to control the transceiver channels (`altgx`) physically located on the same side of the device, and if you use different `reconfig_clk` sources for these `altgx_reconfig` instances, the delta time between any two of these `reconfig_clk` sources becoming stable must not exceed the maximum specification listed.
- (6) The device cannot tolerate prolonged operation at this absolute maximum.
- (7) You must use the 1.1-V RX V_{ICM} setting if the input serial data standard is LVDS and the link is DC-coupled.
- (8) The rate matcher supports only up to ± 300 parts per million (ppm).
- (9) Time taken to `rx_pll_locked` goes high from `rx_analogreset` de-assertion. Refer to [Figure 1–1](#).
- (10) The time in which the CDR must be kept in lock-to-reference mode after `rx_pll_locked` goes high and before `rx_locktodata` is asserted in manual mode. Refer to [Figure 1–1](#).
- (11) The time taken to recover valid data after the `rx_locktodata` signal is asserted in manual mode. Refer to [Figure 1–1](#).
- (12) The time taken to recover valid data after the `rx_freqlocked` signal goes high in automatic mode. Refer to [Figure 1–2](#).
- (13) To support data rates lower than the minimum specification through oversampling, use the CDR in LTR mode only.

Table 1-35 lists the transceiver specifications for Arria II GZ devices.

Table 1-35. Transceiver Specifications for Arria II GZ Devices (Part 1 of 5)

| Symbol/ Description | Conditions | -C3 and -I3 (1) | | | -C4 and -I4 | | | Unit |
|--|---|-----------------|---------------|------|----------------|---------------|-------|----------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Reference Clock | | | | | | | | |
| Supported I/O Standards | 1.2-V PCML, 1.5-V PCML, 2.5-V PCML, Differential LVPECL, LVDS, and HCSL | | | | | | | |
| Input frequency from REFCLK input pins | — | 50 | — | 697 | 50 | — | 637.5 | MHz |
| Phase frequency detector (CMU PLL and receiver CDR) | — | 50 | — | 325 | 50 | — | 325 | MHz |
| Absolute V_{MAX} for a REFCLK pin | — | — | — | 1.6 | — | — | 1.6 | V |
| Operational V_{MAX} for a REFCLK pin | — | — | — | 1.5 | — | — | 1.5 | V |
| Absolute V_{MIN} for a REFCLK pin | — | -0.4 | — | — | -0.4 | — | — | V |
| Rise/fall time (2) | — | — | — | 0.2 | — | — | 0.2 | UI |
| Duty cycle | — | 45 | — | 55 | 45 | — | 55 | % |
| Peak-to-peak differential input voltage | — | 200 | — | 1600 | 200 | — | 1600 | mV |
| Spread-spectrum modulating clock frequency | PCIe | 30 | — | 33 | 30 | — | 33 | kHz |
| Spread-spectrum downspread | PCIe | — | 0 to -0.5% | — | — | 0 to -0.5% | — | — |
| On-chip termination resistors | — | — | 100 | — | — | 100 | — | Ω |
| V_{ICM} (AC coupled) | — | 1100 \pm 10% | | | 1100 \pm 10% | | | mV |
| V_{ICM} (DC coupled) | HCSL I/O standard for PCIe reference clock | 250 | — | 550 | 250 | — | 550 | mV |
| Transmitter REFCLK Phase Noise | 10 Hz | — | — | -50 | — | — | -50 | dBc/Hz |
| | 100 Hz | — | — | -80 | — | — | -80 | dBc/Hz |
| | 1 KHz | — | — | -110 | — | — | -110 | dBc/Hz |
| | 10 KHz | — | — | -120 | — | — | -120 | dBc/Hz |
| | 100 KHz | — | — | -120 | — | — | -120 | dBc/Hz |
| | \geq 1 MHz | — | — | -130 | — | — | -130 | dBc/Hz |
| Transmitter REFCLK Phase Jitter (rms) for 100 MHz REFCLK (3) | 10 KHz to 20 MHz | — | — | 3 | — | — | 3 | ps |
| R_{REF} | — | — | 2000 \pm 1% | — | — | 2000 \pm 1% | — | Ω |

Table 1-35. Transceiver Specifications for Arria II GZ Devices (Part 2 of 5)

| Symbol/ Description | Conditions | -C3 and -I3 (1) | | | -C4 and -I4 | | | Unit |
|---|--|---------------------|-----|------|---------------------|-----|------|------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Transceiver Clocks | | | | | | | | |
| Calibration block clock frequency (cal_blk_clk) | — | 10 | — | 125 | 10 | — | 125 | MHz |
| fixedclk clock frequency | PCIe Receiver Detect | — | 125 | — | — | 125 | — | MHz |
| reconfig_clk clock frequency | Dynamic reconfiguration clock frequency | 2.5/ 37.5 (4) | — | 50 | 2.5/ 37.5 (4) | — | 50 | MHz |
| Delta time between reconfig_clks (5) | — | — | — | 2 | — | — | 2 | ms |
| Transceiver block minimum power-down (gxb_powerdown) pulse width | — | 1 | — | — | 1 | — | — | μs |
| Receiver | | | | | | | | |
| Supported I/O Standards | 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS | | | | | | | |
| Data rate (16) | — | 600 | — | 6375 | 600 | — | 3750 | Mbps |
| Absolute V_{MAX} for a receiver pin (6) | — | — | — | 1.6 | — | — | 1.6 | V |
| Operational V_{MAX} for a receiver pin | — | — | — | 1.5 | — | — | 1.5 | V |
| Absolute V_{MIN} for a receiver pin | — | -0.4 | — | — | -0.4 | — | — | V |
| Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) before device configuration | — | — | — | 1.6 | — | — | 1.6 | V |
| Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) after device configuration | $V_{ICM} = 0.82$ V setting | — | — | 2.7 | — | — | 2.7 | V |
| | $V_{ICM} = 1.1$ V setting (7) | — | — | 1.6 | — | — | 1.6 | V |
| Minimum differential eye opening at receiver serial input pins (8) | Data Rate = 600 Mbps to 5 Gbps Equalization = 0 DC gain = 0 dB | 100 | — | — | 165 | — | — | mV |
| | Data Rate > 5 Gbps Equalization = 0 DC gain = 0 dB | 165 | — | — | 165 | — | — | mV |
| V_{ICM} | $V_{ICM} = 0.82$ V setting | 820 ± 10% | | | 820 ± 10% | | | mV |
| | $V_{ICM} = 1.1$ V setting (7) | 1100 ± 10% | | | 1100 ± 10% | | | mV |

Table 1-35. Transceiver Specifications for Arria II GZ Devices (Part 3 of 5)

| Symbol/ Description | Conditions | -C3 and -I3 (1) | | | -C4 and -I4 | | | Unit |
|--|--|---|-----|-------|-------------|-----|-------|-----------------------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Receiver DC Coupling Support | — | For more information about receiver DC coupling support, refer to the “DC-Coupled Links” section in the <i>Transceiver Architecture for Arria II Devices</i> chapter. | | | | | | |
| Differential on-chip termination resistors | 85-Ω setting | 85 ± 20% | | | 85 ± 20% | | | Ω |
| | 100-Ω setting | 100 ± 20% | | | 100 ± 20% | | | Ω |
| | 120-Ω setting | 120 ± 20% | | | 120 ± 20% | | | Ω |
| | 150-Ω setting | 150 ± 20% | | | 150 ± 20% | | | Ω |
| Differential and common mode return loss | PCIe (Gen 1 and Gen 2), XAU1, HiGig+, CEI SR/LR, SRIO SR/LR, CPRI LV/HV, OBSAI, SATA | Compliant | | | | | | — |
| Programmable PPM detector (9) | — | ± 62.5, 100, 125, 200, 250, 300, 500, 1,000 | | | | | | ppm |
| Run length | — | — | — | 200 | — | — | 200 | UI |
| Programmable equalization | — | — | — | 16 | — | — | 16 | dB |
| t _{LTR} (10) | — | — | — | 75 | — | — | 75 | μs |
| t _{LTR_LTD_Manual} (11) | — | 15 | — | — | 15 | — | — | μs |
| t _{LTD_Manual} (12) | — | — | — | 4000 | — | — | 4000 | ns |
| t _{LTD_Auto} (13) | — | — | — | 4000 | — | — | 4000 | ns |
| Receiver CDR 3 dB Bandwidth in lock-to-data (LTD) mode | PCIe Gen1 | 2.0 - 3.5 | | | | | | MHz |
| | PCIe Gen2 | 40 - 65 | | | | | | MHz |
| | (OIF) CEI PHY at 6.375 Gbps | 20 - 35 | | | | | | MHz |
| | XAU1 | 10 - 18 | | | | | | MHz |
| | SRIO 1.25 Gbps | 10 - 18 | | | | | | MHz |
| | SRIO 2.5 Gbps | 10 - 18 | | | | | | MHz |
| | SRIO 3.125 Gbps | 6 - 10 | | | | | | MHz |
| | GIGE | 6 - 10 | | | | | | MHz |
| | SONET OC12 | 3 - 6 | | | | | | MHz |
| | SONET OC48 | 14 - 19 | | | | | | MHz |
| Receiver buffer and CDR offset cancellation time (per channel) | — | — | — | 17000 | — | — | 17000 | recon fig_ clk cycles |
| Programmable DC gain | DC Gain Setting = 0 | — | 0 | — | — | 0 | — | dB |
| | DC Gain Setting = 1 | — | 3 | — | — | 3 | — | dB |
| | DC Gain Setting = 2 | — | 6 | — | — | 6 | — | dB |

Table 1-35. Transceiver Specifications for Arria II GZ Devices (Part 4 of 5)

| Symbol/ Description | Conditions | -C3 and -I3 (1) | | | -C4 and -I4 | | | Unit |
|---|---|-----------------|-----|------|-------------|-----|------|------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Transmitter | | | | | | | | |
| Supported I/O Standards | 1.5-V PCML | | | | | | | |
| Data rate (14) | — | 600 | — | 6375 | 600 | — | 3750 | Mbps |
| V _{OCM} | 0.65 V setting | — | 650 | — | — | 650 | — | mV |
| Differential on-chip termination resistors | 85-Ω setting | 85 ± 15% | | | 85 ± 15% | | | Ω |
| | 100-Ω setting | 100 ± 15% | | | 100 ± 15% | | | Ω |
| | 120-Ω setting | 120 ± 15% | | | 120 ± 15% | | | Ω |
| | 150-Ω setting | 150 ± 15% | | | 150 ± 15% | | | Ω |
| Differential and common mode return loss | PCIe Gen1 and Gen2 (TX V _{OD} =4), XAUI (TX V _{OD} =6), HiGig+ (TX V _{OD} =6), CEI SR/LR (TX V _{OD} =8), SRIO SR (V _{OD} =6), SRIO LR (V _{OD} =8), CPRI LV (V _{OD} =6), CPRI HV (V _{OD} =2), OBSAI (V _{OD} =6), SATA (V _{OD} =4), | Compliant | | | | | | — |
| Rise time (15) | — | 50 | — | 200 | 50 | — | 200 | ps |
| Fall time (15) | — | 50 | — | 200 | 50 | — | 200 | ps |
| Intra-differential pair skew | — | — | — | 15 | — | — | 15 | ps |
| Intra-transceiver block transmitter channel-to-channel skew | ×4 PMA and PCS bonded mode Example: XAUI, PCIe ×4, Basic ×4 | — | — | 120 | — | — | 120 | ps |
| Inter-transceiver block transmitter channel-to-channel skew | ×8 PMA and PCS bonded mode Example: PCIe ×8, Basic ×8 | — | — | 500 | — | — | 500 | ps |
| CMUO PLL and CMU1 PLL | | | | | | | | |
| Supported Data Range | — | 600 | — | 6375 | 600 | — | 3750 | Mbps |
| pll_powerdown minimum pulse width (t _{pll_powerdown}) | — | 1 | | | 1 | | | μs |
| CMU PLL lock time from pll_powerdown de-assertion | — | — | — | 100 | — | — | 100 | μs |

Table 1-35. Transceiver Specifications for Arria II GZ Devices (Part 5 of 5)

| Symbol/ Description | Conditions | -C3 and -I3 (1) | | | -C4 and -I4 | | | Unit |
|--|-----------------------------|--------------------------------------|-----|-----|-------------|-----|-----|------|
| | | Min | Typ | Max | Min | Typ | Max | |
| -3 dB Bandwidth | PCIe Gen1 | 2.5 - 3.5 | | | | | | MHz |
| | PCIe Gen2 | 6 - 8 | | | | | | MHz |
| | (OIF) CEI PHY at 4.976 Gbps | 7 - 11 | | | | | | MHz |
| | (OIF) CEI PHY at 6.375 Gbps | 5 - 10 | | | | | | MHz |
| | XAUI | 2 - 4 | | | | | | MHz |
| | SRIO 1.25 Gbps | 3 - 5.5 | | | | | | MHz |
| | SRIO 2.5 Gbps | 3 - 5.5 | | | | | | MHz |
| | SRIO 3.125 Gbps | 2 - 4 | | | | | | MHz |
| | GIGE | 2.5 - 4.5 | | | | | | MHz |
| | SONET OC12 | 1.5 - 2.5 | | | | | | MHz |
| SONET OC48 | 3.5 - 6 | | | | | | MHz | |
| Transceiver-FPGA Fabric Interface | | | | | | | | |
| Interface speed | — | 25 | — | 325 | 25 | — | 250 | MHz |
| Digital reset pulse width | — | Minimum is two parallel clock cycles | | | | | | — |

Notes to Table 1-35:

- (1) The 3x speed grade is the fastest speed grade offered in the following Arria II GZ devices: EP2AGZ225, EP2AGZ300, and EP2AGZ350.
- (2) The rise and fall time transition is specified from 20% to 80%.
- (3) To calculate the REFCLK rms phase jitter requirement at reference clock frequencies other than 100 MHz, use the following formula:
REFCLK rms phase jitter at f (MHz) = REFCLK rms phase jitter at 100 MHz * 100/f.
- (4) The minimum `reconfig_clk` frequency is 2.5 MHz if the transceiver channel is configured in **Transmitter only** mode. The minimum `reconfig_clk` frequency is 37.5 MHz if the transceiver channel is configured in **Receiver only** or **Receiver and Transmitter** mode.
- (5) If your design uses more than one dynamic reconfiguration controller (`altgx_reconfig`) instances to control the transceiver (`altgx`) channels physically located on the same side of the device AND if you use different `reconfig_clk` sources for these `altgx_reconfig` instances, the delta time between any two of these `reconfig_clk` sources becoming stable must not exceed the maximum specification listed.
- (6) The device cannot tolerate prolonged operation at this absolute maximum.
- (7) You must use the 1.1-V RX V_{ICM} setting if the input serial data standard is LVDS.
- (8) The differential eye opening specification at the receiver input pins assumes that Receiver Equalization is disabled. If you enable Receiver Equalization, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level. Use H-Spice simulation to derive the minimum eye opening requirement with Receiver Equalization enabled.
- (9) The rate matcher supports only up to ± 300 ppm.
- (10) Time taken to `rx_pll_locked` goes high from `rx_analogreset` de-assertion. Refer to [Figure 1-1 on page 1-33](#).
- (11) Time for which the CDR must be kept in lock-to-reference mode after `rx_pll_locked` goes high and before `rx_locktodata` is asserted in manual mode. Refer to [Figure 1-1 on page 1-33](#).
- (12) Time taken to recover valid data after the `rx_locktodata` signal is asserted in manual mode. Refer to [Figure 1-1 on page 1-33](#).
- (13) Time taken to recover valid data after the `rx_freqlocked` signal goes high in automatic mode. Refer to [Figure 1-2 on page 1-33](#).
- (14) A GPLL may be required to meet the PMA-FPGA fabric interface timing above certain data rates. For more information, refer to the [Transceiver Clocking for Arria II Devices](#) chapter.
- (15) The Quartus II software automatically selects the appropriate slew rate depending on the configured data rate or functional mode.
- (16) To support data rates lower than the minimum specification through oversampling, use the CDR in LTR mode only.

Figure 1-1 shows the lock time parameters in manual mode.

 LTD = lock-to-data. LTR = lock-to-reference.

Figure 1-1. Lock Time Parameters for Manual Mode



Figure 1-2 shows the lock time parameters in automatic mode.

Figure 1-2. Lock Time Parameters for Automatic Mode



Figure 1-3 shows the differential receiver input waveform.

Figure 1-3. Receiver Input Waveform

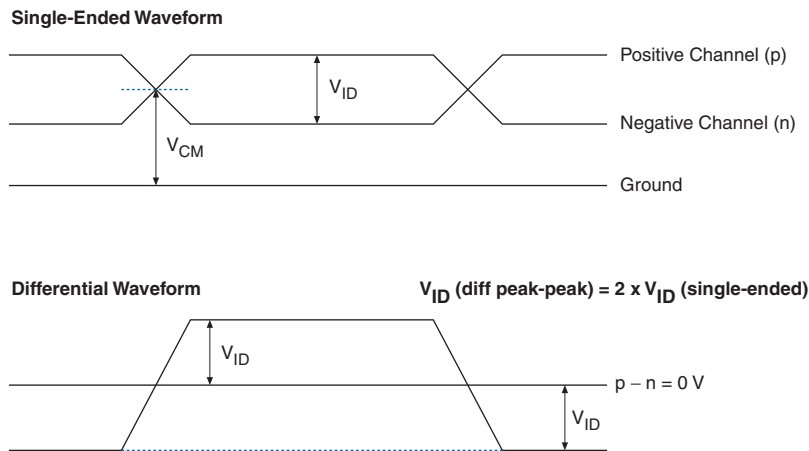


Figure 1-4 shows the transmitter output waveform.

Figure 1-4. Transmitter Output Waveform

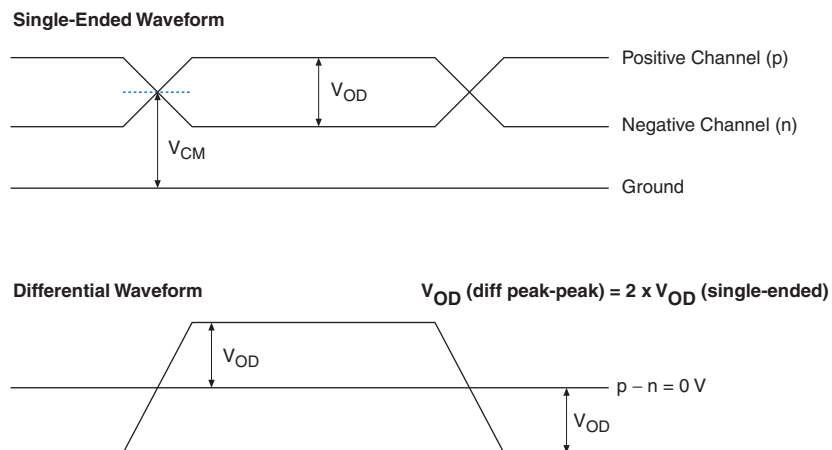


Table 1-36 lists the typical V_{OD} for TX term that equals 85Ω for Arria II GZ devices.

Table 1-36. Typical V_{OD} Setting, TX Term = 85Ω for Arria II GZ Devices

| Symbol | V_{OD} Setting (mV) | | | | | | | |
|---|-----------------------|----------------|----------------|----------------|----------------|----------------|----------------|-----------------|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| V_{OD} differential peak-to-peak Typical (mV) | $170 \pm 20\%$ | $340 \pm 20\%$ | $510 \pm 20\%$ | $595 \pm 20\%$ | $680 \pm 20\%$ | $765 \pm 20\%$ | $850 \pm 20\%$ | $1020 \pm 20\%$ |

Table 1–37 lists the typical V_{OD} for TX term that equals $100\ \Omega$ for Arria II GX and GZ devices.

Table 1–37. Typical V_{OD} Setting, TX Termination = $100\ \Omega$ for Arria II Devices

| Quartus II Setting | V_{OD} Setting (mV) |
|--------------------|-----------------------|
| 1 | 400 |
| 2 | 600 |
| 3 (Arria II GZ) | 700 |
| 4 | 800 |
| 5 | 900 |
| 6 | 1000 |
| 7 | 1200 |

Table 1–38 lists the typical transmitter pre-emphasis levels in dB for the first post tap under the following conditions: low-frequency data pattern (five 1s and five 0s) at 6.375 Gbps. The levels listed in Table 1–38 are a representation of possible pre-emphasis levels under these specified conditions only, the pre-emphasis levels may change with data pattern and data rate.

To predict the pre-emphasis level for your specific data rate and pattern, run simulations using the Arria II GX HSSI HSPICE models.

Table 1–38. Transmitter Pre-Emphasis Levels for Arria II GX Devices

| Arria II GX (Quartus II Software) First Post Tap Setting | Arria II GX (Quartus II Software) VOD Setting | | | | | | |
|--|---|-----|-----|-----|-----|-----|------|
| | 1 | 2 | 4 | 5 | 6 | 7 | Unit |
| 0 (off) | 0 | 0 | 0 | 0 | 0 | 0 | — |
| 1 | 0.7 | 0 | 0 | 0 | 0 | 0 | dB |
| 2 | 2.7 | 1.2 | 0.3 | 0 | 0 | 0 | dB |
| 3 | 4.9 | 2.4 | 1.2 | 0.8 | 0.5 | 0.2 | dB |
| 4 | 7.5 | 3.8 | 2.1 | 1.6 | 1.2 | 0.6 | dB |
| 5 | — | 5.3 | 3.1 | 2.4 | 1.8 | 1.1 | dB |
| 6 | — | 7 | 4.3 | 3.3 | 2.7 | 1.7 | dB |

Table 1-39 lists typical transmitter pre-emphasis levels for Arria II GZ devices (in dB) for the first post tap under the following conditions (low-frequency data pattern [five 1s and five 0s] at 6.25 Gbps). The levels listed in Table 1-39 are a representation of possible pre-emphasis levels under the specified conditions only and that the pre-emphasis levels may change with data pattern and data rate.

 To predict the pre-emphasis level for your specific data rate and pattern, run simulations using the [Arria II HSSI HSPICE](#) models.

Table 1-39. Transmitter Pre-Emphasis Levels for Arria II GZ Devices (Part 1 of 2)

| Pre-Emphasis 1st Post-Tap Setting | V _{DD} Setting | | | | | | | |
|--|-------------------------|-----|------|------|-----|-----|-----|-----|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | N/A | 0.7 | 0 | 0 | 0 | 0 | 0 | 0 |
| 2 | N/A | 1 | 0.3 | 0 | 0 | 0 | 0 | 0 |
| 3 | N/A | 1.5 | 0.6 | 0 | 0 | 0 | 0 | 0 |
| 4 | N/A | 2 | 0.7 | 0.3 | 0 | 0 | 0 | 0 |
| 5 | N/A | 2.7 | 1.2 | 0.5 | 0.3 | 0 | 0 | 0 |
| 6 | N/A | 3.1 | 1.3 | 0.8 | 0.5 | 0.2 | 0 | 0 |
| 7 | N/A | 3.7 | 1.8 | 1.1 | 0.7 | 0.4 | 0.2 | 0 |
| 8 | N/A | 4.2 | 2.1 | 1.3 | 0.9 | 0.6 | 0.3 | 0 |
| 9 | N/A | 4.9 | 2.4 | 1.6 | 1.2 | 0.8 | 0.5 | 0.2 |
| 10 | N/A | 5.4 | 2.8 | 1.9 | 1.4 | 1 | 0.7 | 0.3 |
| 11 | N/A | 6 | 3.2 | 2.2 | 1.7 | 1.2 | 0.9 | 0.4 |
| 12 | N/A | 6.8 | 3.5 | 2.6 | 1.9 | 1.4 | 1.1 | 0.6 |
| 13 | N/A | 7.5 | 3.8 | 2.8 | 2.1 | 1.6 | 1.2 | 0.6 |
| 14 | N/A | 8.1 | 4.2 | 3.1 | 2.3 | 1.7 | 1.3 | 0.7 |
| 15 | N/A | 8.8 | 4.5 | 3.4 | 2.6 | 1.9 | 1.5 | 0.8 |
| 16 | N/A | N/A | 4.9 | 3.7 | 2.9 | 2.2 | 1.7 | 0.9 |
| 17 | N/A | N/A | 5.3 | 4 | 3.1 | 2.4 | 1.8 | 1.1 |
| 18 | N/A | N/A | 5.7 | 4.4 | 3.4 | 2.6 | 2 | 1.2 |
| 19 | N/A | N/A | 6.1 | 4.7 | 3.6 | 2.8 | 2.2 | 1.4 |
| 20 | N/A | N/A | 6.6 | 5.1 | 4 | 3.1 | 2.4 | 1.5 |
| 21 | N/A | N/A | 7 | 5.4 | 4.3 | 3.3 | 2.7 | 1.7 |
| 22 | N/A | N/A | 8 | 6.1 | 4.8 | 3.8 | 3 | 2 |
| 23 | N/A | N/A | 9 | 6.8 | 5.4 | 4.3 | 3.4 | 2.3 |
| 24 | N/A | N/A | 10 | 7.6 | 6 | 4.8 | 3.9 | 2.6 |
| 25 | N/A | N/A | 11.4 | 8.4 | 6.8 | 5.4 | 4.4 | 3 |
| 26 | N/A | N/A | 12.6 | 9.4 | 7.4 | 5.9 | 4.9 | 3.3 |
| 27 | N/A | N/A | N/A | 10.3 | 8.1 | 6.4 | 5.3 | 3.6 |
| 28 | N/A | N/A | N/A | 11.3 | 8.8 | 7.1 | 5.8 | 4 |

Table 1–39. Transmitter Pre-Emphasis Levels for Arria II GZ Devices (Part 2 of 2)

| Pre-Emphasis 1st Post-Tap Setting | V ₀₀ Setting | | | | | | | |
|--|-------------------------|-----|-----|------|------|-----|-----|-----|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| 29 | N/A | N/A | N/A | 12.5 | 9.6 | 7.7 | 6.3 | 4.3 |
| 30 | N/A | N/A | N/A | N/A | 11.4 | 9 | 7.4 | N/A |
| 31 | N/A | N/A | N/A | N/A | 12.9 | 10 | 8.2 | N/A |

Table 1–40 lists the transceiver jitter specifications for all supported protocols for Arria II GX devices.

Table 1–40. Transceiver Block Jitter Specifications for Arria II GX Devices (Note 1) (Part 1 of 10)

| Symbol/ Description | Conditions | I3 | | | C4 | | | C5, I5 | | | C6 | | | Unit |
|---|---|--------|-----|------|--------|-----|------|--------|-----|------|--------|-----|------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| SONET/SDH Transmit Jitter Generation (2) | | | | | | | | | | | | | | |
| Peak-to-peak jitter at 622.08 Mbps | Pattern = PRBS15 | — | — | 0.1 | — | — | 0.1 | — | — | 0.1 | — | — | 0.1 | UI |
| RMS jitter at 622.08 Mbps | Pattern = PRBS15 | — | — | 0.01 | — | — | 0.01 | — | — | 0.01 | — | — | 0.01 | UI |
| Peak-to-peak jitter at 2488.32 Mbps | Pattern = PRBS15 | — | — | 0.1 | — | — | 0.1 | — | — | 0.1 | — | — | 0.1 | UI |
| RMS jitter at 2488.32 Mbps | Pattern = PRBS15 | — | — | 0.01 | — | — | 0.01 | — | — | 0.01 | — | — | 0.01 | UI |
| SONET/SDH Receiver Jitter Tolerance (2) | | | | | | | | | | | | | | |
| Jitter tolerance at 622.08 Mbps | Jitter frequency = 0.03 KHz Pattern = PRBS15 | > 15 | | | > 15 | | | > 15 | | | > 15 | | | UI |
| | Jitter frequency = 25 KHZ Pattern = PRBS15 | > 1.5 | | | > 1.5 | | | > 1.5 | | | > 1.5 | | | UI |
| | Jitter frequency = 250 KHz Pattern = PRBS15 | > 0.15 | | | > 0.15 | | | > 0.15 | | | > 0.15 | | | UI |

Table 1-40. Transceiver Block Jitter Specifications for Arria II GX Devices (Note 1) (Part 2 of 10)

| Symbol/ Description | Conditions | I3 | | | C4 | | | C5, I5 | | | C6 | | | Unit |
|--|--|--------|-----|------|--------|-----|------|--------|-----|------|--------|-----|------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Jitter tolerance at 2488.32 Mbps | Jitter frequency = 0.06 KHz Pattern = PRBS15 | > 15 | | | > 15 | | | > 15 | | | > 15 | | | UI |
| | Jitter frequency = 100 KHz Pattern = PRBS15 | > 1.5 | | | > 1.5 | | | > 1.5 | | | > 1.5 | | | UI |
| | Jitter frequency = 1 MHz Pattern = PRBS15 | > 0.15 | | | > 0.15 | | | > 0.15 | | | > 0.15 | | | UI |
| | Jitter frequency = 10 MHz Pattern = PRBS15 | > 0.15 | | | > 0.15 | | | > 0.15 | | | > 0.15 | | | UI |
| XAUI Transmit Jitter Generation (3) | | | | | | | | | | | | | | |
| Total jitter at 3.125 Gbps | Pattern = CJPAT | — | — | 0.3 | — | — | 0.3 | — | — | 0.3 | — | — | 0.3 | UI |
| Deterministic jitter at 3.125 Gbps | Pattern = CJPAT | — | — | 0.17 | — | — | 0.17 | — | — | 0.17 | — | — | 0.17 | UI |
| XAUI Receiver Jitter Tolerance (3) | | | | | | | | | | | | | | |
| Total jitter | — | > 0.65 | | | > 0.65 | | | > 0.65 | | | > 0.65 | | | UI |
| Deterministic jitter | — | > 0.37 | | | > 0.37 | | | > 0.37 | | | > 0.37 | | | UI |
| Peak-to-peak jitter | Jitter frequency = 22.1 KHz | > 8.5 | | | > 8.5 | | | > 8.5 | | | > 8.5 | | | UI |
| Peak-to-peak jitter | Jitter frequency = 1.875 MHz | > 0.1 | | | > 0.1 | | | > 0.1 | | | > 0.1 | | | UI |
| Peak-to-peak jitter | Jitter frequency = 20 MHz | > 0.1 | | | > 0.1 | | | > 0.1 | | | > 0.1 | | | UI |
| PCIe Transmit Jitter Generation (4) | | | | | | | | | | | | | | |
| Total jitter at 2.5 Gbps (Gen1) | Compliance pattern | — | — | 0.25 | — | — | 0.25 | — | — | 0.25 | — | — | 0.25 | UI |

Table 1–40. Transceiver Block Jitter Specifications for Arria II GX Devices (Note 1) (Part 3 of 10)

| Symbol/ Description | Conditions | I3 | | | C4 | | | C5, I5 | | | C6 | | | Unit |
|---|--|--------|-----|------|--------|-----|------|--------|-----|------|--------|-----|------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| PCIe Receiver Jitter Tolerance (4) | | | | | | | | | | | | | | |
| Total jitter at 2.5 Gbps (Gen1) | Compliance pattern | > 0.6 | | | > 0.6 | | | > 0.6 | | | > 0.6 | | | UI |
| PCIe (Gen 1) Electrical Idle Detect Threshold (9) | | | | | | | | | | | | | | |
| VRX-IDLE-DETDIFF (p-p) | Compliance pattern | 65 | — | 175 | 65 | — | 175 | 65 | — | 175 | 65 | — | 175 | mV |
| Serial RapidIO® (SRIO) Transmit Jitter Generation (5) | | | | | | | | | | | | | | |
| Deterministic jitter (peak-to-peak) | Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT | — | — | 0.17 | — | — | 0.17 | — | — | 0.17 | — | — | 0.17 | UI |
| Total jitter (peak-to-peak) | Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT | — | — | 0.35 | — | — | 0.35 | — | — | 0.35 | — | — | 0.35 | UI |
| SRIO Receiver Jitter Tolerance (5) | | | | | | | | | | | | | | |
| Deterministic jitter tolerance (peak-to-peak) | Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT | > 0.37 | | | > 0.37 | | | > 0.37 | | | > 0.37 | | | UI |
| Combined deterministic and random jitter tolerance (peak-to-peak) | Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT | > 0.55 | | | > 0.55 | | | > 0.55 | | | > 0.55 | | | UI |
| Sinusoidal jitter tolerance (peak-to-peak) | Jitter frequency = 22.1 KHz Data rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT | > 8.5 | | | > 8.5 | | | > 8.5 | | | > 8.5 | | | UI |
| | Jitter frequency = 1.875 MHz Data rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT | > 0.1 | | | > 0.1 | | | > 0.1 | | | > 0.1 | | | UI |
| | Jitter frequency = 20 MHz Data rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT | > 0.1 | | | > 0.1 | | | > 0.1 | | | > 0.1 | | | UI |
| GIGE Transmit Jitter Generation (6) | | | | | | | | | | | | | | |
| Deterministic jitter (peak-to-peak) | Pattern = CRPAT | — | — | 0.14 | — | — | 0.14 | — | — | 0.14 | — | — | 0.14 | UI |

Table 1-40. Transceiver Block Jitter Specifications for Arria II GX Devices (Note 1) (Part 4 of 10)

| Symbol/ Description | Conditions | I3 | | | C4 | | | C5, I5 | | | C6 | | | Unit |
|---|---|--------|-----|-----------|--------|-----|-------|--------|-----|-------|--------|-----|-------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Total jitter (peak-to-peak) | Pattern = CRPAT | — | — | 0.27 9 | — | — | 0.279 | — | — | 0.279 | — | — | 0.279 | UI |
| GIGE Receiver Jitter Tolerance (6) | | | | | | | | | | | | | | |
| Deterministic jitter tolerance (peak-to-peak) | Pattern = CJPAT | > 0.4 | | | > 0.4 | | | > 0.4 | | | > 0.4 | | | UI |
| Combined deterministic and random jitter tolerance (peak-to-peak) | Pattern = CJPAT | > 0.66 | | | > 0.66 | | | > 0.66 | | | > 0.66 | | | UI |
| HiGig Transmit Jitter Generation (7) | | | | | | | | | | | | | | |
| Deterministic jitter (peak-to-peak) | Data rate = 3.75 Gbps Pattern = CJPAT | — | — | 0.17 | — | — | 0.17 | — | — | — | — | — | — | UI |
| Total jitter (peak-to-peak) | Data rate = 3.75 Gbps Pattern = CJPAT | — | — | 0.35 | — | — | 0.35 | — | — | — | — | — | — | UI |
| HiGig Receiver Jitter Tolerance (7) | | | | | | | | | | | | | | |
| Deterministic jitter tolerance (peak-to-peak) | Data rate = 3.75 Gbps Pattern = CJPAT | > 0.37 | | | > 0.37 | | | — | — | — | — | — | — | UI |
| Combined deterministic and random jitter tolerance (peak-to-peak) | Data rate = 3.75 Gbps Pattern = CJPAT | > 0.65 | | | > 0.65 | | | — | — | — | — | — | — | UI |
| Sinusoidal jitter tolerance (peak-to-peak) | Jitter frequency = 22.1 KHz Data rate = 3.75 Gbps Pattern = CJPAT | > 8.5 | | | > 8.5 | | | — | — | — | — | — | — | UI |
| | Jitter frequency = 1.875MHz Data rate = 3.75 Gbps Pattern = CJPAT | > 0.1 | | | > 0.1 | | | — | — | — | — | — | — | UI |
| | Jitter frequency = 20 MHz Data rate = 3.75 Gbps Pattern = CJPAT | > 0.1 | | | > 0.1 | | | — | — | — | — | — | — | UI |

Table 1-40. Transceiver Block Jitter Specifications for Arria II GX Devices (Note 1) (Part 5 of 10)

| Symbol/ Description | Conditions | I3 | | | C4 | | | C5, I5 | | | C6 | | | Unit |
|--|--|-------|-----|-----|-------|-----|-----|--------|-----|-----|-------|-----|-----|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| SDI Transmitter Jitter Generation (8) | | | | | | | | | | | | | | |
| Alignment jitter (peak-to-peak) | Data rate = 1.485 Gbps (HD) pattern = Color Bar Low- frequency Roll-off = 100 KHz | 0.2 | — | — | 0.2 | — | — | 0.2 | — | — | 0.2 | — | — | UI |
| | Data rate = 2.97 Gbps (3G) pattern = Color bar Low- frequency Roll-off = 100 KHz | 0.3 | — | — | 0.3 | — | — | 0.3 | — | — | 0.3 | — | — | UI |
| SDI Receiver Jitter Tolerance (8) | | | | | | | | | | | | | | |
| Sinusoidal jitter tolerance (peak-to-peak) | Jitter frequency = 15 KHz Data rate = 2.97 Gbps (3G) Pattern = single line scramble color bar | > 2 | | | > 2 | | | > 2 | | | > 2 | | | UI |
| | Jitter frequency = 100 KHz Data rate = 2.97 Gbps (3G) Pattern = single line scramble color bar | > 0.3 | | | > 0.3 | | | > 0.3 | | | > 0.3 | | | UI |
| | Jitter frequency = 148.5 MHz Data rate = 2.97 Gbps (3G) Pattern = single line scramble color bar | > 0.3 | | | > 0.3 | | | > 0.3 | | | > 0.3 | | | UI |

Table 1-40. Transceiver Block Jitter Specifications for Arria II GX Devices (Note 1) (Part 6 of 10)

| Symbol/ Description | Conditions | I3 | | | C4 | | | C5, I5 | | | C6 | | | Unit |
|---|--|--------|-----|------|--------|-----|------|--------|-----|------|--------|-----|------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Sinusoidal jitter tolerance (peak-to-peak) | Jitter frequency = 20 KHz Data rate = 1.485 Gbps (HD) Pattern = 75% color bar | > 1 | | | > 1 | | | > 1 | | | > 1 | | | UI |
| | Jitter frequency = 100 KHz Data rate = 1.485 Gbps (HD) Pattern = 75% color bar | > 0.2 | | | > 0.2 | | | > 0.2 | | | > 0.2 | | | UI |
| | Jitter frequency = 148.5 MHz Data rate = 1.485 Gbps (HD) Pattern = 75% color bar | > 0.2 | | | > 0.2 | | | > 0.2 | | | > 0.2 | | | UI |
| SATA Transmit Jitter Generation (10) | | | | | | | | | | | | | | |
| Total jitter at 1.5 Gbps (G1) | Compliance pattern | — | — | 0.55 | — | — | 0.55 | — | — | 0.55 | — | — | 0.55 | UI |
| Deterministic jitter at 1.5 Gbps (G1) | Compliance pattern | — | — | 0.35 | — | — | 0.35 | — | — | 0.35 | — | — | 0.35 | UI |
| Total jitter at 3.0 Gbps (G2) | Compliance pattern | — | — | 0.55 | — | — | 0.55 | — | — | 0.55 | — | — | 0.55 | UI |
| Deterministic jitter at 3.0 Gbps (G2) | Compliance pattern | — | — | 0.35 | — | — | 0.35 | — | — | 0.35 | — | — | 0.35 | UI |
| Total jitter at 6.0 Gbps (G3) | Compliance pattern | — | — | 0.52 | — | — | — | — | — | — | — | — | — | UI |
| Random jitter at 6.0 Gbps (G3) | Compliance pattern | — | — | 0.18 | — | — | — | — | — | — | — | — | — | UI |
| SATA Receiver Jitter Tolerance (10) | | | | | | | | | | | | | | |
| Total jitter tolerance at 1.5 Gbps (G1) | Compliance pattern | > 0.65 | | | > 0.65 | | | > 0.65 | | | > 0.65 | | | UI |
| Deterministic jitter tolerance at 1.5 Gbps (G1) | Compliance pattern | > 0.35 | | | > 0.35 | | | > 0.35 | | | > 0.35 | | | UI |
| SSC modulation frequency at 1.5 Gbps (G1) | Compliance pattern | 33 | | | 33 | | | 33 | | | 33 | | | kHz |

Table 1–40. Transceiver Block Jitter Specifications for Arria II GX Devices (Note 1) (Part 7 of 10)

| Symbol/ Description | Conditions | I3 | | | C4 | | | C5, I5 | | | C6 | | | Unit |
|---|--------------------|--------|-----|-----|--------|-----|-----|--------|-----|-----|--------|-----|-----|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| SSC modulation deviation at 1.5 Gbps (G1) | Compliance pattern | 5700 | | | 5700 | | | 5700 | | | 5700 | | | ppm |
| RX differential skew at 1.5 Gbps (G1) | Compliance pattern | 80 | | | 80 | | | 80 | | | 80 | | | ps |
| RX AC common mode voltage at 1.5 Gbps (G1) | Compliance pattern | 150 | | | 150 | | | 150 | | | 150 | | | mV |
| Total jitter tolerance at 3.0 Gbps (G2) | Compliance pattern | > 0.65 | | | > 0.65 | | | > 0.65 | | | > 0.65 | | | UI |
| Deterministic jitter tolerance at 3.0 Gbps (G2) | Compliance pattern | > 0.35 | | | > 0.35 | | | > 0.35 | | | > 0.35 | | | UI |
| SSC modulation frequency at 3.0 Gbps (G2) | Compliance pattern | 33 | | | 33 | | | 33 | | | 33 | | | kHz |
| SSC modulation deviation at 3.0 Gbps (G2) | Compliance pattern | 5700 | | | 5700 | | | 5700 | | | 5700 | | | ppm |
| RX differential skew at 3.0 Gbps (G2) | Compliance pattern | 75 | | | 75 | | | 75 | | | 75 | | | ps |
| RX AC common mode voltage at 3.0 Gbps (G2) | Compliance pattern | 150 | | | 150 | | | 150 | | | 150 | | | mV |
| Total jitter tolerance at 6.0 Gbps (G3) | Compliance pattern | > 0.60 | | | > 0.60 | | | > 0.60 | | | > 0.60 | | | UI |
| Random jitter tolerance at 6.0 Gbps (G3) | Compliance pattern | > 0.18 | | | > 0.18 | | | > 0.18 | | | > 0.18 | | | UI |
| SSC modulation frequency at 6.0 Gbps (G3) | Compliance pattern | 33 | | | 33 | | | 33 | | | 33 | | | kHz |
| SSC modulation deviation at 6.0 Gbps (G3) | Compliance pattern | 5700 | | | 5700 | | | 5700 | | | 5700 | | | ppm |
| RX differential skew at 6.0 Gbps (G3) | Compliance pattern | 30 | | | 30 | | | 30 | | | 30 | | | ps |
| RX AC common mode voltage at 6.0 Gbps (G3) | Compliance pattern | 100 | | | 100 | | | 100 | | | 100 | | | mV |

Table 1-40. Transceiver Block Jitter Specifications for Arria II GX Devices (Note 1) (Part 8 of 10)

| Symbol/ Description | Conditions | I3 | | | C4 | | | C5, I5 | | | C6 | | | Unit |
|--|--|--------|-----|-------|--------|-----|-------|--------|-----|-------|--------|-----|-------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| CPRI Transmit Jitter Generation (11) | | | | | | | | | | | | | | |
| Total jitter | E.6.HV, E.12.HV Pattern = CJPAT | — | — | 0.279 | — | — | 0.279 | — | — | 0.279 | — | — | 0.279 | UI |
| | E.6.LV, E.12.LV, E.24.LV, E.30.LV Pattern = CJTPAT | — | — | 0.35 | — | — | 0.35 | — | — | 0.35 | — | — | 0.35 | UI |
| Deterministic jitter | E.6.HV, E.12.HV Pattern = CJPAT | — | — | 0.14 | — | — | 0.14 | — | — | 0.14 | — | — | 0.14 | UI |
| | E.6.LV, E.12.LV, E.24.LV, E.30.LV Pattern = CJTPAT | — | — | 0.17 | — | — | 0.17 | — | — | 0.17 | — | — | 0.17 | UI |
| CPRI Receiver Jitter Tolerance (11) | | | | | | | | | | | | | | |
| Total jitter tolerance | E.6.HV, E.12.HV Pattern = CJPAT | > 0.66 | | | > 0.66 | | | > 0.66 | | | > 0.66 | | | UI |
| Deterministic jitter tolerance | E.6.HV, E.12.HV Pattern = CJPAT | > 0.4 | | | > 0.4 | | | > 0.4 | | | > 0.4 | | | UI |
| Total jitter tolerance | E.6.LV, E.12.LV, E.24.LV, E.30.LV Pattern = CJTPAT | > 0.65 | | | > 0.65 | | | > 0.65 | | | > 0.65 | | | UI |
| | E.60.LV Pattern = PRBS31 | > 0.6 | | | — | | | — | | | — | | | UI |
| Deterministic jitter tolerance | E.6.LV, E.12.LV, E.24.LV, E.30.LV Pattern = CJTPAT | > 0.37 | | | > 0.37 | | | > 0.37 | | | > 0.37 | | | UI |
| | E.60.LV Pattern = PRBS31 | > 0.45 | | | — | | | — | | | — | | | UI |
| Combined deterministic and random jitter tolerance | E.6.LV, E.12.LV, E.24.LV, E.30.LV Pattern = CJTPAT | > 0.55 | | | > 0.55 | | | > 0.55 | | | > 0.55 | | | UI |
| OBSAI Transmit Jitter Generation (12) | | | | | | | | | | | | | | |
| Total jitter at 768 Mbps, 1536 Mbps, and 3072 Mbps | REFCLK = 153.6 MHz Pattern = CJPAT | — | — | 0.35 | — | — | 0.35 | — | — | 0.35 | — | — | 0.35 | UI |
| Deterministic jitter at 768 Mbps, 1536 Mbps, and 3072 Mbps | REFCLK = 153.6 MHz Pattern = CJPAT | — | — | 0.17 | — | — | 0.17 | — | — | 0.17 | — | — | 0.17 | UI |

Table 1-40. Transceiver Block Jitter Specifications for Arria II GX Devices (Note 1) (Part 9 of 10)

| Symbol/ Description | Conditions | I3 | | | C4 | | | C5, I5 | | | C6 | | | Unit |
|--|---|--------|-----|-----|--------|-----|-----|--------|-----|-----|--------|-----|-----|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| OBSAI Receiver Jitter Tolerance (12) | | | | | | | | | | | | | | |
| Deterministic jitter tolerance at 768 Mbps, 1536 Mbps, and 3072 Mbps | Pattern = CJPAT | > 0.37 | | | > 0.37 | | | > 0.37 | | | > 0.37 | | | UI |
| Combined deterministic and random jitter tolerance at 768 Mbps, 1536 Mbps, and 3072 Mbps | Pattern = CJPAT | > 0.55 | | | > 0.55 | | | > 0.55 | | | > 0.55 | | | UI |
| Sinusoidal jitter tolerance at 768 Mbps | Jitter frequency = 5.4 KHz Pattern = CJPAT | > 8.5 | | | > 8.5 | | | > 8.5 | | | > 8.5 | | | UI |
| | Jitter frequency = 460.8 KHz to 20 MHz Pattern = CJPAT | > 0.1 | | | > 0.1 | | | > 0.1 | | | > 0.1 | | | UI |
| Sinusoidal jitter tolerance at 1536 Mbps | Jitter frequency = 10.9 KHz Pattern = CJPAT | > 8.5 | | | > 8.5 | | | > 8.5 | | | > 8.5 | | | UI |
| | Jitter frequency = 921.6 KHz to 20 MHz Pattern = CJPAT | > 0.1 | | | > 0.1 | | | > 0.1 | | | > 0.1 | | | UI |

Table 1-40. Transceiver Block Jitter Specifications for Arria II GX Devices (Note 1) (Part 10 of 10)

| Symbol/ Description | Conditions | I3 | | | C4 | | | C5, I5 | | | C6 | | | Unit |
|--|--|-------|-----|-----|-------|-----|-----|--------|-----|-----|-------|-----|-----|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Sinusoidal jitter tolerance at 3072 Mbps | Jitter frequency = 21.8 KHz Pattern = CJPAT | > 8.5 | | | > 8.5 | | | > 8.5 | | | > 8.5 | | | UI |
| | Jitter frequency = 1843.2 KHz to 20 MHz Pattern = CJPAT | > 0.1 | | | > 0.1 | | | > 0.1 | | | > 0.1 | | | UI |

Notes to Table 1-40:

- (1) Dedicated `refclk` pins are used to drive the input reference clocks. The jitter numbers are valid for the stated conditions only.
- (2) The jitter numbers for SONET/SDH are compliant to the GR-253-CORE Issue 3 Specification.
- (3) The jitter numbers for XAUI are compliant to the IEEE802.3ae-2002 Specification.
- (4) The jitter numbers for PCIe are compliant to the PCIe Base Specification 2.0.
- (5) The jitter numbers for SRIO are compliant to the RapidIO Specification 1.3.
- (6) The jitter numbers for GIGE are compliant to the IEEE802.3-2002 Specification.
- (7) The jitter numbers for HiGig are compliant to the IEEE802.3ae-2002 Specification.
- (8) The HD-SDI and 3G-SDI jitter numbers are compliant to the SMPTE292M and SMPTE424M Specifications.
- (9) Arria II PCIe receivers are compliant to this specification provided the VTX_CM-DC-ACTIVEIDLE-DELTA of the upstream transmitter is less than 50 mV.
- (10) The jitter numbers for Serial Advanced Technology Attachment (SATA) are compliant to the Serial ATA Revision 3.0 Specification.
- (11) The jitter numbers for Common Public Radio Interface (CPRI) are compliant to the CPRI Specification V3.0.
- (12) The jitter numbers for Open Base Station Architecture Initiative (OBSAI) are compliant to the OBSAI RP3 Specification V4.1.

Table 1-41 lists the transceiver jitter specifications for all supported protocols for Arria II GZ devices.

Table 1-41. Transceiver Block Jitter Specifications for Arria II GZ Devices (Note 1), (2) (Part 1 of 7)

| Symbol/ Description | Conditions | -C3 and -I3 | | | -C4 and -I4 | | | Unit |
|---|---|-------------|-----|------|-------------|-----|------|------|
| | | Min | Typ | Max | Min | Typ | Max | |
| SONET/SDH Transmit Jitter Generation (3) | | | | | | | | |
| Peak-to-peak jitter at 622.08 Mbps | Pattern = PRBS15 | — | — | 0.1 | — | — | 0.1 | UI |
| RMS jitter at 622.08 Mbps | Pattern = PRBS15 | — | — | 0.01 | — | — | 0.01 | UI |
| Peak-to-peak jitter at 2488.32 Mbps | Pattern = PRBS15 | — | — | 0.1 | — | — | 0.1 | UI |
| RMS jitter at 2488.32 Mbps | Pattern = PRBS15 | — | — | 0.01 | — | — | 0.01 | UI |
| SONET/SDH Receiver Jitter Tolerance (3) | | | | | | | | |
| Jitter tolerance at 622.08 Mbps | Jitter frequency = 0.03 KHz Pattern = PRBS15 | > 15 | | | > 15 | | | UI |
| | Jitter frequency = 25 KHz Pattern = PRBS15 | > 1.5 | | | > 1.5 | | | UI |
| | Jitter frequency = 250 KHz Pattern = PRBS15 | > 0.15 | | | > 0.15 | | | UI |

Table 1–41. Transceiver Block Jitter Specifications for Arria II GZ Devices (Note 1), (2) (Part 2 of 7)

| Symbol/ Description | Conditions | –C3 and –I3 | | | –C4 and –I4 | | | Unit |
|--|---|-------------|-----|------|-------------|-----|------|------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Jitter tolerance at 2488.32 Mbps | Jitter frequency = 0.06 KHz Pattern = PRBS15 | > 15 | | | > 15 | | | UI |
| | Jitter frequency = 100 KHz Pattern = PRBS15 | > 1.5 | | | > 1.5 | | | UI |
| | Jitter frequency = 1 MHz Pattern = PRBS15 | > 0.15 | | | > 0.15 | | | UI |
| | Jitter frequency = 10 MHz Pattern = PRBS15 | > 0.15 | | | > 0.15 | | | UI |
| Fibre Channel Transmit Jitter Generation (4), (5) | | | | | | | | |
| Total jitter FC-1 | Pattern = CRPAT | — | — | 0.23 | — | — | 0.23 | UI |
| Deterministic jitter FC-1 | Pattern = CRPAT | — | — | 0.11 | — | — | 0.11 | UI |
| Total jitter FC-2 | Pattern = CRPAT | — | — | 0.33 | — | — | 0.33 | UI |
| Deterministic jitter FC-2 | Pattern = CRPAT | — | — | 0.2 | — | — | 0.2 | UI |
| Total jitter FC-4 | Pattern = CRPAT | — | — | 0.52 | — | — | 0.52 | UI |
| Deterministic jitter FC-4 | Pattern = CRPAT | — | — | 0.33 | — | — | 0.33 | UI |
| Fibre Channel Receiver Jitter Tolerance (4), (6) | | | | | | | | |
| Deterministic jitter FC-1 | Pattern = CJTPAT | > 0.37 | | | > 0.37 | | | UI |
| Random jitter FC-1 | Pattern = CJTPAT | > 0.31 | | | > 0.31 | | | UI |
| Sinusoidal jitter FC-1 | Fc/25000 | > 1.5 | | | > 1.5 | | | UI |
| | Fc/1667 | > 0.1 | | | > 0.1 | | | UI |
| Deterministic jitter FC-2 | Pattern = CJTPAT | > 0.33 | | | > 0.33 | | | UI |
| Random jitter FC-2 | Pattern = CJTPAT | > 0.29 | | | > 0.29 | | | UI |
| Sinusoidal jitter FC-2 | Fc/25000 | > 1.5 | | | > 1.5 | | | UI |
| | Fc/1667 | > 0.1 | | | > 0.1 | | | UI |
| Deterministic jitter FC-4 | Pattern = CJTPAT | > 0.33 | | | > 0.33 | | | UI |
| Random jitter FC-4 | Pattern = CJTPAT | > 0.29 | | | > 0.29 | | | UI |
| Sinusoidal jitter FC-4 | Fc/25000 | > 1.5 | | | > 1.5 | | | UI |
| | Fc/1667 | > 0.1 | | | > 0.1 | | | UI |
| XAUI Transmit Jitter Generation (7) | | | | | | | | |
| Total jitter at 3.125 Gbps | Pattern = CJPAT | — | — | 0.3 | — | — | 0.3 | UI |
| Deterministic jitter at 3.125 Gbps | Pattern = CJPAT | — | — | 0.17 | — | — | 0.17 | UI |
| XAUI Receiver Jitter Tolerance (7) | | | | | | | | |
| Total jitter | — | > 0.65 | | | > 0.65 | | | UI |
| Deterministic jitter | — | > 0.37 | | | > 0.37 | | | UI |

Table 1-41. Transceiver Block Jitter Specifications for Arria II GZ Devices (Note 1), (2) (Part 3 of 7)

| Symbol/ Description | Conditions | -C3 and -I3 | | | -C4 and -I4 | | | Unit |
|--|--|---------------|-----|-------|---------------|-----|-------|------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Peak-to-peak jitter | Jitter frequency = 22.1 KHz | > 8.5 | | | > 8.5 | | | UI |
| Peak-to-peak jitter | Jitter frequency = 1.875 MHz | > 0.1 | | | > 0.1 | | | UI |
| Peak-to-peak jitter | Jitter frequency = 20 MHz | > 0.1 | | | > 0.1 | | | UI |
| PCIe Transmit Jitter Generation (8) | | | | | | | | |
| Total jitter at 2.5 Gbps (Gen1)— x1, x4, and x8 | Compliance pattern | — | — | 0.25 | — | — | 0.25 | UI |
| Total jitter at 5 Gbps (Gen2)— x1, x4, and x8 | Compliance pattern | — | — | 0.25 | — | — | — | UI |
| PCIe Receiver Jitter Tolerance (8) | | | | | | | | |
| Total jitter at 2.5 Gbps (Gen1) | Compliance pattern | > 0.6 | | | > 0.6 | | | UI |
| Total jitter at 5 Gbps (Gen2) | Compliance pattern | Not supported | | | Not supported | | | UI |
| PCIe (Gen 1) Electrical Idle Detect Threshold | | | | | | | | |
| $V_{RX-IDLE-DETDIFFp-p}$ (9) | Compliance pattern | 65 | — | 175 | 65 | — | 175 | UI |
| SRIO Transmit Jitter Generation (10) | | | | | | | | |
| Deterministic jitter (peak-to-peak) | Data rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT | — | — | 0.17 | — | — | 0.17 | UI |
| Total jitter (peak-to-peak) | Data rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT | — | — | 0.35 | — | — | 0.35 | UI |
| SRIO Receiver Jitter Tolerance (10) | | | | | | | | |
| Deterministic jitter tolerance (peak-to-peak) | Data rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT | > 0.37 | | | > 0.37 | | | UI |
| Combined deterministic and random jitter tolerance (peak-to- peak) | Data rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT | > 0.55 | | | > 0.55 | | | UI |
| Sinusoidal jitter tolerance (peak- to-peak) | Jitter frequency = 22.1 KHz Data rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT | > 8.5 | | | > 8.5 | | | UI |
| | Jitter frequency = 1.875 MHz Data rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT | > 0.1 | | | > 0.1 | | | UI |
| | Jitter frequency = 20 MHz Data rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT | > 0.1 | | | > 0.1 | | | UI |
| GIGE Transmit Jitter Generation (11) | | | | | | | | |
| Deterministic jitter (peak-to-peak) | Pattern = CRPAT | — | — | 0.14 | — | — | 0.14 | UI |
| Total jitter (peak-to-peak) | Pattern = CRPAT | — | — | 0.279 | — | — | 0.279 | UI |

Table 1-41. Transceiver Block Jitter Specifications for Arria II GZ Devices (Note 1), (2) (Part 4 of 7)

| Symbol/ Description | Conditions | -C3 and -I3 | | | -C4 and -I4 | | | Unit |
|---|---|-------------|-----|------|-------------|-----|-----|------|
| | | Min | Typ | Max | Min | Typ | Max | |
| GIGE Receiver Jitter Tolerance (11) | | | | | | | | |
| Deterministic jitter tolerance (peak-to-peak) | Pattern = CJPAT | > 0.4 | | | > 0.4 | | | UI |
| Combined deterministic and random jitter tolerance (peak-to-peak) | Pattern = CJPAT | > 0.66 | | | > 0.66 | | | UI |
| HiGig Transmit Jitter Generation | | | | | | | | |
| Deterministic jitter (peak-to-peak) | Data rate = 3.75 Gbps Pattern = CJPAT | — | — | 0.17 | — | — | — | UI |
| Total jitter (peak-to-peak) | Data rate = 3.75 Gbps Pattern = CJPAT | — | — | 0.35 | — | — | — | UI |
| HiGig Receiver Jitter Tolerance | | | | | | | | |
| Deterministic jitter tolerance (peak-to-peak) | Data rate = 3.75 Gbps Pattern = CJPAT | > 0.37 | | | — | — | — | UI |
| Combined deterministic and random jitter tolerance (peak-to-peak) | Data rate = 3.75 Gbps Pattern = CJPAT | > 0.65 | | | — | — | — | UI |
| Sinusoidal jitter tolerance (peak-to-peak) | Jitter frequency = 22.1 KHz Data rate = 3.75 Gbps Pattern = CJPAT | > 8.5 | | | — | — | — | UI |
| | Jitter frequency = 22.1 KHz Data rate = 3.75 Gbps Pattern = CJPAT | > 0.1 | | | — | — | — | UI |
| | Jitter frequency = 22.1 KHz Data rate = 3.75 Gbps Pattern = CJPAT | > 0.1 | | | — | — | — | UI |
| (OIF) CEI Transmitter Jitter Generation | | | | | | | | |
| Total jitter (peak-to-peak) | Data rate = 6.375 Gbps Pattern = PRBS15 BER = 10^{-12} | — | — | 0.3 | — | — | 0.3 | UI |
| (OIF) CEI Receiver Jitter Tolerance | | | | | | | | |
| Deterministic jitter tolerance (peak-to-peak) | Data rate = 6.375 Gbps Pattern = PRBS31 BER = 10^{-12} | > 0.675 | | | — | — | — | UI |
| Combined deterministic and random jitter tolerance (peak-to-peak) | Data rate = 6.375 Gbps Pattern = PRBS31 BER = 10^{-12} | > 0.988 | | | — | — | — | UI |

Table 1-41. Transceiver Block Jitter Specifications for Arria II GZ Devices (Note 1), (2) (Part 5 of 7)

| Symbol/ Description | Conditions | -C3 and -I3 | | | -C4 and -I4 | | | Unit |
|---|---|-------------|--------|------|-------------|-------|------|------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Sinusoidal jitter tolerance (peak-to-peak) | Jitter Frequency = 38.2 KHz Data rate = 6.375 Gbps Pattern = PRBS31 BER = 10 ⁻¹² | | > 0.5 | | — | — | — | UI |
| | Jitter Frequency = 3.82 MHz Data rate = 6.375 Gbps Pattern = PRBS31 BER = 10 ⁻¹² | | > 0.05 | | — | — | — | UI |
| | Jitter Frequency = 20 MHz Data rate = 6.375 Gbps Pattern = PRBS31 BER = 10 ⁻¹² | | > 0.05 | | — | — | — | UI |
| SDI Transmitter Jitter Generation (12) | | | | | | | | |
| Alignment jitter (peak-to-peak) | Data rate = 1.485 Gbps (HD) Pattern = color bar Low-frequency roll-off = 100 KHz | 0.2 | — | — | 0.2 | — | — | UI |
| | Data rate = 2.97 Gbps (3G) Pattern = color bar Low-frequency roll-off = 100 KHz | 0.3 | — | — | 0.3 | — | — | UI |
| SDI Receiver Jitter Tolerance (12) | | | | | | | | |
| Sinusoidal jitter tolerance (peak-to-peak) | Jitter frequency = 15 KHz Data rate = 2.97 Gbps (3G) Pattern = single line scramble color bar | | > 2 | | | > 2 | | UI |
| | Jitter frequency = 100 KHz Data rate = 2.97 Gbps (3G) Pattern = single line scramble color bar | | > 0.3 | | | > 0.3 | | UI |
| | Jitter frequency = 148.5 MHz Data rate = 2.97 Gbps (3G) Pattern = single line scramble color bar | | > 0.3 | | | > 0.3 | | UI |
| Sinusoidal jitter tolerance (peak-to-peak) | Jitter frequency = 20 KHz Data rate = 1.485 Gbps (HD) pattern = 75% color bar | | > 1 | | | > 1 | | UI |
| | Jitter frequency = 100 KHz Data rate = 1.485 Gbps (HD) Pattern = 75% color bar | | > 0.2 | | | > 0.2 | | UI |
| | Jitter frequency = 148.5 MHz Data rate = 1.485 Gbps (HD) Pattern = 75% color bar | | > 0.2 | | | > 0.2 | | UI |
| SAS Transmit Jitter Generation (13) | | | | | | | | |
| Total jitter at 1.5 Gbps (G1) | Pattern = CJPAT | — | — | 0.55 | — | — | 0.55 | UI |
| Deterministic jitter at 1.5 Gbps (G1) | Pattern = CJPAT | — | — | 0.35 | — | — | 0.35 | UI |
| Total jitter at 3.0 Gbps (G2) | Pattern = CJPAT | — | — | 0.55 | — | — | 0.55 | UI |

Table 1–41. Transceiver Block Jitter Specifications for Arria II GZ Devices (Note 1), (2) (Part 6 of 7)

| Symbol/ Description | Conditions | –C3 and –I3 | | | –C4 and –I4 | | | Unit |
|--|---|-------------|-----|-------|-------------|-----|-------|------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Deterministic jitter at 3.0 Gbps (G2) | Pattern = CJPAT | — | — | 0.35 | — | — | 0.35 | UI |
| Total jitter at 6.0 Gbps (G3) | Pattern = CJPAT | — | — | 0.25 | — | — | 0.25 | UI |
| Random jitter at 6.0 Gbps (G3) | Pattern = CJPAT | — | — | 0.15 | — | — | 0.15 | UI |
| SAS Receiver Jitter Tolerance (13) | | | | | | | | |
| Total jitter tolerance at 1.5 Gbps (G1) | Pattern = CJPAT | — | — | 0.65 | — | — | 0.65 | UI |
| Deterministic jitter tolerance at 1.5 Gbps (G1) | Pattern = CJPAT | — | — | 0.35 | — | — | 0.35 | UI |
| Sinusoidal jitter tolerance at 1.5 Gbps (G1) | Jitter frequency = 900 KHz to 5 MHz Pattern = CJTPAT BER = 1E-12 | > 0.1 | | | > 0.1 | | | UI |
| CPRI Transmit Jitter Generation (14) | | | | | | | | |
| Total jitter | E.6.HV, E.12.HV Pattern = CJPAT | — | — | 0.279 | — | — | 0.279 | UI |
| | E.6.LV, E.12.LV, E.24.LV, E.30.LV Pattern = CJPAT | — | — | 0.35 | — | — | 0.35 | UI |
| Deterministic jitter | E.6.HV, E.12.HV Pattern = CJPAT | — | — | 0.14 | — | — | 0.14 | UI |
| | E.6.LV, E.12.LV, E.24.LV, E.30.LV Pattern = CJPAT | — | — | 0.17 | — | — | 0.17 | UI |
| CPRI Receiver Jitter Tolerance (14) | | | | | | | | |
| Total jitter tolerance | E.6.HV, E.12.HV Pattern = CJPAT | > 0.66 | | | > 0.66 | | | UI |
| Deterministic jitter tolerance | E.6.HV, E.12.HV Pattern = CJPAT | > 0.4 | | | > 0.4 | | | UI |
| Total jitter tolerance | E.6.LV, E.12.LV, E.24.LV, E.30.LV Pattern = CJPAT | > 0.65 | | | > 0.65 | | | UI |
| Deterministic jitter tolerance | E.6.LV, E.12.LV, E.24.LV, E.30.LV Pattern = CJPAT | > 0.37 | | | > 0.37 | | | UI |
| Combined deterministic and random jitter tolerance | E.6.LV, E.12.LV, E.24.LV, E.30.LV Pattern = CJPAT | > 0.55 | | | > 0.55 | | | UI |
| OBSAI Transmit Jitter Generation (15) | | | | | | | | |
| Total jitter at 768 Mbps, 1536 Mbps, and 3072 Mbps | REFCLK = 153.6 MHz Pattern CJPAT | — | — | 0.35 | — | — | 0.35 | UI |
| Deterministic jitter at 768 Mbps, 1536 Mbps, and 3072 Mbps | REFCLK = 153.6 MHz Pattern CJPAT | — | — | 0.17 | — | — | 0.17 | UI |

Table 1–41. Transceiver Block Jitter Specifications for Arria II GZ Devices (Note 1), (2) (Part 7 of 7)

| Symbol/ Description | Conditions | –C3 and –I3 | | | –C4 and –I4 | | | Unit |
|--|--|-------------|-----|-----|-------------|-----|-----|------|
| | | Min | Typ | Max | Min | Typ | Max | |
| OBSAI Receiver Jitter Tolerance (15) | | | | | | | | |
| Deterministic jitter tolerance at 768 Mbps, 1536 Mbps, and 3072 Mbps | Pattern = CJPAT | > 0.37 | | | > 0.37 | | | UI |
| Combined deterministic and random jitter tolerance at 768 Mbps, 1536 Mbps, and 3072 Mbps | Pattern = CJPAT | > 0.55 | | | > 0.55 | | | UI |
| Sinusoidal jitter tolerance at 768 Mbps | Jitter frequency = 5.4 KHz Pattern = CJPAT | > 8.5 | | | > 8.5 | | | UI |
| | Jitter frequency = 460 MHz to 20 MHz Pattern = CJPAT | > 0.1 | | | > 0.1 | | | UI |
| Sinusoidal jitter tolerance at 1536 Mbps | Jitter frequency = 10.9 KHz Pattern = CJPAT | > 8.5 | | | > 8.5 | | | UI |
| | Jitter frequency = 921.6 MHz to 20 MHz Pattern = CJPAT | > 0.1 | | | > 0.1 | | | UI |
| Sinusoidal jitter tolerance at 3072 Mbps | Jitter frequency = 21.8 KHz Pattern = CJPAT | > 8.5 | | | > 8.5 | | | UI |
| | Jitter frequency = 1843.2 MHz to 20 MHz Pattern = CJPAT | > 0.1 | | | > 0.1 | | | UI |

Notes to Table 1–41:

- (1) Dedicated `refclk` pins were used to drive the input reference clocks.
- (2) The jitter numbers are valid for the stated conditions only.
- (3) The jitter numbers for SONET/SDH are compliant to the GR-253-CORE Issue 3 Specification.
- (4) The jitter numbers for Fibre Channel are compliant to the FC-PI-4 Specification revision 6.10.
- (5) The Fibre Channel transmitter jitter generation numbers are compliant to the specification at the δ_T inter operability point.
- (6) The Fibre Channel receiver jitter tolerance numbers are compliant to the specification at the δ_R interpretability point.
- (7) The jitter numbers for XAUI are compliant to the IEEE802.3ae-2002 Specification.
- (8) The jitter numbers for PCIe are compliant to the PCIe Base Specification 2.0.
- (9) Arria II GZ PCIe receivers are compliant to this specification provided the $V_{TX-CM-DC-ACTIVEIDLE-DELTA}$ of the upstream transmitter is less than 50 mV.
- (10) The jitter numbers for SRIO are compliant to the RapidIO Specification 1.3.
- (11) The jitter numbers for GIGE are compliant to the IEEE802.3-2002 Specification.
- (12) The HD-SDI and 3G-SDI jitter numbers are compliant to the SMPTE292M and SMPTE424M Specifications.
- (13) The jitter numbers for Serial Attached SCSI (SAS) are compliant to the SAS-2.1 Specification.
- (14) The jitter numbers for CPRI are compliant to the CPRI Specification V3.0.
- (15) The jitter numbers for OBSAI are compliant to the OBSAI RP3 Specification V4.1.

Core Performance Specifications for the Arria II Device Family

This section describes the clock tree, phase-locked loop (PLL), digital signal processing (DSP), embedded memory, configuration, and JTAG specifications for Arria II GX and GZ devices.

Clock Tree Specifications

Table 1-42 lists the clock tree specifications for Arria II GX devices.

Table 1-42. Clock Tree Performance for Arria II GX Devices

| Clock Network | Performance | | | Unit |
|---------------|-------------|-------|-----|------|
| | I3, C4 | C5,I5 | C6 | |
| GCLK and RCLK | 500 | 500 | 400 | MHz |
| PCLK | 420 | 350 | 280 | MHz |

Table 1-43 lists the clock tree specifications for Arria II GZ devices.

Table 1-43. Clock Tree Performance for Arria II GZ Devices

| Clock Network | Performance | | Unit |
|---------------|-------------|-------------|------|
| | -C3 and -I3 | -C4 and -I4 | |
| GCLK and RCLK | 700 | 500 | MHz |
| PCLK | 500 | 450 | MHz |

PLL Specifications

Table 1-44 lists the PLL specifications for Arria II GX devices.

Table 1-44. PLL Specifications for Arria II GX Devices (Part 1 of 3)

| Symbol | Description | Min | Typ | Max | Unit |
|----------------------|---|-----|-----|-----------|----------|
| f_{IN} | Input clock frequency (from clock input pins residing in right/top/bottom banks) (-4 Speed Grade) | 5 | — | 670 (1) | MHz |
| | Input clock frequency (from clock input pins residing in right/top/bottom banks) (-5 Speed Grade) | 5 | — | 622 (1) | MHz |
| | Input clock frequency (from clock input pins residing in right/top/bottom banks) (-6 Speed Grade) | 5 | — | 500 (1) | MHz |
| f_{INPFD} | Input frequency to the PFD | 5 | — | 325 | MHz |
| f_{VCO} | PLL VCO operating Range (2) | 600 | — | 1,400 | MHz |
| f_{INDUTY} | Input clock duty cycle | 40 | — | 60 | % |
| $f_{EINDUTY}$ | External feedback clock input duty cycle | 40 | — | 60 | % |
| t_{INCCJ} (3), (4) | Input clock cycle-to-cycle jitter (Frequency \geq 100 MHz) | — | — | 0.15 | UI (p-p) |
| | Input clock cycle-to-cycle jitter (Frequency \leq 100 MHz) | — | — | \pm 750 | ps (p-p) |

Table 1-44. PLL Specifications for Arria II GX Devices (Part 2 of 3)

| Symbol | Description | Min | Typ | Max | Unit |
|-------------------|--|-----|-----|---------|----------------|
| f_{OUT} | Output frequency for internal global or regional clock (-4 Speed Grade) | — | — | 500 | MHz |
| | Output frequency for internal global or regional clock (-5 Speed Grade) | — | — | 500 | MHz |
| | Output frequency for internal global or regional clock (-6 Speed Grade) | — | — | 400 | MHz |
| f_{OUT_EXT} | Output frequency for external clock output (-4 Speed Grade) | — | — | 670 (5) | MHz |
| | Output frequency for external clock output (-5 Speed Grade) | — | — | 622 (5) | MHz |
| | Output frequency for external clock output (-6 Speed Grade) | — | — | 500 (5) | MHz |
| $t_{OUTDUTY}$ | Duty cycle for external clock output (when set to 50%) | 45 | 50 | 55 | % |
| t_{OUTPJ_DC} | Dedicated clock output period jitter ($f_{OUT} \geq 100$ MHz) | — | — | 300 | ps (p-p) |
| | Dedicated clock output period jitter ($f_{OUT} < 100$ MHz) | — | — | 30 | mUI (p-p) |
| t_{OUTCCJ_DC} | Dedicated clock output cycle-to-cycle jitter ($f_{OUT} \geq 100$ MHz) | — | — | 300 | ps (p-p) |
| | Dedicated clock output cycle-to-cycle jitter ($f_{OUT} < 100$ MHz) | — | — | 30 | mUI (p-p) |
| f_{OUTPJ_IO} | Regular I/O clock output period jitter ($f_{OUT} \geq 100$ MHz) | — | — | 650 | ps (p-p) |
| | Regular I/O clock output period jitter ($f_{OUT} < 100$ MHz) | — | — | 65 | mUI (p-p) |
| f_{OUTCCJ_IO} | Regular I/O clock output cycle-to-cycle jitter ($f_{OUT} \geq 100$ MHz) | — | — | 650 | ps (p-p) |
| | Regular I/O clock output cycle-to-cycle jitter ($f_{OUT} < 100$ MHz) | — | — | 65 | mUI (p-p) |
| $t_{CONFIGPLL}$ | Time required to reconfigure PLL scan chains | — | 3.5 | — | SCANCLK cycles |
| $t_{CONFIGPHASE}$ | Time required to reconfigure phase shift | — | 1 | — | SCANCLK cycles |
| $f_{SCANCLK}$ | SCANCLK frequency | — | — | 100 | MHz |
| t_{LOCK} | Time required to lock from end of device configuration | — | — | 1 | ms |
| t_{DLOCK} | Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays) | — | — | 1 | ms |
| $f_{CL\ BW}$ | PLL closed-loop low bandwidth | — | 0.3 | — | MHz |
| | PLL closed-loop medium bandwidth | — | 1.5 | — | MHz |
| | PLL closed-loop high bandwidth | — | 4 | — | MHz |
| t_{PLL_PSERR} | Accuracy of PLL phase shift | — | — | ±50 | ps |
| t_{ARESET} | Minimum pulse width on <i>areset</i> signal | 10 | — | — | ns |

Table 1-44. PLL Specifications for Arria II GX Devices (Part 3 of 3)

| Symbol | Description | Min | Typ | Max | Unit |
|---|--|-----|-----|------|-----------|
| $t_{CASC_OUTJITTER_PERIOD_DEDCLK}$ (6), (7) | Period Jitter for dedicated clock output in cascaded PLLs (FOUT ≥ 100 MHz) | — | — | 425 | ps (p-p) |
| | Period Jitter for dedicated clock output in cascaded PLLs (FOUT ≤ 100 MHz) | — | — | 42.5 | mUI (p-p) |

Notes to Table 1-44:

- (1) f_{IN} is limited by the I/O f_{MAX} .
- (2) The VCO frequency reported by the Quartus II software in the PLL summary section of the compilation report takes into consideration the VCO post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the f_{VCO} specification.
- (3) A high-input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean-clock source, which is less than 200 ps.
- (4) F_{REF} is f_{IN}/N when $N = 1$.
- (5) This specification is limited by the lower of the two: I/O f_{MAX} or f_{OUT} of the PLL.
- (6) Peak-to-peak jitter with a probability level of 10^{-12} (14 sigma, 99.999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied. The external memory interface clock output jitter specifications use a different measurement method and are available in Table 1-62 on page 1-70.
- (7) The cascaded PLL specification is only applicable with the following condition:
 - a. Upstream PLL: $0.59 \text{ MHz} \leq \text{Upstream PLL BW} < 1 \text{ MHz}$
 - b. Downstream PLL: $\text{Downstream PLL BW} > 2 \text{ MHz}$

Table 1-45 lists the PLL specifications for Arria II GZ devices when operating in both the commercial junction temperature range (0° to 85°C) and the industrial junction temperature range (-40° to 100°C).

Table 1-45. PLL Specifications for Arria II GZ Devices (Part 1 of 2)

| Symbol | Parameter | Min | Typ | Max | Unit |
|-------------------|--|-----|-----|---------|----------------|
| f_{IN} | Input clock frequency (-3 speed grade) | 5 | — | 717 (1) | MHz |
| | Input clock frequency (-4 speed grade) | 5 | — | 717 (1) | MHz |
| f_{INPFD} | Input frequency to the PFD | 5 | — | 325 | MHz |
| f_{VCO} | PLL VCO operating range (-3 speed grade) | 600 | — | 1,300 | MHz |
| | PLL VCO operating range (-4 speed grade) | 600 | — | 1,300 | MHz |
| $t_{EINDUTY}$ | Input clock or external feedback clock input duty cycle | 40 | — | 60 | % |
| f_{OUT} | Output frequency for internal global or regional clock (-3 speed grade) | — | — | 700 (2) | MHz |
| | Output frequency for internal global or regional clock (-4 speed grade) | — | — | 500 (2) | MHz |
| f_{OUT_EXT} | Output frequency for external clock output (-3 speed grade) | — | — | 717 (2) | MHz |
| | Output frequency for external clock output (-4 speed grade) | — | — | 717 (2) | MHz |
| $t_{OUTDUTY}$ | Duty cycle for external clock output (when set to 50%) | 45 | 50 | 55 | % |
| t_{FCOMP} | External feedback clock compensation time | — | — | 10 | ns |
| $t_{CONFIGPLL}$ | Time required to reconfigure scan chain | — | 3.5 | — | scanclk cycles |
| $t_{CONFIGPHASE}$ | Time required to reconfigure phase shift | — | 1 | — | scanclk cycles |
| $f_{SCANCLK}$ | scanclk frequency | — | — | 100 | MHz |
| t_{LOCK} | Time required to lock from end-of-device configuration or de-assertion of areset | — | — | 1 | ms |

Table 1–45. PLL Specifications for Arria II GZ Devices (Part 2 of 2)

| Symbol | Parameter | Min | Typ | Max | Unit |
|--------------------------------|--|-----|-----|------|-----------|
| t_{DLOCK} | Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays) | — | — | 1 | ms |
| f_{CLBW} | PLL closed-loop low bandwidth | — | 0.3 | — | MHz |
| | PLL closed-loop medium bandwidth | — | 1.5 | — | MHz |
| | PLL closed-loop high bandwidth (7) | — | 4 | — | MHz |
| t_{PLL_PSERR} | Accuracy of PLL phase shift | — | — | ±50 | ps |
| t_{ARESET} | Minimum pulse width on the $areset$ signal | 10 | — | — | ns |
| t_{INCCJ} (3), (4) | Input clock cycle to cycle jitter ($F_{REF} \geq 100$ MHz) | — | — | 0.15 | UI (p-p) |
| | Input clock cycle to cycle jitter ($F_{REF} < 100$ MHz) | — | — | ±750 | ps (p-p) |
| t_{OUTPJ_DC} (5) | Period Jitter for dedicated clock output ($F_{OUT} \geq 100$ MHz) | — | — | 175 | ps (p-p) |
| | Period Jitter for dedicated clock output ($F_{OUT} < 100$ MHz) | — | — | 17.5 | mUI (p-p) |
| t_{OUTCCJ_DC} (5) | Cycle to Cycle Jitter for dedicated clock output ($F_{OUT} \geq 100$ MHz) | — | — | 175 | ps (p-p) |
| | Cycle to Cycle Jitter for dedicated clock output ($F_{OUT} < 100$ MHz) | — | — | 17.5 | mUI (p-p) |
| t_{OUTPJ_IO} (5), (8) | Period Jitter for clock output on regular I/O ($F_{OUT} \geq 100$ MHz) | — | — | 600 | ps (p-p) |
| | Period Jitter for clock output on regular I/O ($F_{OUT} < 100$ MHz) | — | — | 60 | mUI (p-p) |
| t_{OUTCCJ_IO} (5), (8) | Cycle to Cycle Jitter for clock output on regular I/O ($F_{OUT} \geq 100$ MHz) | — | — | 600 | ps (p-p) |
| | Cycle to Cycle Jitter for clock output on regular I/O ($F_{OUT} < 100$ MHz) | — | — | 60 | mUI (p-p) |
| $t_{CASC_OUTPJ_DC}$ (5), (6) | Period Jitter for dedicated clock output in cascaded PLLs ($F_{OUT} \geq 100$ MHz) | — | — | 250 | ps (p-p) |
| | Period Jitter for dedicated clock output in cascaded PLLs ($F_{OUT} < 100$ MHz) | — | — | 25 | mUI (p-p) |
| f_{DRIFT} | Frequency drift after PFDENA is disabled for duration of 100 μ s | — | — | ±10 | % |

Notes to Table 1–45:

- (1) This specification is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.
- (2) This specification is limited by the lower of the two: I/O F_{MAX} or F_{OUT} of the PLL.
- (3) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source that is less than 120 ps.
- (4) F_{REF} is f_{IN}/N when $N = 1$.
- (5) Peak-to-peak jitter with a probability level of 10^{-12} (14 sigma, 99.9999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied. The external memory interface clock output jitter specifications use a different measurement method and are available in [Table 1–64 on page 1–71](#).
- (6) The cascaded PLL specification is only applicable with the following condition:
 - a. Upstream PLL: $0.59 \text{ Mhz} \leq \text{Upstream PLL BW} < 1 \text{ MHz}$
 - b. Downstream PLL: $\text{Downstream PLL BW} > 2 \text{ MHz}$
- (7) High bandwidth PLL settings are not supported in external feedback mode.
- (8) External memory interface clock output jitter specifications use a different measurement method, which is available in [Table 1–63 on page 1–71](#).

DSP Block Specifications

Table 1-46 lists the DSP block performance specifications for Arria II GX devices.

Table 1-46. DSP Block Performance Specifications for Arria II GX Devices (Note 1)

| Mode | Resources Used | Performance | | | | Unit |
|--|-----------------------|-------------|-----|-------|-----|------|
| | Number of Multipliers | C4 | I3 | C5,I5 | C6 | |
| 9 × 9-bit multiplier | 1 | 380 | 310 | 300 | 250 | MHz |
| 12 × 12-bit multiplier | 1 | 380 | 310 | 300 | 250 | MHz |
| 18 × 18-bit multiplier | 1 | 380 | 310 | 300 | 250 | MHz |
| 36 × 36-bit multiplier | 1 | 350 | 270 | 270 | 220 | MHz |
| 18 × 36-bit high-precision multiplier adder mode | 1 | 350 | 270 | 270 | 220 | MHz |
| 18 × 18-bit multiply accumulator | 4 | 380 | 310 | 300 | 250 | MHz |
| 18 × 18-bit multiply adder | 4 | 380 | 310 | 300 | 250 | MHz |
| 18 × 18-bit multiply adder-signed full precision | 2 | 380 | 310 | 300 | 250 | MHz |
| 18 × 18-bit multiply adder with loopback (2) | 2 | 275 | 220 | 220 | 180 | MHz |
| 36-bit shift (32-bit data) | 1 | 350 | 270 | 270 | 220 | MHz |
| Double mode | 1 | 350 | 270 | 270 | 220 | MHz |

Notes to Table 1-46:

- (1) Maximum is for a fully-pipelined block with **Round** and **Saturation** disabled.
- (2) Maximum is for loopback input registers disabled, **Round** and **Saturation** disabled, pipeline and output registers enabled.

Table 1-47 lists the DSP block performance specifications for Arria II GZ devices.

Table 1-47. DSP Block Performance Specifications for Arria II GZ Devices (Note 1) (Part 1 of 2)

| Mode | Resources Used | Performance | | Unit |
|--|-----------------------|-------------|-----|------|
| | Number of Multipliers | -3 | -4 | |
| 9 × 9-bit multiplier | 1 | 460 | 400 | MHz |
| 12 × 12-bit multiplier | 1 | 500 | 440 | MHz |
| 18 × 18-bit multiplier | 1 | 550 | 480 | MHz |
| 36 × 36-bit multiplier | 1 | 440 | 380 | MHz |
| 18 × 18-bit multiply accumulator | 4 | 440 | 380 | MHz |
| 18 × 18-bit multiply adder | 4 | 470 | 410 | MHz |
| 18 × 18-bit multiply adder-signed full precision | 2 | 450 | 390 | MHz |
| 18 × 18-bit multiply adder with loopback (2) | 2 | 350 | 310 | MHz |
| 36-bit shift (32-bit data) | 1 | 440 | 380 | MHz |

Table 1-47. DSP Block Performance Specifications for Arria II GZ Devices (Note 1) (Part 2 of 2)

| Mode | Resources Used | Performance | | Unit |
|-------------|-----------------------|-------------|-----|------|
| | Number of Multipliers | -3 | -4 | |
| Double mode | 1 | 440 | 380 | MHz |

Notes to Table 1-47:

- (1) Maximum is for fully pipelined block with **Round** and **Saturation** disabled.
(2) Maximum for loopback input registers disabled, **Round** and **Saturation** disabled, and pipeline and output registers enabled.

Embedded Memory Block Specifications

Table 1-48 lists the embedded memory block specifications for Arria II GX devices.

Table 1-48. Embedded Memory Block Performance Specifications for Arria II GX Devices

| Memory | Mode | Resources Used | | Performance | | | | Unit |
|---------------------------------|---|----------------|-----------------|-------------|-----|-------|------|------|
| | | ALUTs | Embedded Memory | I3 | C4 | C5,I5 | C6 | |
| Memory Logic Array Block (MLAB) | Single port 64 × 10 | 0 | 1 | 450 | 500 | 450 | 378 | MHz |
| | Simple dual-port 32 × 20 single clock | 0 | 1 | 270 | 500 | 450 | 378 | MHz |
| | Simple dual-port 64 × 10 single clock | 0 | 1 | 428 | 500 | 450 | 378 | MHz |
| M9K Block | Single-port 256 × 36 | 0 | 1 | 360 | 400 | 360 | 310 | MHz |
| | Single-port 256 × 36, with the read-during-write option set to Old Data | 0 | 1 | 250 | 280 | 250 | 210 | MHz |
| | Simple dual-port 256 × 36 single CLK | 0 | 1 | 360 | 400 | 360 | 310 | MHz |
| | Single-port 256 × 36 single CLK, with the read-during-write option set to Old Data | 0 | 1 | 250 | 280 | 250 | 210 | MHz |
| | True dual port 512 × 18 single CLK | 0 | 1 | 360 | 400 | 360 | 310 | MHz |
| | True dual-port 512 × 18 single CLK, with the read-during-write option set to Old Data | 0 | 1 | 250 | 280 | 250 | 210 | MHz |
| | Min Pulse Width (clock high time) | — | — | 900 | 850 | 950 | 1130 | ps |
| | Min Pulse Width (clock low time) | — | — | 730 | 690 | 770 | 920 | ps |

Table 1-49 lists the embedded memory block specifications for Arria II GZ devices.

Table 1-49. Embedded Memory Block Performance Specifications for Arria II GZ Devices (Note 1)

| Memory | Mode | Resources Used | | Performance | | | | Unit |
|--------------------|---|----------------|------------------|-------------|-----|-----|-----|------|
| | | ALUTs | TriMatrix Memory | C3 | I3 | C4 | I4 | |
| MLAB (2) | Single port 64 × 10 | 0 | 1 | 500 | 500 | 450 | 450 | MHz |
| | Simple dual-port 32 × 20 | 0 | 1 | 500 | 500 | 450 | 450 | MHz |
| | Simple dual-port 64 × 10 | 0 | 1 | 500 | 500 | 450 | 450 | MHz |
| | ROM 64 × 10 | 0 | 1 | 500 | 500 | 450 | 450 | MHz |
| | ROM 32 × 20 | 0 | 1 | 500 | 500 | 450 | 450 | MHz |
| M9K Block (2) | Single-port 256 × 36 | 0 | 1 | 540 | 540 | 475 | 475 | MHz |
| | Simple dual-port 256 × 36 | 0 | 1 | 490 | 490 | 420 | 420 | MHz |
| | Simple dual-port 256 × 36, with the read-during-write option set to Old Data | 0 | 1 | 340 | 340 | 300 | 300 | MHz |
| | True dual port 512 × 18 | 0 | 1 | 430 | 430 | 370 | 370 | MHz |
| | True dual-port 512 × 18, with the read-during-write option set to Old Data | 0 | 1 | 335 | 335 | 290 | 290 | MHz |
| | ROM 1 Port | 0 | 1 | 540 | 540 | 475 | 475 | MHz |
| | ROM 2 Port | 0 | 1 | 540 | 540 | 475 | 475 | MHz |
| | Min Pulse Width (clock high time) | — | — | 800 | 800 | 850 | 850 | ps |
| | Min Pulse Width (clock low time) | — | — | 625 | 625 | 690 | 690 | ps |
| M144K Block (2) | Single-port 2K × 72 | 0 | 1 | 440 | 400 | 380 | 350 | MHz |
| | Simple dual-port 2K × 72 | 0 | 1 | 435 | 375 | 385 | 325 | MHz |
| | Simple dual-port 2K × 72, with the read-during-write option set to Old Data | 0 | 1 | 240 | 225 | 205 | 200 | MHz |
| | Simple dual-port 2K × 64 (with ECC) | 0 | 1 | 300 | 295 | 255 | 250 | MHz |
| | True dual-port 4K × 36 | 0 | 1 | 375 | 350 | 330 | 310 | MHz |
| | True dual-port 4K × 36, with the read-during-write option set to Old Data | 0 | 1 | 230 | 225 | 205 | 200 | MHz |
| | ROM 1 Port | 0 | 1 | 500 | 450 | 435 | 420 | MHz |
| | ROM 2 Port | 0 | 1 | 465 | 425 | 400 | 400 | MHz |
| | Min Pulse Width (clock high time) | — | — | 755 | 860 | 860 | 950 | ps |
| | Min Pulse Width (clock low time) | — | — | 625 | 690 | 690 | 690 | ps |

Notes to Table 1-48:

- (1) To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL set to 50% output duty cycle. Use the Quartus II software to report timing for this and other memory block clocking schemes.
- (2) When you use the error detection CRC feature, there is no degradation in F_{MAX} .

Configuration

Table 1-50 lists the configuration mode specifications for Arria II GX and GZ devices.

Table 1-50. Configuration Mode Specifications for Arria II Devices

| Programming Mode | DCLK Frequency | | | Unit |
|------------------------------------|----------------|-----|-----|------|
| | Min | Typ | Max | |
| Passive serial | — | — | 125 | MHz |
| Fast passive parallel | — | — | 125 | MHz |
| Fast active serial (fast clock) | 17 | 26 | 40 | MHz |
| Fast active serial (slow clock) | 8.5 | 13 | 20 | MHz |
| Remote update only in fast AS mode | — | — | 10 | MHz |

JTAG Specifications

Table 1-51 lists the JTAG timing parameters and values for Arria II GX and GZ devices.

Table 1-51. JTAG Timing Parameters and Values for Arria II Devices

| Symbol | Description | Min | Max | Unit |
|-----------------|--|-----|-----|------|
| t_{JCP} | TCK clock period | 30 | — | ns |
| t_{JCH} | TCK clock high time | 14 | — | ns |
| t_{JCL} | TCK clock low time | 14 | — | ns |
| $t_{JPSU(TDI)}$ | TDI JTAG port setup time | 1 | — | ns |
| $t_{JPSU(TMS)}$ | TMS JTAG port setup time | 3 | — | ns |
| t_{JPH} | JTAG port hold time | 5 | — | ns |
| t_{JPCO} | JTAG port clock to output | — | 11 | ns |
| t_{JPZX} | JTAG port high impedance to valid output | — | 14 | ns |
| t_{JPXZ} | JTAG port valid output to high impedance | — | 14 | ns |

Chip-Wide Reset (Dev_CLRn) Specifications

Table 1-52 lists the specifications for the chip-wide reset (Dev_CLRn) for Arria II GX and GZ devices.

Table 1-52. Chip-Wide Reset (Dev_CLRn) Specifications for Arria II Devices

| Description | Min | Typ | Max | Unit |
|-------------|-----|-----|-----|---------|
| Dev_CLRn | 500 | — | — | μ S |

Periphery Performance

This section describes periphery performance, including high-speed I/O, external memory interface, and IOE programmable delay.

I/O performance supports several system interfaces, for example the high-speed I/O interface, external memory interface, and the PCI/PCI-X bus interface. I/O using SSTL-18 Class I termination standard can achieve up to the stated DDR2 SDRAM interfacing speed with typical DDR2 SDRAM memory interface setup. I/O using general purpose I/O (GPIO) standards such as 3.0, 2.5, 1.8, or 1.5 LVTTTL/LVCMOS are capable of typical 200 MHz interfacing frequency with 10pF load.



Actual achievable frequency depends on design- and system-specific factors. You should perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

High-Speed I/O Specification

Table 1-53 lists the high-speed I/O timing for Arria II GX devices.

Table 1-53. High-Speed I/O Specifications for Arria II GX Devices (Part 1 of 4)

| Symbol | Conditions | I3 | | C4 | | C5,I5 | | C6 | | Unit |
|--|-------------------------------------|-----|-----|-----|-----|-------|-------|-----|-------|------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| Clock | | | | | | | | | | |
| $f_{\text{HSCLK_IN}}$ (input clock frequency)—Row I/O | Clock boost factor, W = 1 to 40 (1) | 5 | 670 | 5 | 670 | 5 | 622 | 5 | 500 | MHz |
| $f_{\text{HSCLK_IN}}$ (input clock frequency)—Column I/O | Clock boost factor, W = 1 to 40 (1) | 5 | 500 | 5 | 500 | 5 | 472.5 | 5 | 472.5 | MHz |
| $f_{\text{HSCLK_OUT}}$ (output clock frequency)—Row I/O | — | 5 | 670 | 5 | 670 | 5 | 622 | 5 | 500 | MHz |
| $f_{\text{HSCLK_OUT}}$ (output clock frequency)—Column I/O | — | 5 | 500 | 5 | 500 | 5 | 472.5 | 5 | 472.5 | MHz |

Table 1-53. High-Speed I/O Specifications for Arria II GX Devices (Part 2 of 4)

| Symbol | Conditions | I3 | | C4 | | C5,I5 | | C6 | | Unit |
|---|---|-----|-------------|-----|-------------|-------|-------------|-----|-----|------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| Transmitter | | | | | | | | | | |
| $f_{\text{HSDR_TX}}$ (true LVDS output data rate) | SERDES factor, J = 3 to 10 (using dedicated SERDES) | 150 | 1250 (2) | 150 | 1250 (2) | 150 | 1050 (2) | 150 | 840 | Mbps |
| | SERDES factor, J = 4 to 10 (using logic elements as SERDES) | (3) | 945 | (3) | 945 | (3) | 840 | (3) | 740 | Mbps |
| | SERDES factor, J = 2 (using DDR registers) and J = 1 (using SDR register) | (3) | (3) | (3) | (3) | (3) | (3) | (3) | (3) | Mbps |
| $f_{\text{HSDR_TX_E3R}}$ (emulated LVDS_E_3R output data rate) (7) | SERDES factor, J = 4 to 10 | (3) | 945 | (3) | 945 | (3) | 840 | (3) | 740 | Mbps |

Table 1-53. High-Speed I/O Specifications for Arria II GX Devices (Part 3 of 4)

| Symbol | Conditions | I3 | | C4 | | C5,I5 | | C6 | | Unit |
|--|---|-----|-------|-----|-------|-------|-------|-----|------|------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| t_{TX_JITTER} (4) | True LVDS with dedicated SERDES (data rate 600–1,250 Mbps) | — | 175 | — | 175 | — | 225 | — | 300 | ps |
| | True LVDS with dedicated SERDES (data rate < 600 Mbps) | — | 0.105 | — | 0.105 | — | 0.135 | — | 0.18 | UI |
| | True LVDS and emulated LVDS_E_3R with logic elements as SERDES (data rate 600 – 945 Mbps) | — | 260 | — | 260 | — | 300 | — | 350 | ps |
| | True LVDS and emulated LVDS_E_3R with logic elements as SERDES (data rate < 600 Mbps) | — | 0.16 | — | 0.16 | — | 0.18 | — | 0.21 | UI |
| t_{TX_DCD} | True LVDS and emulated LVDS_E_3R | 45 | 55 | 45 | 55 | 45 | 55 | 45 | 55 | % |
| t_{RISE} and t_{FALL} | True LVDS and emulated LVDS_E_3R | — | 200 | — | 200 | — | 225 | — | 250 | ps |
| TCCS | True LVDS (5) | — | 150 | — | 150 | — | 175 | — | 200 | ps |
| | Emulated LVDS_E_3R | — | 200 | — | 200 | — | 250 | — | 300 | ps |
| Receiver (6) | | | | | | | | | | |
| True differential I/O standards - f_{HSDRDP} (data rate) | SERDES factor J = 3 to 10 | 150 | 1250 | 150 | 1250 | 150 | 1050 | 150 | 840 | Mbps |

Table 1-53. High-Speed I/O Specifications for Arria II GX Devices (Part 4 of 4)

| Symbol | Conditions | I3 | | C4 | | C5,I5 | | C6 | | Unit |
|-------------------------------|---|-----|------------|-----|------------|-------|------------|-----|------------|------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| f_{HSDR} (data rate) | SERDES factor J = 3 to 10 | (3) | 945 (7) | (3) | 945 (7) | (3) | 740 (7) | (3) | 640 (7) | Mbps |
| | SERDES factor J = 2 (using DDR registers) | (3) | (7) | (3) | (7) | (3) | (7) | (3) | (7) | Mbps |
| | SERDES factor J = 1 (using SDR registers) | (3) | (7) | (3) | (7) | (3) | (7) | (3) | (7) | Mbps |
| Soft-CDR PPM tolerance | Soft-CDR mode | — | 300 | — | 300 | — | 300 | — | 300 | ±PPM |
| DPA run length | DPA mode | — | 10,000 | — | 10,000 | — | 10,000 | — | 10,000 | UI |
| Sampling window (SW) | Non-DPA mode (5) | — | 300 | — | 300 | — | 350 | — | 400 | ps |

Notes to Table 1-53:

- (1) $f_{\text{HSCLK_IN}} = f_{\text{HSDR}} / W$. Use W to determine the supported selection of input reference clock frequencies for the desired data rate.
- (2) Applicable for interfacing with DPA receivers only. For interfacing with non-DPA receivers, you must calculate the leftover timing margin in the receiver by performing link timing closure analysis. For Arria II GX transmitter to Arria II GX non-DPA receiver, the maximum supported data rate is 945 Mbps. For data rates above 840 Mbps, perform PCB trace compensation by adjusting the PCB trace length for LVDS channels to improve channel-to-channel skews.
- (3) The minimum and maximum specification depends on the clock source (for example, PLL and clock pin) and the clock routing resource you use (global, regional, or local). The I/O differential buffer and input register do not have a minimum toggle rate.
- (4) The specification is only applicable under the influence of core noise.
- (5) Applicable for true LVDS using dedicated SERDES only.
- (6) Dedicated SERDES and DPA features are only available on the right banks.
- (7) You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and the receiver sampling margin to determine the leftover timing margin.

Table 1-54 lists the high-speed I/O timing for Arria II GZ devices.

Table 1-54. High-Speed I/O Specifications for Arria II GZ Devices (Note 1), (2), (10) (Part 1 of 3)

| Symbol | Conditions | C3, I3 | | | C4, I4 | | | Unit |
|--|---------------------------------------|--------|-----|-----|--------|-----|-----|------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Clock | | | | | | | | |
| $f_{\text{HSCLK_in}}$ (input clock frequency) true differential I/O standards | Clock boost factor W = 1 to 40 (3) | 5 | — | 717 | 5 | — | 717 | MHz |
| $f_{\text{HSCLK_in}}$ (input clock frequency) single ended I/O standards (9) | Clock boost factor W = 1 to 40 (3) | 5 | — | 717 | 5 | — | 717 | MHz |
| $f_{\text{HSCLK_in}}$ (input clock frequency) single ended I/O standards (10) | Clock boost factor W = 1 to 40 (3) | 5 | — | 420 | 5 | — | 420 | MHz |

Table 1-54. High-Speed I/O Specifications for Arria II GZ Devices (Note 1), (2), (10) (Part 2 of 3)

| Symbol | Conditions | C3, I3 | | | C4, I4 | | | Unit |
|---|--|--------|-----|---------|--------|-----|---------|------|
| | | Min | Typ | Max | Min | Typ | Max | |
| $f_{\text{HCLK_OUT}}$ (output clock frequency) | — | 5 | — | 717 (7) | 5 | — | 717 (7) | MHz |
| Transmitter | | | | | | | | |
| f_{HSDR} (true LVDS output data rate) | SERDES factor, J = 3 to 10 (using dedicated SERDES) (8) | (4) | — | 1250 | (4) | — | 1250 | Mbps |
| | SERDES factor J = 2, (using DDR registers) | (4) | — | (5) | (4) | — | (5) | Mbps |
| | SERDES factor J = 1, (uses an SDR register) | (4) | — | (5) | (4) | — | (5) | Mbps |
| f_{HSDR} (emulated LVDS_E_3R output data rate) (5) | SERDES factor J = 4 to 10 | (4) | — | 1152 | (4) | — | 800 | Mbps |
| f_{HSDR} (emulated LVDS_E_1R output data rate) | | (4) | — | 200 | (4) | — | 200 | Mbps |
| $t_{\text{x Jitter}}$ | Total jitter for data rate, 600 Mbps to 1.6 Gbps | — | — | 160 | — | — | 160 | ps |
| | Total jitter for data rate, < 600 Mbps | — | — | 0.1 | — | — | 0.1 | UI |
| $t_{\text{x Jitter}}$ - emulated differential I/O standards with three external output resistor network | Total jitter for data rate, 600 Mbps to 1.25 Gbps | — | — | 300 | — | — | 325 | ps |
| | Total jitter for data rate < 600 Mbps | — | — | 0.2 | — | — | 0.25 | UI |
| $t_{\text{x Jitter}}$ - emulated differential I/O standards with one external output resistor network | — | — | — | 0.15 | — | — | 0.15 | UI |
| t_{DUTY} | TX output clock duty cycle for both True and emulated differential I/O standards | 45 | 50 | 55 | 45 | 50 | 55 | % |

Table 1-54. High-Speed I/O Specifications for Arria II GZ Devices (Note 1), (2), (10) (Part 3 of 3)

| Symbol | Conditions | C3, I3 | | | C4, I4 | | | Unit |
|---|--|--------|-----|-------|--------|-----|-------|-------|
| | | Min | Typ | Max | Min | Typ | Max | |
| t_{RISE} & t_{FALL} | True differential I/O standards | — | — | 200 | — | — | 200 | ps |
| | Emulated differential I/O standards with three external output resistor networks | — | — | 250 | — | — | 300 | ps |
| | Emulated differential I/O standards with one external output resistor | — | — | 500 | — | — | 500 | ps |
| TCCS | True LVDS | — | — | 100 | — | — | 100 | ps |
| | Emulated LVDS_E_3R | — | — | 250 | — | — | 250 | ps |
| Receiver | | | | | | | | |
| True differential I/O standards - $f_{HSDRDPA}$ (data rate) | SERDES factor J = 3 to 10 | 150 | — | 1250 | 150 | — | 1250 | Mbps |
| f_{HSDR} (data rate) | SERDES factor J = 3 to 10 | (4) | — | (6) | (4) | — | (6) | Mbps |
| | SERDES factor J = 2, uses DDR registers | (4) | — | (5) | (4) | — | (5) | Mbps |
| | SERDES factor J = 1, uses an SDR register | (4) | — | (5) | (4) | — | (5) | Mbps |
| DPA run length | DPA mode | — | — | 10000 | — | — | 10000 | UI |
| Soft-CDR PPM tolerance | Soft-CDR mode | — | — | 300 | — | — | 300 | ± PPM |
| Sampling Window (SW) | Non-DPA mode | — | — | 300 | — | — | 300 | ps |

Notes to Table 1-54:

- (1) When J = 3 to 10, use the SERDES block.
- (2) When J = 1 or 2, bypass the SERDES block.
- (3) Clock Boost Factor (W) is the ratio between input data rate to the input clock rate.
- (4) The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.
- (5) You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine leftover timing margin.
- (6) You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and the receiver sampling margin to determine the maximum data rate supported.
- (7) This is achieved by using the LVDS and DPA clock network.
- (8) If the receiver with DPA enabled and transmitter are using shared PLLs, the minimum data rate is 150 Mbps.
- (9) This only applies to DPA and soft-CDR modes.
- (10) This only applies to LVDS source synchronous mode.

Table 1-55 lists DPA lock time specifications for Arria II GX and GZ devices.

Table 1-55. DPA Lock Time Specifications for Arria II Devices (Note 1), (2), (3)

| Standard | Training Pattern | Number of Data Transitions in One Repetition of the Training Pattern | Number of Repetitions per 256 Data Transitions (4) | Maximum |
|--------------------|----------------------|--|--|----------------------|
| SPI-4 | 00000000001111111111 | 2 | 128 | 640 data transitions |
| Parallel Rapid I/O | 00001111 | 2 | 128 | 640 data transitions |
| | 10010000 | 4 | 64 | 640 data transitions |
| Miscellaneous | 10101010 | 8 | 32 | 640 data transitions |
| | 01010101 | 8 | 32 | 640 data transitions |

Notes to Table 1-55:

- (1) The DPA lock time is for one channel.
- (2) One data transition is defined as a 0-to-1 or 1-to-0 transition.
- (3) The DPA lock time stated in the table applies to both commercial and industrial grade.
- (4) This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

Figure 1-5 shows the LVDS soft-CDR/DPA sinusoidal jitter tolerance specification for Arria II GZ devices at a data rate less than 1.25 Gbps and all the Arria II GX devices.

Figure 1-5. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for All Arria II GX Devices and for Arria II GZ Devices at a Data Rate less than 1.25 Gbps

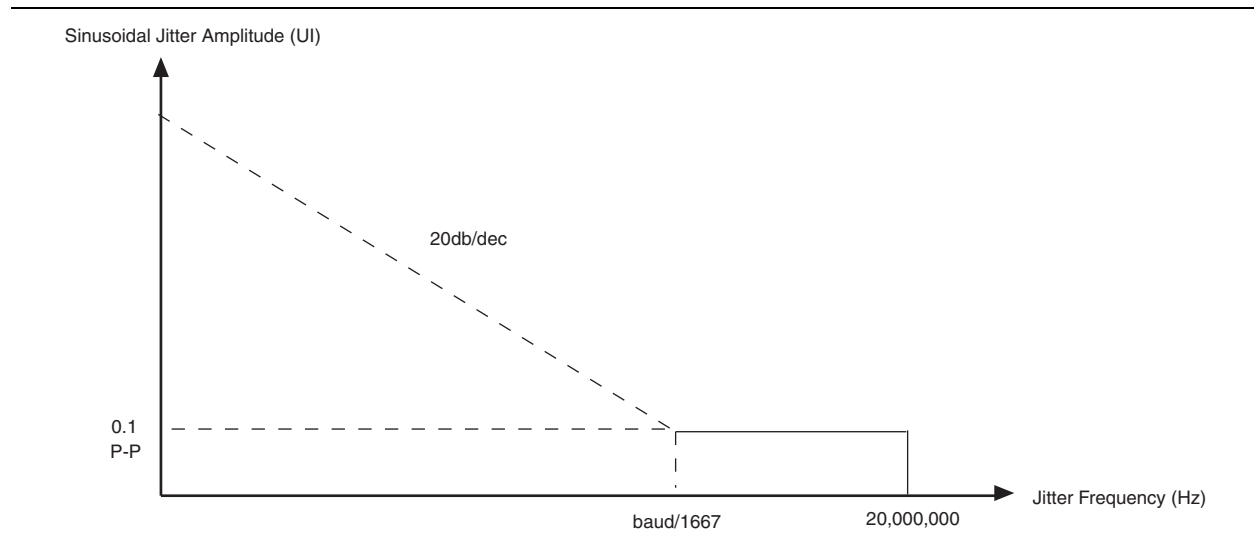


Figure 1-6 shows the LVDS soft-CDR/DPA sinusoidal jitter tolerance specification for Arria II GZ devices at 1.25 Gbps data rate.

Figure 1-6. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for Arria II GZ Devices at a 1.25 Gbps Data Rate



Table 1-56 lists the LVDS soft-CDR/DPA sinusoidal jitter tolerance specification for Arria II GZ devices at 1.25 Gbps data rate.

Table 1-56. LVDS Soft-CDR/DPA Sinusoidal Jitter Mask Values for Arria II GZ Devices at 1.25 Gbps Data Rate

| Jitter Frequency (Hz) | | Sinusoidal Jitter (UI) |
|-----------------------|------------|------------------------|
| F1 | 10,000 | 25.000 |
| F2 | 17,565 | 25.000 |
| F3 | 1,493,000 | 0.350 |
| F4 | 50,000,000 | 0.350 |

External Memory Interface Specifications


 For the maximum clock rate supported for Arria II GX and GZ device family, refer to the [External Memory Interface Spec Estimator](#) page on the Altera website.

Table 1-57 lists the external memory interface specifications for Arria II GX devices.

Table 1-57. External Memory Interface Specifications for Arria II GX Devices (Part 1 of 2)

| Frequency Mode | Frequency Range (MHz) | | | Resolution (°) | DQS Delay Buffer Mode (1) | Number of Delay Chains |
|----------------|-----------------------|------------|---------|----------------|---------------------------|------------------------|
| | C4 | I3, C5, I5 | C6 | | | |
| 0 | 90-140 | 90-130 | 90-110 | 22.5 | Low | 16 |
| 1 | 110-180 | 110-170 | 110-150 | 30 | Low | 12 |
| 2 | 140-220 | 140-210 | 140-180 | 36 | Low | 10 |
| 3 | 170-270 | 170-260 | 170-220 | 45 | Low | 8 |
| 4 | 220-340 | 220-310 | 220-270 | 30 | High | 12 |

Table 1-57. External Memory Interface Specifications for Arria II GX Devices (Part 2 of 2)

| Frequency Mode | Frequency Range (MHz) | | | Resolution (°) | DQS Delay Buffer Mode (1) | Number of Delay Chains |
|----------------|-----------------------|------------|---------|----------------|---------------------------|------------------------|
| | C4 | I3, C5, I5 | C6 | | | |
| 5 | 270-410 | 270-380 | 270-320 | 36 | High | 10 |
| 6 | 320-450 | 320-410 | 320-370 | 45 | High | 8 |

Note to Table 1-57:

(1) Low indicates a 6-bit DQS delay setting; high indicates a 5-bit DQS delay setting.

Table 1-58 lists the DLL frequency range specifications for Arria II GZ devices.

Table 1-58. DLL Frequency Range Specifications for Arria II GZ Devices

| Frequency Mode | Frequency Range (MHz) | | Available Phase Shift | DQS Delay Buffer Mode (1) | Number of Delay Chains |
|----------------|-----------------------|---------|------------------------|---------------------------|------------------------|
| | -3 | -4 | | | |
| 0 | 90-130 | 90-120 | 22.5°, 45°, 67.5°, 90° | Low | 16 |
| 1 | 120-170 | 120-160 | 30°, 60°, 90°, 120° | Low | 12 |
| 2 | 150-210 | 150-200 | 36°, 72°, 108°, 144° | Low | 10 |
| 3 | 180-260 | 180-240 | 45°, 90°, 135°, 180° | Low | 8 |
| 4 | 240-320 | 240-290 | 30°, 60°, 90°, 120° | High | 12 |
| 5 | 290-380 | 290-360 | 36°, 72°, 108°, 144° | High | 10 |
| 6 | 360-450 | 360-450 | 45°, 90°, 135°, 180° | High | 8 |
| 7 | 470-630 | 470-590 | 60°, 120°, 180°, 240° | High | 6 |

Note to Table 1-58:

(1) Low indicates a 6-bit DQS delay setting; high indicates a 5-bit DQS delay setting.

Table 1-59 lists the DQS phase offset delay per stage for Arria II GX devices.

Table 1-59. DQS Phase Offset Delay Per Setting for Arria II GX Devices (Note 1), (2), (3)

| Speed Grade | Min | Max | Unit |
|-------------|-----|------|------|
| C4 | 7.0 | 13.0 | ps |
| I3, C5, I5 | 7.0 | 15.0 | ps |
| C6 | 8.5 | 18.0 | ps |

Notes to Table 1-59:

- (1) The valid settings for phase offset are -64 to +63 for frequency modes 0 to 3 and -32 to +31 for frequency modes 4 to 5.
- (2) The typical value equals the average of the minimum and maximum values.
- (3) The delay settings are linear.

Table 1-60 lists the DQS phase shift error for Arria II GX devices.

Table 1-60. DQS Phase Shift Error Specification for DLL-Delayed Clock (t_{DQS_PSERR}) for Arria II GX Devices (Note 1)

| Number of DQS Delay Buffer | C4 | I3, C5, I5 | C6 | Unit |
|----------------------------|-----|------------|-----|------|
| 1 | 26 | 30 | 36 | ps |
| 2 | 52 | 60 | 72 | ps |
| 3 | 78 | 90 | 108 | ps |
| 4 | 104 | 120 | 144 | ps |

Note to Table 1-60:

- (1) This error specification is the absolute maximum and minimum error. For example, skew on three DQS delay buffers in a C4 speed grade is ± 78 ps or ± 39 ps.

Table 1-61 lists the DQS phase shift error for Arria II GZ devices.

Table 1-61. DQS Phase Shift Error Specification for DLL-Delayed Clock (t_{DQS_PSERR}) for Arria II GZ Devices (Note 1)

| Number of DQS Delay Buffer | -3 | -4 | Unit |
|----------------------------|-----|-----|------|
| 1 | 28 | 30 | ps |
| 2 | 56 | 60 | ps |
| 3 | 84 | 90 | ps |
| 4 | 112 | 120 | ps |

Note to Table 1-61:

- (1) This error specification is the absolute maximum and minimum error. For example, skew on three DQS delay buffers in a 3 speed grade is ± 84 ps or ± 42 ps.

Table 1-62 lists the memory output clock jitter specifications for Arria II GX devices.

Table 1-62. Memory Output Clock Jitter Specification for Arria II GX Devices (Note 1), (2), (3)

| Parameter | Clock Network | Symbol | -4 | | -5 | | -6 | | Unit |
|------------------------------|---------------|-----------------|------|-----|------|-----|------|-----|------|
| | | | Min | Max | Min | Max | Min | Max | |
| Clock period jitter | Global | $t_{JIT(per)}$ | -100 | 100 | -125 | 125 | -125 | 125 | ps |
| Cycle-to-cycle period jitter | Global | $t_{JIT(cc)}$ | -200 | 200 | -250 | 250 | -250 | 250 | ps |
| Duty cycle jitter | Global | $t_{JIT(duty)}$ | -100 | 100 | -125 | 125 | -125 | 125 | ps |

Notes to Table 1-62:

- (1) The memory output clock jitter measurements are for 200 consecutive clock cycles, as specified in the JEDEC DDR2/DDR3 SDRAM standard.
- (2) The clock jitter specification applies to memory output clock pins generated using DDIO circuits clocked by a PLL output routed on a global clock network.
- (3) The memory output clock jitter stated in Table 1-62 is applicable when an input jitter of 30 ps is applied.

Table 1–63 lists the memory output clock jitter specifications for Arria II GZ devices.

Table 1–63. Memory Output Clock Jitter Specification for Arria II GZ Devices (Note 1), (2), (3)

| Parameter | Clock Network | Symbol | –3 | | –4 | | Unit |
|------------------------------|---------------|-----------------|-------|------|-------|------|------|
| | | | Min | Max | Min | Max | |
| Clock period jitter | Regional | $t_{JIT(per)}$ | -55 | 55 | -55 | 55 | ps |
| Cycle-to-cycle period jitter | Regional | $t_{JIT(cc)}$ | -110 | 110 | -110 | 110 | ps |
| Duty cycle jitter | Regional | $t_{JIT(duty)}$ | -82.5 | 82.5 | -82.5 | 82.5 | ps |
| Clock period jitter | Global | $t_{JIT(per)}$ | -82.5 | 82.5 | -82.5 | 82.5 | ps |
| Cycle-to-cycle period jitter | Global | $t_{JIT(cc)}$ | -165 | 165 | -165 | 165 | ps |
| Duty cycle jitter | Global | $t_{JIT(duty)}$ | -90 | 90 | -90 | 90 | ps |

Notes to Table 1–63:

- (1) The memory output clock jitter measurements are for 200 consecutive clock cycles, as specified in the JEDEC DDR2/DDR3 SDRAM standard.
- (2) The clock jitter specification applies to memory output clock pins generated using differential signal-splitter and DDIO circuits clocked by a PLL output routed on a regional or global clock network as specified. Altera recommends using regional clock networks whenever possible.
- (3) The memory output clock jitter stated in Table 1–63 is applicable when an input jitter of 30 ps is applied.

Duty Cycle Distortion (DCD) Specifications

Table 1–64 lists the worst-case DCD specifications for Arria II GX devices.

Table 1–64. Duty Cycle Distortion on I/O Pins for Arria II GX Devices (Note 1)

| Symbol | C4 | | I3, C5, I5 | | C6 | | Unit |
|-------------------|-----|-----|------------|-----|-----|-----|------|
| | Min | Max | Min | Max | Min | Max | |
| Output Duty Cycle | 45 | 55 | 45 | 55 | 45 | 55 | % |

Note to Table 1–64:

- (1) The DCD specification applies to clock outputs from the PLL, global clock tree, IOE driving dedicated, and general purpose I/O pins.

Table 1–65 lists the worst-case DCD specifications for Arria II GZ devices.

Table 1–65. Duty Cycle Distortion on I/O Pins for Arria II GZ Devices (Note 1)

| Symbol | C3, I3 | | C4, I4 | | Unit |
|-------------------|--------|-----|--------|-----|------|
| | Min | Max | Min | Max | |
| Output Duty Cycle | 45 | 55 | 45 | 55 | % |

Note to Table 1–65:

- (1) The DCD specification applies to clock outputs from the PLL, global clock tree, IOE driving dedicated, and general purpose I/O pins.

IOE Programmable Delay

Table 1–66 lists the delay associated with each supported IOE programmable delay chain for Arria II GX devices.

Table 1–66. IOE Programmable Delay for Arria II GX Devices

| Parameter | Available Settings (1) | Minimum Offset (2) | Maximum Offset | | | | | | | | Unit |
|--|---------------------------|-----------------------|----------------|-------|-------|------------|-------|-------|-------|-------|------|
| | | | Fast Model | | | Slow Model | | | | | |
| | | | I3 | C4 | I5 | I3 | C4 | C5 | I5 | C6 | |
| Output enable pin delay | 7 | 0 | 0.413 | 0.442 | 0.413 | 0.814 | 0.713 | 0.796 | 0.801 | 0.873 | ns |
| Delay from output register to output pin | 7 | 0 | 0.339 | 0.362 | 0.339 | 0.671 | 0.585 | 0.654 | 0.661 | 0.722 | ns |
| Input delay from pin to internal cell | 52 | 0 | 1.494 | 1.607 | 1.494 | 2.895 | 2.520 | 2.733 | 2.775 | 2.944 | ns |
| Input delay from pin to input register | 52 | 0 | 1.493 | 1.607 | 1.493 | 2.896 | 2.503 | 2.732 | 2.774 | 2.944 | ns |
| DQS bus to input register delay | 4 | 0 | 0.074 | 0.076 | 0.074 | 0.140 | 0.124 | 0.147 | 0.147 | 0.167 | ns |

Notes to Table 1–66:

- (1) The available setting for every delay chain starts with zero and ends with the specified maximum number of settings.
- (2) The minimum offset represented in the table does not include intrinsic delay.

Table 1–67 lists the IOE programmable delay settings for Arria II GZ devices.

Table 1–67. IOE Programmable Delay for Arria II GZ Devices

| Parameter | Available Settings (1) | Minimum Offset (2) | Maximum Offset | | | | | | Unit |
|-----------|---------------------------|-----------------------|----------------|------------|------------|-------|-------|-------|------|
| | | | Fast Model | | Slow Model | | | | |
| | | | Industrial | Commercial | C3 | I3 | C4 | I4 | |
| D1 | 15 | 0 | 0.462 | 0.505 | 0.795 | 0.801 | 0.857 | 0.864 | ns |
| D2 | 7 | 0 | 0.234 | 0.232 | 0.372 | 0.371 | 0.407 | 0.405 | ns |
| D3 | 7 | 0 | 1.700 | 1.769 | 2.927 | 2.948 | 3.157 | 3.178 | ns |
| D4 | 15 | 0 | 0.508 | 0.554 | 0.882 | 0.889 | 0.952 | 0.959 | ns |
| D5 | 15 | 0 | 0.472 | 0.500 | 0.799 | 0.817 | 0.875 | 0.882 | ns |
| D6 | 6 | 0 | 0.186 | 0.195 | 0.319 | 0.321 | 0.345 | 0.347 | ns |

Notes to Table 1–67:

- (1) You can set this value in the Quartus II software by selecting **D1**, **D2**, **D3**, **D4**, **D5**, and **D6** in the **Assignment Name** column.
- (2) Minimum offset does not include the intrinsic delay.

I/O Timing

Altera offers two ways to determine I/O timing:

- Using the Microsoft Excel-based I/O Timing.
- Using the Quartus II Timing Analyzer.

The Microsoft Excel-based I/O Timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the link timing analysis. The Quartus II timing analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after place-and-route is complete.



The Microsoft Excel-based I/O Timing spreadsheet is downloadable from the [Literature: Arria II Devices](#) web page.

Glossary

Table 1-68 lists the glossary for this chapter.

Table 1-68. Glossary (Part 1 of 4)

| Letter | Subject | Definitions | | |
|--------------------------------------|-----------------------------------|---|----------------------------------|--|
| <p>A, B, C, D</p> | <p>Differential I/O Standards</p> | <p><i>Receiver Input Waveforms</i></p>  <p>Single-Ended Waveform</p> <p>Positive Channel (p) = V_{IH} Negative Channel (n) = V_{IL} Ground</p> <p>V_{ID} V_{CM}</p> <p>Differential Waveform</p> <p>V_{ID} $p - n = 0 V$ V_{ID}</p> <p><i>Transmitter Output Waveforms</i></p>  <p>Single-Ended Waveform</p> <p>Positive Channel (p) = V_{OH} Negative Channel (n) = V_{OL} Ground</p> <p>V_{OD} V_{CM}</p> <p>Differential Waveform</p> <p>V_{OD} $p - n = 0 V$ V_{OD}</p> | | |
| | | <p>E,</p> | <p>f_{HSCLK}</p> | <p>Left/Right PLL input clock frequency.</p> |
| | | <p>F</p> | <p>f_{HSDR}</p> | <p>High-speed I/O block: Maximum/minimum LVDS data transfer rate ($f_{HSDR} = 1/TUI$), non-DPA.</p> |
| | | | <p>$f_{HS DRDPA}$</p> | <p>High-speed I/O block: Maximum/minimum LVDS data transfer rate ($f_{HS DRDPA} = 1/TUI$), DPA.</p> |

Table 1-68. Glossary (Part 2 of 4)

| Letter | Subject | Definitions |
|-------------------------------|---|---|
| <p>G, H, I, J</p> | <p>J</p> <p>JTAG Timing Specifications</p> | <p>High-speed I/O block: Deserialization factor (width of parallel data bus).</p> <p>JTAG Timing Specifications:</p>  |
| | <p>K, L, M, N, O, P</p> | <p>PLL Specifications</p> |
| <p>Q, R</p> | | <p>R_L</p> |

Table 1-68. Glossary (Part 3 of 4)

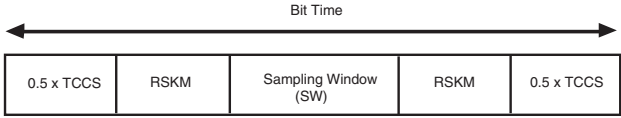
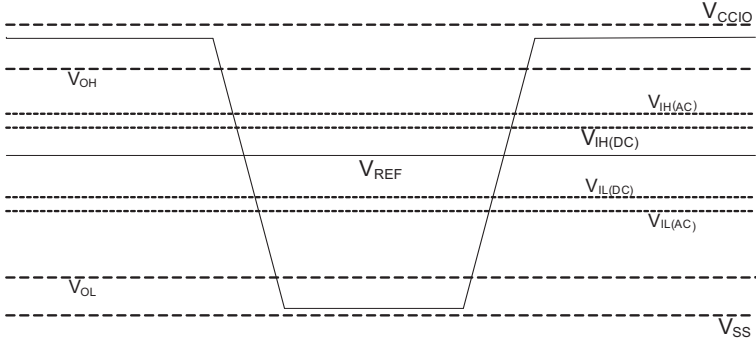
| Letter | Subject | Definitions |
|--------|---|---|
| S | <p>SW (sampling window)</p> | <p>The period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window:</p> <p><i>Timing Diagram</i></p>  |
| | <p>Single-ended Voltage Referenced I/O Standard</p> | <p>The JEDEC standard for SSTL and HSTL I/O standards define both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state.</p> <p>The new logic state is then maintained as long as the input stays beyond the AC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing:</p> <p><i>Single-Ended Voltage Referenced I/O Standard</i></p>  |
| T | <p>t_c</p> | <p>High-speed receiver and transmitter input and output clock period.</p> |
| | <p>TCCS (channel-to-channel-skew)</p> | <p>The timing difference between the fastest and slowest output edges, including t_{CO} variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the <i>Timing Diagram</i> figure under S in this table).</p> |
| | <p>t_{DUTY}</p> | <p>High-speed I/O block: Duty cycle on the high-speed transmitter output clock.</p> <p>Timing Unit Interval (TUI)</p> <p>The timing budget allowed for skew, propagation delays, and data sampling window. (TUI = 1/(Receiver Input Clock Frequency Multiplication Factor) = t_c/w)</p> |
| | <p>t_{FALL}</p> | <p>Signal high-to-low transition time (80-20%)</p> |
| | <p>t_{INCCJ}</p> | <p>Cycle-to-cycle jitter tolerance on the PLL clock input.</p> |
| | <p>t_{OUTPJ_IO}</p> | <p>Period jitter on the general purpose I/O driven by a PLL.</p> |
| | <p>t_{OUTPJ_DC}</p> | <p>Period jitter on the dedicated clock output driven by a PLL.</p> |
| | <p>t_{RISE}</p> | <p>Signal low-to-high transition time (20-80%).</p> |

Table 1–68. Glossary (Part 4 of 4)

| Letter | Subject | Definitions |
|---------------------|---|---|
| U, V | $V_{CM(DC)}$ | DC common mode input voltage. |
| | V_{ICM} | Input common mode voltage: The common mode of the differential signal at the receiver. |
| | V_{ID} | Input differential voltage swing: The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver. |
| | $V_{DIF(AC)}$ | AC differential input voltage: Minimum AC input differential voltage required for switching. |
| | $V_{DIF(DC)}$ | DC differential input voltage: Minimum DC input differential voltage required for switching. |
| | V_{IH} | Voltage input high: The minimum positive voltage applied to the input which is accepted by the device as a logic high. |
| | $V_{IH(AC)}$ | High-level AC input voltage. |
| | $V_{IH(DC)}$ | High-level DC input voltage. |
| | V_{IL} | Voltage input low: The maximum positive voltage applied to the input which is accepted by the device as a logic low. |
| | $V_{IL(AC)}$ | Low-level AC input voltage. |
| | $V_{IL(DC)}$ | Low-level DC input voltage. |
| | V_{OCM} | Output common mode voltage: The common mode of the differential signal at the transmitter. |
| V_{OD} | Output differential voltage swing: The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter. | |
| W, X, Y, Z | W | High-speed I/O block: The clock boost factor. |

Document Revision History

Table 1–69 lists the revision history for this chapter.

Table 1–69. Document Revision History (Part 1 of 2)

| Date | Version | Changes |
|---------------|---------|---|
| December 2013 | 4.4 | Updated Table 1–34 and Table 1–35. |
| July 2012 | 4.3 | <ul style="list-style-type: none"> ■ Updated the $V_{CCH_GXBL/R}$ operating conditions in Table 1–6. ■ Finalized Arria II GZ information in Table 1–20. ■ Added BLVDS specification in Table 1–32 and Table 1–33. ■ Updated input and output waveforms in Table 1–68. |
| December 2011 | 4.2 | <ul style="list-style-type: none"> ■ Updated Table 1–32, Table 1–33, Table 1–34, Table 1–35, Table 1–40, Table 1–41, Table 1–54, and Table 1–67. ■ Minor text edits. |
| June 2011 | 4.1 | <ul style="list-style-type: none"> ■ Added Table 1–60. ■ Updated Table 1–32, Table 1–33, Table 1–38, Table 1–41, and Table 1–61. ■ Updated the “Switching Characteristics” section introduction. ■ Minor text edits. |

Table 1-69. Document Revision History (Part 2 of 2)

| Date | Version | Changes |
|---------------|---------|---|
| December 2010 | 4.0 | <ul style="list-style-type: none"> ■ Added Arria II GZ information. ■ Added Table 1-61 with Arria II GX information. ■ Updated Table 1-1, Table 1-2, Table 1-5, Table 1-6, Table 1-7, Table 1-11, Table 1-35, Table 1-37, Table 1-40, Table 1-42, Table 1-44, Table 1-45, Table 1-57, Table 1-61, and Table 1-63. ■ Updated Figure 1-5. ■ Updated for the Quartus II version 10.0 release. ■ Updated the first paragraph for searchability. ■ Minor text edits. |
| July 2010 | 3.0 | <ul style="list-style-type: none"> ■ Updated Table 1-1, Table 1-4, Table 1-16, Table 1-19, Table 1-21, Table 1-23, Table 1-25, Table 1-26, Table 1-30, and Table 1-35 ■ Added Table 1-27 and Table 1-29. ■ Added I3 speed grade information to Table 1-19, Table 1-21, Table 1-22, Table 1-24, Table 1-25, Table 1-30, Table 1-32, Table 1-33, Table 1-34, and Table 1-35. ■ Updated the “Operating Conditions” section. ■ Removed “Preliminary” from Table 1-19, Table 1-21, Table 1-22, Table 1-23, Table 1-24, Table 1-25, Table 1-26, Table 1-28, Table 1-30, Table 1-32, Table 1-33, Table 1-34, and Figure 1-4. ■ Minor text edits. |
| March 2010 | 2.3 | <p>Updated for the Quartus II version 9.1 SP2 release:</p> <ul style="list-style-type: none"> ■ Updated Table 1-3, Table 1-7, Table 1-19, Table 1-21, Table 1-22, Table 1-24, Table 1-25 and Table 1-33. ■ Updated “Recommended Operating Conditions” section. ■ Minor text edits. |
| February 2010 | 2.2 | Updated Table 1-19. |
| February 2010 | 2.1 | <p>Updated for Arria II GX v9.1 SP1 release:</p> <ul style="list-style-type: none"> ■ Updated Table 1-19, Table 1-23, Table 1-28, Table 1-30, and Table 1-33. ■ Added Figure 1-5. ■ Minor text edits. |
| November 2009 | 2.0 | <p>Updated for Arria II GX v9.1 release:</p> <ul style="list-style-type: none"> ■ Updated Table 1-1, Table 1-4, Table 1-13, Table 1-14, Table 1-19, Table 1-15, Table 1-22, Table 1-24, and Table 1-28. ■ Added Table 1-6 and Table 1-33. ■ Added “Bus Hold” on page 1-5. ■ Added “IOE Programmable Delay” section. ■ Minor text edit. |
| June 2009 | 1.2 | <ul style="list-style-type: none"> ■ Updated Table 1-1, Table 1-3, Table 1-7, Table 1-8, Table 1-18, Table 1-23, Table 1-25, Table 1-26, Table 1-29, Table 1-30, Table 1-31, Table 1-32, and Table 1-33. ■ Added Table 1-32. ■ Updated Equation 1-1. |
| March 2009 | 1.1 | Added “I/O Timing” section. |
| February 2009 | 1.0 | Initial release. |



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| Country / Region | Hongkong, China |
| Total Employees | 100 - 200 People |
| Year Established | 2018 |
| Main Markets | North America South Asia Western Europe |



sales@fpgamall.com



+00852-56428680