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EP3C25F256C7N Intel IC FPGA 156 I/O 256FBGA

1. Cyclone III Device Family Overview

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Cyclone® III device family offers a unique combination of high functionality, low power and low cost. Based on Taiwan Semiconductor Manufacturing Company (TSMC) low-power (LP) process technology, silicon optimizations and software features to minimize power consumption, Cyclone III device family provides the ideal solution for your high-volume, low-power, and cost-sensitive applications. To address the unique design needs, Cyclone III device family offers the following two variants:

- Cyclone III—lowest power, high functionality with the lowest cost
- Cyclone III LS—lowest power FPGAs with security

With densities ranging from about 5,000 to 200,000 logic elements (LEs) and 0.5 Megabits (Mb) to 8 Mb of memory for less than ¼ watt of static power consumption, Cyclone III device family makes it easier for you to meet your power budget. Cyclone III LS devices are the first to implement a suite of security features at the silicon, software, and intellectual property (IP) level on a low-power and high-functionality FPGA platform. This suite of security features protects the IP from tampering, reverse engineering and cloning. In addition, Cyclone III LS devices support design separation which enables you to introduce redundancy in a single chip to reduce size, weight, and power of your application.

This chapter contains the following sections:

- "Cyclone III Device Family Features" on page 1–1
- "Cyclone III Device Family Architecture" on page 1–6
- "Reference and Ordering Information" on page 1–12

Cyclone III Device Family Features

Cyclone III device family offers the following features:

Lowest Power FPGAs

- Lowest power consumption with TSMC low-power process technology and Altera® power-aware design flow
- Low-power operation offers the following benefits:
  - Extended battery life for portable and handheld applications
  - Reduced or eliminated cooling system costs
  - Operation in thermally-challenged environments
- Hot-socketing operation support

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ISO 9001:2008 Registered

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Design Security Feature

Cyclone III LS devices offer the following design security features:

- Configuration security using advanced encryption standard (AES) with 256-bit volatile key
- Routing architecture optimized for design separation flow with the Quartus® II software
  - Design separation flow achieves both physical and functional isolation between design partitions
- Ability to disable external JTAG port
- Error Detection (ED) Cycle Indicator to core
  - Provides a pass or fail indicator at every ED cycle
  - Provides visibility over intentional or unintentional change of configuration random access memory (CRAM) bits
- Ability to perform zeroization to clear contents of the FPGA logic, CRAM, embedded memory, and AES key
- Internal oscillator enables system monitor and health check capabilities

Increased System Integration

- High memory-to-logic and multiplier-to-logic ratio
- High I/O count, low-and mid-range density devices for user I/O constrained applications
  - Adjustable I/O slew rates to improve signal integrity
  - Supports I/O standards such as LVTTL, LVCMOS, SSTL, HSTL, PCI, PCI-X, LVPECL, bus LVDS (BLVDS), LVDS, mini-LVDS, RSDS, and PPDS
  - Supports the multi-value on-chip termination (OCT) calibration feature to eliminate variations over process, voltage, and temperature (PVT)
- Four phase-locked loops (PLLs) per device provide robust clock management and synthesis for device clock management, external system clock management, and I/O interfaces
  - Five outputs per PLL
  - Cascadable to save I/Os, ease PCB routing, and reduce jitter
  - Dynamically reconfigurable to change phase shift, frequency multiplication or division, or both, and input frequency in the system without reconfiguring the device
- Remote system upgrade without the aid of an external controller
- Dedicated cyclical redundancy code checker circuitry to detect single-event upset (SEU) issues
- Nios® II embedded processor for Cyclone III device family, offering low cost and custom-fit embedded processing solutions

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- Wide collection of pre-built and verified IP cores from Altera and Altera Megafunction Partners Program (AMPP) partners
- Supports high-speed external memory interfaces such as DDR, DDR2, SDR SDRAM, and QDRII SRAM
  - Auto-calibrating PHY feature eases the timing closure process and eliminates variations with PVT for DDR, DDR2, and QDRII SRAM interfaces

Cyclone III device family supports vertical migration that allows you to migrate your device to other devices with the same dedicated pins, configuration pins, and power pins for a given package-across device densities. This allows you to optimize device density and cost as your design evolves.

Table 1–1 lists Cyclone III device family features.

Table 1–1. Cyclone III Device Family Features

Family	Device	Logic Elements	Number of M9K Blocks	Total RAM Bits	18 x 18 Multipliers	PLLs	Global Clock Networks	Maximum User I/Os
Cyclone III	EP3C5	5,136	46	423,936	23	2	10	182
	EP3C10	10,320	46	423,936	23	2	10	182
	EP3C16	15,408	56	516,096	56	4	20	346
	EP3C25	24,624	66	608,256	66	4	20	215
	EP3C40	39,600	126	1,161,216	126	4	20	535
	EP3C55	55,856	260	2,396,160	156	4	20	377
	EP3C80	81,264	305	2,810,880	244	4	20	429
	EP3C120	119,088	432	3,981,312	288	4	20	531
Cyclone III LS	EP3CLS70	70,208	333	3,068,928	200	4	20	429
	EP3CLS100	100,448	483	4,451,328	276	4	20	429
	EP3CLS150	150,848	666	6,137,856	320	4	20	429
	EP3CLS200	198,464	891	8,211,456	396	4	20	429

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Table 1–2 lists Cyclone III device family package options, I/O pins, and differential channel counts.

Table 1–2. Cyclone III Device Family Package Options, I/O pin and Differential Channel Counts *(1), (2), (3), (4), (5)*

Family	Package	E144 *(7)*	M164	P240	F256	U256	F324	F484	U484	F780
Cyclone III *(8)*	EP3C5	94, 22	106, 28	—	182, 68	182, 68	—	—	—	—
	EP3C10	94, 22	106, 28	—	182, 68	182, 68	—	—	—	—
	EP3C16	84, 19	92, 23	160, 47	168, 55	168, 55	—	346, 140	346, 140	—
	EP3C25	82, 18	—	148, 43	156, 54	156, 54	215, 83	—	—	—
	EP3C40	—	—	128, 26	—	—	195, 61	331, 127	331, 127	535, 227 *(6)*
	EP3C55	—	—	—	—	—	—	327, 135	327, 135	377, 163
	EP3C80	—	—	—	—	—	—	295, 113	295, 113	429, 181
	EP3C120	—	—	—	—	—	—	283, 106	—	531, 233
Cyclone III LS	EP3CLS70	—	—	—	—	—	—	294, 113	294, 113	429, 181
	EP3CLS100	—	—	—	—	—	—	294, 113	294, 113	429, 181
	EP3CLS150	—	—	—	—	—	—	226, 87	—	429, 181
	EP3CLS200	—	—	—	—	—	—	226, 87	—	429, 181

Notes to Table 1–2:

(1) For each device package, the first number indicates the number of the I/O pin; the second number indicates the differential channel count.

(2) For more information about device packaging specifications, refer to the Cyclone III Package and Thermal Resistance webpage.

(3) The I/O pin numbers are the maximum I/O counts (including clock input pins) supported by the device package combination and can be affected by the configuration scheme selected for the device.

(4) All packages are available in lead-free and leaded options.

(5) Vertical migration is not supported between Cyclone III and Cyclone III LS devices.

(6) The EP3C40 device in the F780 package supports restricted vertical migration. Maximum user I/Os are restricted to 510 I/Os if you enable migration to the EP3C120 and are using voltage referenced I/O standards. If you are not using voltage referenced I/O standards, you can increase the maximum number of I/Os.

(7) The E144 package has an exposed pad at the bottom of the package. This exposed pad is a ground pad that must be connected to the ground plane on your PCB. Use this exposed pad for electrical connectivity and not for thermal purposes.

(8) All Cyclone III device UBGA packages are supported by the Quartus II software version 7.1 SP1 and later, with the exception of the UBGA packages of EP3C16, which are supported by the Quartus II software version 7.2.

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Table 1–3 lists Cyclone III device family package sizes.

Table 1–3. Cyclone III Device Family Package Sizes

Family	Package	Pitch (mm)	Nominal Area (mm²)	Length x Width (mm × mm)	Height (mm)
Cyclone III	E144	0.5	484	22 × 22	1.60
	M164	0.5	64	8 × 8	1.40
	P240	0.5	1197	34.6 × 34.6	4.10
	F256	1.0	289	17 × 17	1.55
	U256	0.8	196	14 × 14	2.20
	F324	1.0	361	19 × 19	2.20
	F484	1.0	529	23 × 23	2.60
	U484	0.8	361	19 × 19	2.20
	F780	1.0	841	29 × 29	2.60
Cyclone III LS	F484	1.0	529	23 × 23	2.60
	U484	0.8	361	19 × 19	2.20
	F780	1.0	841	29 × 29	2.60

Table 1–4 lists Cyclone III device family speed grades.

Table 1–4. Cyclone III Device Family Speed Grades (Part 1 of 2)

Family	Device	E144	M164	P240	F256	U256	F324	F484	U484	F780
Cyclone III	EP3C5	C7, C8, I7, A7	C7, C8, I7	—	C6, C7, C8, I7, A7	C6, C7, C8, I7, A7	—	—	—	—
	EP3C10	C7, C8, I7, A7	C7, C8, I7	—	C6, C7, C8, I7, A7	C6, C7, C8, I7, A7	—	—	—	—
	EP3C16	C7, C8, I7, A7	C7, C8, I7	C8	C6, C7, C8, I7, A7	C6, C7, C8, I7, A7	—	C6, C7, C8, I7, A7	C6, C7, C8, I7, A7	—
	EP3C25	C7, C8, I7, A7	—	C8	C6, C7, C8, I7, A7	C6, C7, C8, I7, A7	C6, C7, C8, I7, A7	—	—	—
	EP3C40	—	—	C8	—	—	C6, C7, C8, I7, A7	C6, C7, C8, I7, A7	C6, C7, C8, I7, A7	C6, C7, C8, I7
	EP3C55	—	—	—	—	—	—	C6, C7, C8, I7	C6, C7, C8, I7	C6, C7, C8, I7
	EP3C80	—	—	—	—	—	—	C6, C7, C8, I7	C6, C7, C8, I7	C6, C7, C8, I7
	EP3C120	—	—	—	—	—	—	C7, C8, I7	—	C7, C8, I7

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Table 1–4. Cyclone III Device Family Speed Grades (Part 2 of 2)

Family	Device	E144	M164	P240	F256	U256	F324	F484	U484	F780
Cyclone III LS	EP3CLS70	—	—	—	—	—	—	C7, C8, I7	C7, C8, I7	C7, C8, I7
	EP3CLS100	—	—	—	—	—	—	C7, C8, I7	C7, C8, I7	C7, C8, I7
	EP3CLS150	—	—	—	—	—	—	C7, C8, I7	—	C7, C8, I7
	EP3CLS200	—	—	—	—	—	—	C7, C8, I7	—	C7, C8, I7

Table 1–5 lists Cyclone III device family configuration schemes.

Table 1–5. Cyclone III Device Family Configuration Schemes

Configuration Scheme	Cyclone III	Cyclone III LS
Active serial (AS)	✓	✓
Active parallel (AP)	✓	—
Passive serial (PS)	✓	✓
Fast passive parallel (FPP)	✓	✓
Joint Test Action Group (JTAG)	✓	✓

Cyclone III Device Family Architecture

Cyclone III device family includes a customer-defined feature set that is optimized for portable applications and offers a wide range of density, memory, embedded multiplier, and I/O options. Cyclone III device family supports numerous external memory interfaces and I/O protocols that are common in high-volume applications. The Quartus II software features and parameterizable IP cores make it easier for you to use the Cyclone III device family interfaces and protocols.

The following sections provide an overview of the Cyclone III device family features.

Logic Elements and Logic Array Blocks

The logic array block (LAB) consists of 16 logic elements and a LAB-wide control block. An LE is the smallest unit of logic in the Cyclone III device family architecture. Each LE has four inputs, a four-input look-up table (LUT), a register, and output logic. The four-input LUT is a function generator that can implement any function with four variables.

For more information about LEs and LABs, refer to the *Logic Elements and Logic Array Blocks in the Cyclone III Device Family* chapter.

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Memory Blocks

Each M9K memory block of the Cyclone III device family provides nine Kbits of on-chip memory capable of operating at up to 315 MHz for Cyclone III devices and up to 274 MHz for Cyclone III LS devices. The embedded memory structure consists of M9K memory blocks columns that you can configure as RAM, first-in first-out (FIFO) buffers, or ROM. The Cyclone III device family memory blocks are optimized for applications such as high throughout packet processing, embedded processor program, and embedded data storage.

The Quartus II software allows you to take advantage of the M9K memory blocks by instantiating memory using a dedicated megafunction wizard or by inferring memory directly from the VHDL or Verilog source code.

M9K memory blocks support single-port, simple dual-port, and true dual-port operation modes. Single-port mode and simple dual-port mode are supported for all port widths with a configuration of ×1, ×2, ×4, ×8, ×9, ×16, ×18, ×32, and ×36. True dual-port is supported in port widths with a configuration of ×1, ×2, ×4, ×8, ×9, ×16, and ×18.

For more information about memory blocks, refer to the *Memory Blocks in the Cyclone III Device Family* chapter.

Embedded Multipliers and Digital Signal Processing Support

Cyclone III devices support up to 288 embedded multiplier blocks and Cyclone III LS devices support up to 396 embedded multiplier blocks. Each block supports one individual 18 × 18-bit multiplier or two individual 9 × 9-bit multipliers.

The Quartus II software includes megafunctions that are used to control the operation mode of the embedded multiplier blocks based on user parameter settings. Multipliers can also be inferred directly from the VHDL or Verilog source code. In addition to embedded multipliers, Cyclone III device family includes a combination of on-chip resources and external interfaces, making them ideal for increasing performance, reducing system cost, and lowering the power consumption of digital signal processing (DSP) systems. You can use Cyclone III device family alone or as DSP device co-processors to improve price-to-performance ratios of DSP systems.

The Cyclone III device family DSP system design support includes the following features:

- DSP IP cores:
  - Common DSP processing functions such as finite impulse response (FIR), fast Fourier transform (FFT), and numerically controlled oscillator (NCO) functions
  - Suites of common video and image processing functions
- Complete reference designs for end-market applications
- DSP Builder interface tool between the Quartus II software and the MathWorks Simulink and MATLAB design environments
- DSP development kits

For more information about embedded multipliers and digital signal processing support, refer to the *Embedded Multipliers in Cyclone III Devices* chapter.

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Clock Networks and PLLs

Cyclone III device family includes 20 global clock networks. You can drive global clock signals from dedicated clock pins, dual-purpose clock pins, user logic, and PLLs. Cyclone III device family includes up to four PLLs with five outputs per PLL to provide robust clock management and synthesis. You can use PLLs for device clock management, external system clock management, and I/O interfaces.

You can dynamically reconfigure the Cyclone III device family PLLs to enable auto-calibration of external memory interfaces while the device is in operation. This feature enables the support of multiple input source frequencies and corresponding multiplication, division, and phase shift requirements. PLLs in Cyclone III device family may be cascaded to generate up to ten internal clocks and two external clocks on output pins from a single external clock source.

For more PLL specifications and information, refer to the *Cyclone III Device Data Sheet*, *Cyclone III LS Device Data Sheet*, and *Clock Networks and PLLs in the Cyclone III Device Family* chapters.

I/O Features

Cyclone III device family has eight I/O banks. All I/O banks support single-ended and differential I/O standards listed in Table 1–6.

Table 1–6. Cyclone III Device Family I/O Standards Support

Type	I/O Standard
Single-Ended I/O	LVTTL, LVCMOS, SSTL, HSTL, PCI, and PCI-X
Differential I/O	SSTL, HSTL, LVPECL, BLVDS, LVDS, mini-LVDS, RSDS, and PPDS

The Cyclone III device family I/O also supports programmable bus hold, programmable pull-up resistors, programmable delay, programmable drive strength, programmable slew-rate control to optimize signal integrity, and hot socketing. Cyclone III device family supports calibrated on-chip series termination (R_S OCT) or driver impedance matching (Rs) for single-ended I/O standards, with one OCT calibration block per side.

For more information, refer to the *I/O Features in the Cyclone III Device Family* chapter.

High-Speed Differential Interfaces

Cyclone III device family supports high-speed differential interfaces such as BLVDS, LVDS, mini-LVDS, RSDS, and PPDS. These high-speed I/O standards in Cyclone III device family provide high data throughput using a relatively small number of I/O pins and are ideal for low-cost applications. Dedicated differential output drivers on the left and right I/O banks can send data rates at up to 875 Mbps for Cyclone III devices and up to 740 Mbps for Cyclone III LS devices, without the need for external resistors. This saves board space or simplifies PCB routing. Top and bottom I/O banks support differential transmission (with the addition of an external resistor network) data rates at up to 640 Mbps for both Cyclone III and Cyclone III LS devices.

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For more information, refer to the *High-Speed Differential Interfaces in the Cyclone III Device Family* chapter.

Auto-Calibrating External Memory Interfaces

Cyclone III device family supports common memory types such as DDR, DDR2, SDR SDRAM, and QDRII SRAM. DDR2 SDRAM memory interfaces support data rates up to 400 Mbps for Cyclone III devices and 333 Mbps for Cyclone III LS devices. Memory interfaces are supported on all sides of Cyclone III device family. Cyclone III device family has the OCT, DDR output registers, and 8-to-36-bit programmable DQ group widths features to enable rapid and robust implementation of different memory standards.

An auto-calibrating megafunction is available in the Quartus II software for DDR and QDR memory interface PHYs. This megafunction is optimized to take advantage of the Cyclone III device family I/O structure, simplify timing closure requirements, and take advantage of the Cyclone III device family PLL dynamic reconfiguration feature to calibrate PVT changes.

For more information, refer to the *External Memory Interfaces in the Cyclone III Device Family* chapter.

Support for Industry-Standard Embedded Processors

To quickly and easily create system-level designs using Cyclone III device family, you can select among the ×32-bit soft processor cores: Freescale®V1 Coldfire, ARM® Cortex M1, or Altera Nios® II, along with a library of 50 other IP blocks when using the system-on-a-programmable-chip (SOPC) Builder tool. SOPC Builder is an Altera Quartus II design tool that facilitates system-integration of IP blocks in an FPGA design. The SOPC Builder automatically generates interconnect logic and creates a testbench to verify functionality, saving valuable design time.

Cyclone III device family expands the peripheral set, memory, I/O, or performance of legacy embedded processors. Single or multiple Nios II embedded processors are designed into Cyclone III device family to provide additional co-processing power, or even replace legacy embedded processors in your system. Using the Cyclone III device family and Nios II together provide low-cost, high-performance embedded processing solutions, which in turn allow you to extend the life cycle of your product and improve time-to-market over standard product solutions.

Separate licensing of the Freescale and ARM embedded processors are required.

Hot Socketing and Power-On-Reset

Cyclone III device family features hot socketing (also known as hot plug-in or hot swap) and power sequencing support without the use of external devices. You can insert or remove a board populated with one or more Cyclone III device family during a system operation without causing undesirable effects to the running system bus or the board that was inserted into the system.

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The hot socketing feature allows you to use FPGAs on PCBs that also contain a mixture of 3.3-V, 2.5-V, 1.8-V, 1.5-V, and 1.2-V devices. The Cyclone III device family hot socketing feature eliminates power-up sequence requirements for other devices on the board for proper FPGA operation.

For more information about hot socketing and power-on-reset, refer to the *Hot-Socketing and Power-on Reset in the Cyclone III Device Family* chapter.

SEU Mitigation

Cyclone III LS devices offer built-in error detection circuitry to detect data corruption due to soft errors in the CRAM cells. This feature allows CRAM contents to be read and verified to match a configuration-computed CRC value. The Quartus II software activates the built-in 32-bit CRC checker, which is part of the Cyclone III LS device.

For more information about SEU mitigation, refer to the *SEU Mitigation in the Cyclone III Device Family* chapter.

JTAG Boundary Scan Testing

Cyclone III device family supports the JTAG IEEE Std. 1149.1 specification. The boundary-scan test (BST) architecture offers the capability to test pin connections without using physical test probes and captures functional data while a device is operating normally. Boundary-scan cells in the Cyclone III device family can force signals onto pins or capture data from pins or from logic array signals. Forced test data is serially shifted into the boundary-scan cells. Captured data is serially shifted out and externally compared to expected results. In addition to BST, you can use the IEEE Std. 1149.1 controller for the Cyclone III LS device in-circuit reconfiguration (ICR).

For more information about JTAG boundary scan testing, refer to the *IEEE 1149.1 (JTAG) Boundary-Scan Testing for the Cyclone III Device Family* chapter.

Quartus II Software Support

The Quartus II software is the leading design software for performance and productivity. It is the only complete design solution for CPLDs, FPGAs, and ASICs in the industry. The Quartus II software includes an integrated development environment to accelerate system-level design and seamless integration with leading third-party software tools and flows.

The Cyclone III LS devices provide both physical and functional separation between security critical design partitions. Cyclone III LS devices offer isolation between design partitions. This ensures that device errors do not propagate from one partition to another, whether unintentional or intentional. The Quartus II software design separation flow facilitates the creation of separation regions in Cyclone III LS devices by tightly controlling the routing in and between the LogicLock regions. For ease of use, the separation flow integrates in the existing incremental compilation flow.

For more information about the Quartus II software features, refer to the *Quartus II Handbook*.

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Configuration

Cyclone III device family uses SRAM cells to store configuration data. Configuration data is downloaded to Cyclone III device family each time the device powers up. Low-cost configuration options include the Altera EPCS family serial flash devices as well as commodity parallel flash configuration options. These options provide the flexibility for general-purpose applications and the ability to meet specific configuration and wake-up time requirements of the applications. Cyclone III device family supports the AS, PS, FPP, and JTAG configuration schemes. The AP configuration scheme is only supported in Cyclone III devices.

For more information about configuration, refer to the *Configuration, Design Security, and Remote System Upgrades in the Cyclone III Device Family* chapter.

Remote System Upgrades

Cyclone III device family offers remote system upgrade without an external controller. The remote system upgrade capability in Cyclone III device family allows system upgrades from a remote location. Soft logic (either the Nios II embedded processor or user logic) implemented in Cyclone III device family can download a new configuration image from a remote location, store it in configuration memory, and direct the dedicated remote system upgrade circuitry to start a reconfiguration cycle. The dedicated circuitry performs error detection during and after the configuration process, and can recover from an error condition by reverting to a safe configuration image. The dedicated circuitry also provides error status information. Cyclone III devices support remote system upgrade in the AS and AP configuration scheme. Cyclone III LS devices support remote system upgrade in the AS configuration scheme only.

For more information, refer to the *Configuration, Design Security, and Remote System Upgrades in the Cyclone III Device Family* chapter.

Design Security (Cyclone III LS Devices Only)

Cyclone III LS devices offer design security features which play a vital role in the large and critical designs in the competitive military and commercial environments. Equipped with the configuration bit stream encryption and anti-tamper features, Cyclone III LS devices protect your designs from copying, reverse engineering and tampering. The configuration security of Cyclone III LS devices uses AES with 256-bit security key.

For more information, refer to the *Configuration, Design Security, and Remote System Upgrades in Cyclone III Device Family* chapter.

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Reference and Ordering Information

Figure 1–1 and Figure 1–2 show the ordering codes for Cyclone III and Cyclone III LS devices.

Figure 1–1. Cyclone III Device Packaging Ordering Information

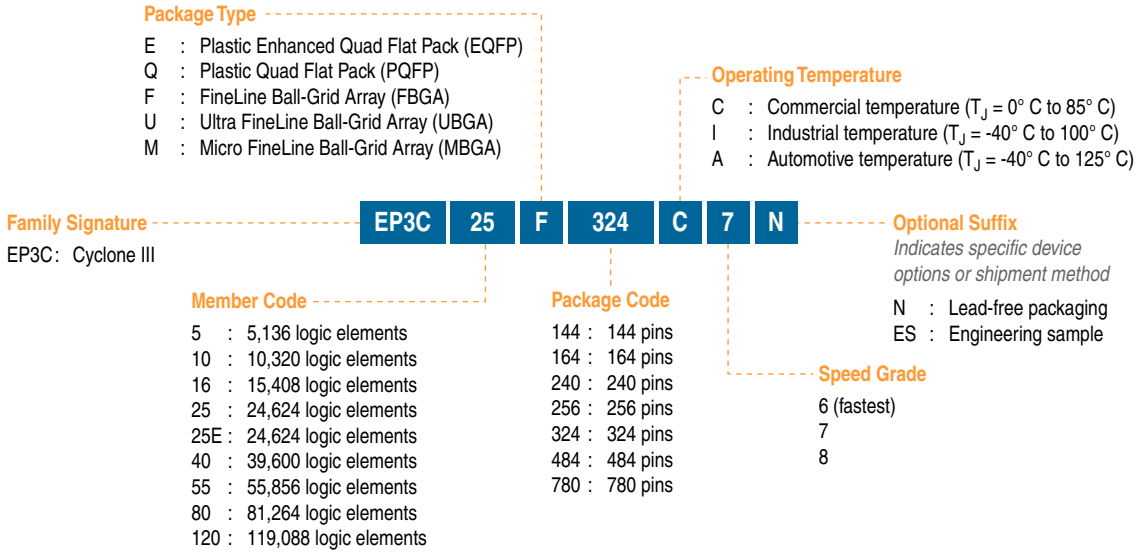
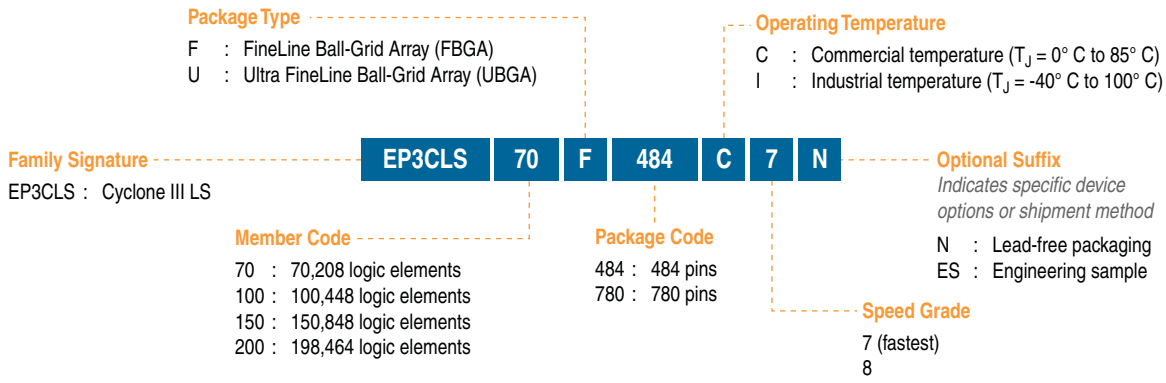


Figure 1–2. Cyclone III LS Device Packaging Ordering Information



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Document Revision History

Table 1–7 lists the revision history for this document.

Table 1–7. Document Revision History

Date	Version	Changes
July 2012	2.4	Updated 484 pin package code in Figure 1–1.
December 2011	2.3	■ Updated Table 1–1 and Table 1–2. ■ Updated Figure 1–1 and Figure 1–2. ■ Updated hyperlinks. ■ Minor text edits.
December 2009	2.2	Minor text edits.
July 2009	2.1	Minor edit to the hyperlinks.
June 2009	2.0	■ Added Table 1–5. ■ Updated Table 1–1, Table 1–2, Table 1–3, and Table 1–4. ■ Updated “Introduction”, “Cyclone III Device Family Architecture”, “Embedded Multipliers and Digital Signal Processing Support ”, “Clock Networks and PLLs ”, “I/O Features ”, “High-Speed Differential Interfaces ”, “Auto-Calibrating External Memory Interfaces ”, “Quartus II Software Support”, “Configuration ”, and “Design Security (Cyclone III LS Devices Only)”. ■ Removed “Referenced Document” section.
October 2008	1.3	■ Updated “Increased System Integration” section. ■ Updated “Memory Blocks” section. ■ Updated chapter to new template.
May 2008	1.2	■ Added 164-pin Micro FineLine Ball-Grid Array (MBGA) details to Table 1–2, Table 1–3 and Table 1–4. ■ Updated Figure 1–2 with automotive temperature information. ■ Updated “Increased System Integration” section, Table 1–6, and “High-Speed Differential Interfaces” section with BLVDS information.
July 2007	1.1	■ Removed the text “Spansion” in “Increased System. ■ Integration” and “Configuration” sections. ■ Removed trademark symbol from “MultiTrack” in “MultiTrack Interconnect”. ■ Removed registered trademark symbol from “Simulink” and “MATLAB” from “Embedded Multipliers and Digital. ■ Signal Processing Support” section. ■ Added chapter TOC and “Referenced Documents” section.
March 2007	1.0	Initial release.

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