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# XC4000XL Electrical Specifications

## Definition of Terms

In the following tables, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

**Advance:** Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or device families. Values are subject to change. Use as estimates, not for production.

**Preliminary:** Based on preliminary characterization. Further changes are not expected.

**Unmarked:** Specifications not identified as either Advance or Preliminary are to be considered Final.

Except for pin-to-pin input and output parameters, the a.c. parameter delay specifications included in this document are derived from measuring internal test patterns. All specifications are representative of worst-case supply voltage and junction temperature conditions.

**All specifications subject to change without notice.**

# XC4000XL D.C. Characteristics

## Absolute Maximum Ratings

| | Description | | | Units |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage relative to Ground | | -0.5 to 4.0 | V |
| $V_{IN}$ | Input voltage relative to Ground (Note 1) | | -0.5 to 5.5 | V |
| $V_{TS}$ | Voltage applied to 3-state output (Note 1) | | -0.5 to 5.5 | V |
| $V_{CCt}$ | Longest Supply Voltage Rise Time from 1 V to 3V | | 50 | ms |
| $T_{STG}$ | Storage temperature (ambient) | | -65 to +150 | °C |
| $T_{SOL}$ | Maximum soldering temperature (10 s @ 1/16 in. = 1.5 mm) | | +260 | °C |
| $T_J$ | Junction Temperature | Ceramic packages | +150 | °C |
| | | Plastic packages | +125 | °C |

Note 1: Maximum DC excursion above $V_{cc}$ or below Ground must be limited to either 0.5 V or 10 mA, whichever is easier to achieve. During transitions, the device pins may undershoot to -2.0 V or overshoot to$V_{CC}$ +2.0 V, provided this over or undershoot lasts less than 10 ns and with the forcing current being limited to 200 mA.

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

## Recommended Operating Conditions

| Symbol | Description | | Min | Max | Units |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage relative to Gnd, $T_J$ = 0 °C to +85°C | Commercial | 3.0 | 3.6 | V |
| | Supply voltage relative to Gnd, $T_J$ = -40°C to +100°C | Industrial | 3.0 | 3.6 | V |
| $V_{IH}$ | High-level input voltage | | 50% of $V_{CC}$ | 5.5 | V |
| $V_{IL}$ | Low-level input voltage | | 0 | 30% of $V_{CC}$ | V |
| $T_{IN}$ | Input signal transition time | | | 250 | ns |

Notes: At junction temperatures above those listed above, all delay parameters increase by 0.35% per °C.
Input and output measurement threshold is ~50% of $V_{CC}$.

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## D.C. Characteristics Over Recommended Operating Conditions

| Symbol | Description | | Min | Max | Units |
|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage @ $I_{OH}$ = -4.0 mA, $V_{CC}$ min (LVTTL) | | 2.4 | | V |
| | High-level output voltage @ $I_{OH}$ = -500 µA, (LVCMOS) | | 90% $V_{CC}$ | | V |
| $V_{OL}$ | Low-level output voltage @ $I_{OL}$ = 12.0 mA, $V_{CC}$ min (LVTTL) (Note 1) | | | 0.4 | V |
| | Low-level output voltage @ $I_{OL}$ = 1500 µA, (LVCMOS) | | | 10% $V_{CC}$ | V |
| $V_{DR}$ | Data Retention Supply Voltage (below which configuration data may be lost) | | 2.5 | | V |
| $I_{CCO}$ | Quiescent FPGA supply current (Note 2) | | | 5 | mA |
| $I_L$ | Input or output leakage current | | -10 | +10 | µA |
| $C_{IN}$ | Input capacitance (sample tested) | BGA, SBGA, PQ, HQ, MQ packages | | 10 | pF |
| | | PGA packages | | 16 | pF |
| $I_{RPU}$ | Pad pull-up (when selected) @ $V_{in}$ = 0 V (sample tested) | | 0.02 | 0.25 | mA |
| $I_{RPD}$ | Pad pull-down (when selected) @ $V_{in}$ = 3.6 V (sample tested) | | 0.02 | 0.15 | mA |
| $I_{RLL}$ | Horizontal Longline pull-up (when selected) @ logic Low | | 0.3 | 2.0 | mA |

Note 1: With up to 64 pins simultaneously sinking 12 mA.
Note 2: With no output current loads, no active input or Longline pull-up resistors, all I/O pins Tri-stated and floating.

## Power-0n Power Supply Requirements

Xilinx FPGAs require a minimum rated power supply current capacity to insure proper initialization, and the power supply ramp-up time does affect the current required. A fast ramp-up time requires more current than a slow ramp-up time. The slowest ramp-up time is 50 ms. Current capacity is not specified for a ramp-up time faster than 2ms. The current capacity varies linealy with ramp-up time, *e.g.*, an XC4036XL with a ramp-up time of 25 ms would require a capacity predicted by the point on the straight line drawn from 1A at 120 µs to 500 mA at 50 ms at the 25 ms time mark. This point is approximately 750 mA .

| Product | Description | Ramp-up Time | |
|---|---|---|---|
| | | Fast (120 µs) | Slow (50 ms) |
| XC4005 - 36XL | Minimum required current supply | 1 A | 500 mA |
| XC4044- 62XL | Minimum required current supply | 2 A | 500 mA |
| XC4085XL[1] | Minimum required current supply | 2 A[1] | 500 mA |

Notes: 1. The XC4085XL fast ramp-up time is 5 ms.
Devices are guaranteed to initialize properly with the minimum current listed above. A larger capacity power supply may result in a larger initialization current.
This specification applies to Commercial and Industrial grade products only.
Ramp-up Time is measured from 0 $V_{DC}$ to 3.6 $V_{DC}$. Peak current required lasts less than 3 ms, and occurs near the internal power on reset threshold voltage. After initialization and before configuration, $I_{CC}$max is less than 10 mA.

# XC4000XL A.C. Characteristics

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

When fewer vertical clock lines are connected, the clock distribution is faster; when multiple clock lines per column are driven from the same global clock, the delay is longer. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature. Values apply to all XC4000XL devices and are expressed in nanoseconds unless otherwise noted.

## Global Low Skew Buffer to Clock K

| | | Speed Grade | All | -3 | -2 | -1 | -09 | -08 | Units |
|---|---|---|---|---|---|---|---|---|---|
| **Description** | **Symbol** | **Device** | **Min** | **Max** | **Max** | **Max** | **Max** | **Max** | |
| Delay from pad through GLS buffer to any clock input, K | $T_{GLS}$ | XC4002XL | 0.3 | 2.1 | 1.8 | 1.6 | 1.5 | | ns |
| | | XC4005XL | 0.4 | 2.7 | 2.3 | 2.0 | 1.9 | | ns |
| | | XC4010XL | 0.5 | 3.2 | 2.8 | 2.4 | 2.3 | | ns |
| | | XC4013XL | 0.6 | 3.6 | 3.1 | 2.7 | 2.6 | 2.3 | ns |
| | | XC4020XL | 0.7 | 4.0 | 3.5 | 3.0 | 2.9 | | ns |
| | | XC4028XL | 0.9 | 4.4 | 3.8 | 3.3 | 3.2 | | ns |
| | | XC4036XL | 1.1 | 4.8 | 4.2 | 3.6 | 3.5 | 3.1 | ns |
| | | XC4044XL | 1.2 | 5.3 | 4.6 | 4.0 | 3.9 | | ns |
| | | XC4052XL | 1.3 | 5.7 | 5.0 | 4.5 | 4.4 | | ns |
| | | XC4062XL | 1.4 | 6.3 | 5.4 | 4.7 | 4.6 | 4.0 | ns |
| | | XC4085XL | 1.6 | 7.2 | 6.2 | 5.7 | 5.5 | | ns |

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## Global Early BUFGEs 1, 2, 5, and 6 to IOB Clock

| | | Speed Grade | All | -3 | -2 | -1 | -09 | -08 | Units |
|---|---|---|---|---|---|---|---|---|---|
| Description | Symbol | Device | Min | Max | Max | Max | Max | Max | |
| Delay from pad through GE buffer to any IOB clock input. | $T_{GE}$ | XC4002XL | 0.1 | 1.6 | 1.4 | 1.3 | 1.2 | | ns |
| | | XC4005XL | 0.3 | 1.9 | 1.8 | 1.7 | 1.6 | | ns |
| | | XC4010XL | 0.3 | 2.2 | 1.9 | 1.7 | 1.7 | | ns |
| | | XC4013XL | 0.4 | 2.4 | 2.1 | 1.8 | 1.7 | 1.5 | ns |
| | | XC4020XL | 0.4 | 2.6 | 2.2 | 2.1 | 2.0 | | ns |
| | | XC4028XL | 0.3 | 2.8 | 2.4 | 2.1 | 2.0 | | ns |
| | | XC4036XL | 0.3 | 3.1 | 2.7 | 2.3 | 2.2 | 1.9 | ns |
| | | XC4044XL | 0.2 | 3.5 | 3.0 | 2.6 | 2.4 | | ns |
| | | XC4052XL | 0.3 | 4.0 | 3.5 | 3.0 | 3.0 | | ns |
| | | XC4062XL | 0.3 | 4.9 | 4.3 | 3.7 | 3.4 | 3.0 | ns |
| | | XC4085XL | 0.4 | 5.8 | 5.1 | 4.7 | 4.3 | | ns |

## Global Early BUFGEs 3, 4, 7, and 8 to IOB Clock

| | | Speed Grade | All | -3 | -2 | -1 | -09 | -08 | Units |
|---|---|---|---|---|---|---|---|---|---|
| Description | Symbol | Device | Min | Max | Max | Max | Max | Max | |
| Delay from pad through GE buffer to any IOB clock input. | $T_{GE}$ | XC4002XL | 0.5 | 2.8 | 2.5 | 2.1 | 1.7 | | ns |
| | | XC4005XL | 0.7 | 3.1 | 2.8 | 2.7 | 2.5 | | ns |
| | | XC4010XL | 0.7 | 3.5 | 3.1 | 2.8 | 2.7 | | ns |
| | | XC4013XL | 0.7 | 3.8 | 3.3 | 2.9 | 2.8 | 2.4 | ns |
| | | XC4020XL | 0.8 | 4.1 | 3.6 | 3.4 | 3.2 | | ns |
| | | XC4028XL | 0.9 | 4.4 | 3.9 | 3.4 | 3.3 | | ns |
| | | XC4036XL | 0.9 | 4.7 | 4.2 | 3.7 | 3.6 | 3.1 | ns |
| | | XC4044XL | 1.0 | 5.1 | 4.5 | 4.0 | 3.7 | | ns |
| | | XC4052XL | 1.1 | 5.5 | 4.8 | 4.3 | 4.3 | | ns |
| | | XC4062XL | 1.2 | 5.9 | 5.2 | 4.8 | 4.5 | 4.0 | ns |
| | | XC4085XL | 1.3 | 6.8 | 6.0 | 5.5 | 5.2 | | ns |

# XC4000XL CLB Characteristics

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000XL devices and are expressed in nanoseconds unless otherwise noted.

## CLB Switching Characteristic Guidelines

| | Speed Grade | -3 | | -2 | | -1 | | -09 | | -08 | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Description** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** |
| **Combinatorial Delays** | | | | | | | | | | | |
| F/G inputs to X/Y outputs | $T_{ILO}$ | | 1.6 | | 1.5 | | 1.3 | | 1.2 | | 1.1 |
| F/G inputs via H' to X/Y outputs | $T_{IHO}$ | | 2.7 | | 2.4 | | 2.2 | | 2.0 | | 1.9 |
| F/G inputs via transparent latch to Q outputs | $T_{ITO}$ | | 2.9 | | 2.6 | | 2.2 | | 2.0 | | 1.8 |
| C inputs via SR/H0 via H to X/Y outputs | $T_{HH0O}$ | | 2.5 | | 2.2 | | 2.0 | | 1.8 | | 1.8 |
| C inputs via H1 via H to X/Y outputs | $T_{HH1O}$ | | 2.4 | | 2.1 | | 1.9 | | 1.6 | | 1.5 |
| C inputs via DIN/H2 via H to X/Y outputs | $T_{HH2O}$ | | 2.5 | | 2.2 | | 2.0 | | 1.8 | | 1.8 |
| C inputs via EC, DIN/H2 to YQ, XQ output (bypass) | $T_{CBYP}$ | | 1.5 | | 1.3 | | 1.1 | | 1.0 | | 0.9 |
| **CLB Fast Carry Logic** | | | | | | | | | | | |
| Operand inputs (F1, F2, G1, G4) to $C_{OUT}$ | $T_{OPCY}$ | | 2.7 | | 2.3 | | 2.0 | | 1.6 | | 1.6 |
| Add/Subtract input (F3) to $C_{OUT}$ | $T_{ASCY}$ | | 3.3 | | 2.9 | | 2.5 | | 1.8 | | 1.8 |
| Initialization inputs (F1, F3) to $C_{OUT}$ | $T_{INCY}$ | | 2.0 | | 1.8 | | 1.5 | | 1.0 | | 0.9 |
| $C_{IN}$ through function generators to X/Y outputs | $T_{SUM}$ | | 2.8 | | 2.6 | | 2.4 | | 1.7 | | 1.5 |
| $C_{IN}$ to $C_{OUT}$, bypass function generators | $T_{BYP}$ | | 0.26 | | 0.23 | | 0.20 | | 0.14 | | 0.14 |
| Carry Net Delay, $C_{OUT}$ to $C_{IN}$ | $T_{NET}$ | | 0.32 | | 0.28 | | 0.25 | | 0.24 | | 0.24 |
| **Sequential Delays** | | | | | | | | | | | |
| Clock K to Flip-Flop outputs Q | $T_{CKO}$ | | 2.1 | | 1.9 | | 1.6 | | 1.5 | | 1.4 |
| Clock K to Latch outputs Q | $T_{CKLO}$ | | 2.1 | | 1.9 | | 1.6 | | 1.5 | | 1.4 |
| **Setup Time before Clock K** | | | | | | | | | | | |
| F/G inputs | $T_{ICK}$ | 1.1 | | 1.0 | | 0.9 | | 0.8 | | 0.8 | |
| F/G inputs via H | $T_{IHCK}$ | 2.2 | | 1.9 | | 1.7 | | 1.6 | | 1.5 | |
| C inputs via H0 through H | $T_{HH0CK}$ | 2.0 | | 1.7 | | 1.6 | | 1.4 | | 1.4 | |
| C inputs via H1 through H | $T_{HH1CK}$ | 1.9 | | 1.6 | | 1.4 | | 1.2 | | 1.1 | |
| C inputs via H2 through H | $T_{HH2CK}$ | 2.0 | | 1.7 | | 1.6 | | 1.4 | | 1.4 | |
| C inputs via DIN | $T_{DICK}$ | 0.9 | | 0.8 | | 0.7 | | 0.6 | | 0.6 | |
| C inputs via EC | $T_{ECCK}$ | 1.0 | | 0.9 | | 0.8 | | 0.7 | | 0.7 | |
| C inputs via S/R, going Low (inactive) | $T_{RCK}$ | 0.6 | | 0.5 | | 0.5 | | 0.4 | | 0.4 | |
| CIN input via F/G | $T_{CCK}$ | 2.3 | | 2.1 | | 1.9 | | 1.3 | | 1.2 | |
| CIN input via F/G and H | $T_{CHCK}$ | 3.4 | | 3.0 | | 2.7 | | 2.1 | | 2.0 | |
| **Hold Time after Clock K** | | | | | | | | | | | |
| F/G inputs | $T_{CKI}$ | 0 | | 0 | | 0 | | 0 | | 0 | |
| F/G inputs via H | $T_{CKIH}$ | 0 | | 0 | | 0 | | 0 | | 0 | |
| C inputs via SR/H0 through H | $T_{CKHH0}$ | 0 | | 0 | | 0 | | 0 | | 0 | |
| C inputs via H1 through H | $T_{CKHH1}$ | 0 | | 0 | | 0 | | 0 | | 0 | |
| C inputs via DIN/H2 through H | $T_{CKHH2}$ | 0 | | 0 | | 0 | | 0 | | 0 | |
| C inputs via DIN/H2 | $T_{CKDI}$ | 0 | | 0 | | 0 | | 0 | | 0 | |
| C inputs via EC | $T_{CKEC}$ | 0 | | 0 | | 0 | | 0 | | 0 | |
| C inputs via SR, going Low (inactive) | $T_{CKR}$ | 0 | | 0 | | 0 | | 0 | | 0 | |
| **Clock** | | | | | | | | | | | |
| Clock High time | $T_{CH}$ | 3.0 | | 2.8 | | 2.5 | | 2.3 | | 2.1 | |
| Clock Low time | $T_{CL}$ | 3.0 | | 2.8 | | 2.5 | | 2.3 | | 2.1 | |
| **Set/Reset Direct** | | | | | | | | | | | |
| Width (High) | $T_{RPW}$ | 3.0 | | 2.8 | | 2.5 | | 2.3 | | 2.3 | |
| Delay from C inputs via S/R, going High to Q | $T_{RIO}$ | | 3.7 | | 3.2 | | 2.8 | | 2.7 | | 2.6 |
| **Global Set/Reset** | | | | | | | | | | | |
| Minimum GSR Pulse Width | $T_{MRW}$ | | 19.8 | | 17.3 | | 15.0 | | 14.0 | | 14.0 |
| Delay from GSR input to any Q | $T_{MRQ}$ | See Table on page 85 for $T_{RRI}$ values per device. | | | | | | | | | |
| **Toggle Frequency (MHz)** (for export control) | $F_{TOG}$ (MHz) | | 166 | | 179 | | 200 | | 217 | | 238 |

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## CLB Single-Port RAM Synchronous (Edge-Triggered) Write Operation Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000XL devices and are expressed in nanoseconds unless otherwise noted.

| Single Port RAM | Speed Grade | | -3 | | -2 | | -1 | | -09 | | -08 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Size | Symbol | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max |
| **Write Operation** | | | | | | | | | | | | |
| Address write cycle time (clock K period) | 16x2<br>32x1 | $T_{WCS}$<br>$T_{WCTS}$ | 9.0<br>9.0 | | 8.4<br>8.4 | | 7.7<br>7.7 | | 7.4<br>7.4 | | 7.4<br>7.4 | |
| Clock K pulse width (active edge) | 16x2<br>32x1 | $T_{WPS}$<br>$T_{WPTS}$ | 4.5<br>4.5 | | 4.2<br>4.2 | | 3.9<br>3.9 | | 3.7<br>3.7 | | 3.7<br>3.7 | |
| Address setup time before clock K | 16x2<br>32x1 | $T_{ASS}$<br>$T_{ASTS}$ | 2.2<br>2.2 | | 2.0<br>2.0 | | 1.7<br>1.7 | | 1.7<br>1.7 | | 1.6<br>1.7 | |
| Address hold time after clock K | 16x2<br>32x1 | $T_{AHS}$<br>$T_{AHTS}$ | 0<br>0 | | 0<br>0 | | 0<br>0 | | 0<br>0 | | 0<br>0 | |
| DIN setup time before clock K | 16x2<br>32x1 | $T_{DSS}$<br>$T_{DSTS}$ | 2.0<br>2.5 | | 1.9<br>2.3 | | 1.7<br>2.1 | | 1.7<br>2.1 | | 1.7<br>2.1 | |
| DIN hold time after clock K | 16x2<br>32x1 | $T_{DHS}$<br>$T_{DHTS}$ | 0<br>0 | | 0<br>0 | | 0<br>0 | | 0<br>0 | | 0<br>0 | |
| WE setup time before clock K | 16x2<br>32x1 | $T_{WSS}$<br>$T_{WSTS}$ | 2.0<br>1.8 | | 1.8<br>1.7 | | 1.6<br>1.5 | | 1.6<br>1.5 | | 1.6<br>1.5 | |
| WE hold time after clock K | 16x2<br>32x1 | $T_{WHS}$<br>$T_{WHTS}$ | 0<br>0 | | 0<br>0 | | 0<br>0 | | 0<br>0 | | 0<br>0 | |
| Data valid after clock K | 16x2<br>32x1 | $T_{WOS}$<br>$T_{WOTS}$ | | 6.8<br>8.1 | | 6.3<br>7.5 | | 5.8<br>6.9 | | 5.8<br>6.7 | | 5.7<br>6.7 |
| **Read Operation** | | | | | | | | | | | | |
| Address read cycle time | 16x2<br>32x1 | $T_{RC}$<br>$T_{RCT}$ | 4.5<br>6.5 | | 3.1<br>5.5 | | 2.6<br>3.8 | | 2.6<br>3.8 | | 2.6<br>3.8 | |
| Data Valid after address change (no Write Enable) | 16x2<br>32x1 | $T_{ILO}$<br>$T_{IHO}$ | | 1.6<br>2.7 | | 1.5<br>2.4 | | 1.3<br>2.2 | | 1.2<br>2.0 | | 1.1<br>1.9 |
| Address setup time before clock K | 16x2<br>32x1 | $T_{ICK}$<br>$T_{IHCK}$ | 1.1<br>2.2 | | 1.0<br>1.9 | | 0.9<br>1.7 | | 0.8<br>1.6 | | 0.8<br>1.5 | |

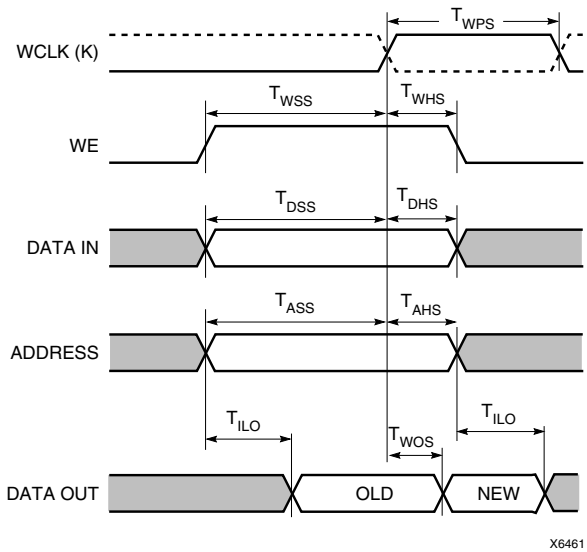
## CLB Dual-Port RAM Synchronous (Edge-Triggered) Write Operation Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000XL devices and are expressed in nanoseconds unless otherwise noted.

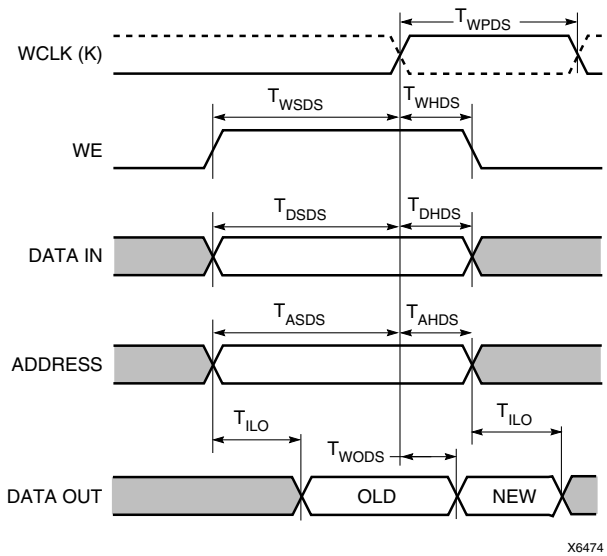
| Dual Port RAM | Speed Grade | | -3 | | -2 | | --1 | | -09 | | -08 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Size | Symbol | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max |
| | | | | | | | | | | | | |
| Address write cycle time (clock K period) | 16x1 | $T_{WCDS}$ | 9.0 | | 8.4 | | 7.7 | | 7.4 | | 7.4 | |
| Clock K pulse width (active edge) | 16x1 | $T_{WPDS}$ | 4.5 | | 4.2 | | 3.9 | | 3.7 | | 3.7 | |
| Address setup time before clock K | 16x1 | $T_{ASDS}$ | 2.5 | | 2.0 | | 1.7 | | 1.7 | | 1.6 | |
| Address hold time after clock K | 16x1 | $T_{AHDS}$ | 0 | | 0 | | 0 | | 0 | | 0 | |
| DIN setup time before clock K | 16x1 | $T_{DSDS}$ | 2.5 | | 2.3 | | 2.0 | | 2.0 | | 2.0 | |
| DIN hold time after clock K | 16x1 | $T_{DHDS}$ | 0 | | 0 | | 0 | | 0 | | 0 | |
| WE setup time before clock K | 16x1 | $T_{WSDS}$ | 1.8 | | 1.7 | | 1.6 | | 1.6 | | 1.6 | |
| WE hold time after clock K | 16x1 | $T_{WHDS}$ | 0 | | 0 | | 0 | | 0 | | 0 | |
| Data valid after clock K | 16x1 | $T_{WODS}$ | | 7.8 | | 7.3 | | 6.7 | | 6.7 | | 6.6 |

## CLB RAM Synchronous (Edge-Triggered) Write Timing Waveforms






**Single-Port RAM**




**Dual-Port RAM**

Product Obsolete/Under Obsolescence
XC4013XL-1PQ208C Xilinx Inc. IC FPGA 160 I/O 208QFP


# XC4000XL Pin-to-Pin Output Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. Values are expressed in nanoseconds unless otherwise noted.

## Output Flip-Flop, Clock to Out

| | | Speed Grade | All | -3 | -2 | -1 | -09 | -08 | Units |
|---|---|---|---|---|---|---|---|---|---|
| Description | Symbol | Device | Min | Max | Max | Max | Max | Max | |
| Global Low Skew Clock to Output using Output Flip Flop | $T_{ICKOF}$ | XC4002XL | 1.2 | 7.1 | 6.1 | 5.4 | 5.1 | | ns |
| | | XC4005XL | 1.3 | 7.7 | 6.6 | 5.8 | 5.4 | | ns |
| | | XC4010XL | 1.4 | 8.2 | 7.1 | 6.2 | 5.8 | | ns |
| | | XC4013XL | 1.5 | 8.6 | 7.4 | 6.5 | 6.1 | 5.6 | ns |
| | | XC4020XL | 1.6 | 9.0 | 7.8 | 6.8 | 6.4 | | ns |
| | | XC4028XL | 1.8 | 9.4 | 8.1 | 7.1 | 6.7 | | ns |
| | | XC4036XL | 2.0 | 9.8 | 8.5 | 7.4 | 7.0 | 6.4 | ns |
| | | XC4044XL | 2.1 | 10.3 | 8.9 | 7.8 | 7.4 | | ns |
| | | XC4052XL | 2.2 | 10.7 | 9.3 | 8.3 | 7.9 | | ns |
| | | XC4062XL | 2.3 | 11.3 | 9.7 | 8.5 | 8.1 | 7.3 | ns |
| | | XC4085XL | 2.5 | 12.2 | 10.5 | 9.5 | 9.0 | | ns |
| For output SLOW option add | $T_{SLOW}$ | All Devices | 0.5 | 3.0 | 2.5 | 2.0 | 1.7 | 1.6 | ns |

Notes: Clock-to-out minimum delay is measured with the fastest route and the lightest load, Clock-to-out maximum delay is measured using the farthest distance and a reference load of one clock pin (IK or OK) per IOB as well as driving all accessible CLB flip-flops. For designs with a smaller number of clock loads, the pad-to-IOB clock pin delay as determined by the static timing analyzer (TRCE) can be added to the AC parameter Tokpof and used as a worst-case pin-to-pin clock-to-out delay for clocked outputs for FAST mode configurations.
Output timing is measured at ~50% $V_{CC}$ threshold with 50 pF external capacitive load. For different loads, see Figure 1.

## Capacitive Load Factor

Figure 1 shows the relationship between I/O output delay and load capacitance. It allows a user to adjust the specified output delay if the load capacitance is different than 50 pF. For example, if the actual load capacitance is 120 pF, add 2.5 ns to the specified delay. If the load capacitance is 20 pF, subtract 0.8 ns from the specified output delay.

Figure 1 is usable over the specified operating conditions of voltage and temperature and is independent of the output slew rate control.

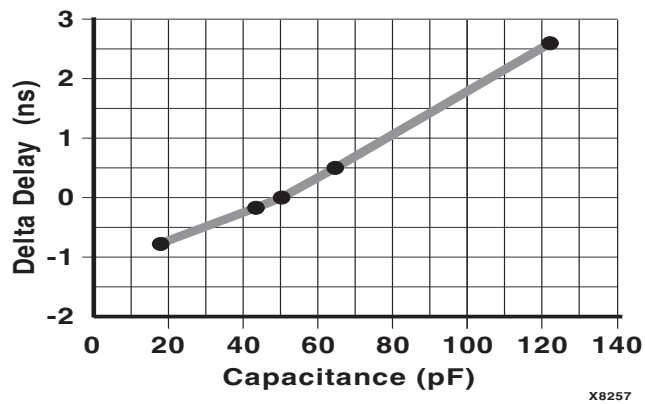



**Figure 1: Delay Factor at Various Capacitive Loads**

## Output Flip-Flop, Clock to Out, BUFGE #s 1, 2, 5, and 6

| | | Speed Grade | All | -3 | -2 | -1 | -09 | -08 | Units |
|---|---|---|---|---|---|---|---|---|---|
| Description | Symbol | Device | Min | Max | Max | Max | Max | Max | |
| Global Early Clock to Output using Output Flip Flop. Values are for BUFGE #s 1, 2, 5, and 6. | $T_{ICKEOF}$ | XC4002XL | 1.0 | 6.6 | 5.7 | 5.1 | 4.8 | | ns |
| | | XC4005XL | 1.2 | 6.9 | 6.1 | 5.5 | 5.2 | | ns |
| | | XC4010XL | 1.2 | 7.2 | 6.2 | 5.5 | 5.3 | | ns |
| | | XC4013XL | 1.3 | 7.4 | 6.4 | 5.6 | 5.3 | 4.8 | ns |
| | | XC4020XL | 1.3 | 7.6 | 6.5 | 5.9 | 5.6 | | ns |
| | | XC4028XL | 1.2 | 7.8 | 6.7 | 5.9 | 5.6 | | ns |
| | | XC4036XL | 1.2 | 8.1 | 7.0 | 6.1 | 5.8 | 5.2 | ns |
| | | XC4044XL | 1.1 | 8.5 | 7.3 | 6.4 | 6.0 | | ns |
| | | XC4052XL | 1.2 | 9.0 | 7.8 | 6.8 | 6.6 | | ns |
| | | XC4062XL | 1.2 | 9.9 | 8.6 | 7.5 | 7.0 | 6.3 | ns |
| | | XC4085XL | 1.3 | 10.8 | 9.4 | 8.5 | 7.9 | | ns |

Notes: Clock-to-out minimum delay is measured with the fastest route and the lightest load, Clock-to-out maximum delay is measured using the farthest distance and a reference load of one clock pin (IK or OK) per IOB as well as driving all accessible CLB flip-flops. For designs with a smaller number of clock loads, the pad-to-IOB clock pin delay as determined by the static timing analyzer (TRCE) can be added to the AC parameter Tokpof and used as a worst-case pin-to-pin clock-to-out delay for clocked outputs for FAST mode configurations.

Output timing is measured at ~50% $V_{CC}$ threshold with 50 pF external capacitive load. For different loads, see Figure 1.

## Output Flip-Flop, Clock to Out, BUFGE #s 3, 4, 7, and 8

| | | Speed Grade | All | -3 | -2 | -1 | -09 | -08 | Units |
|---|---|---|---|---|---|---|---|---|---|
| Description | Symbol | Device | Min | Max | Max | Max | Max | Max | |
| Global Early Clock to Output using Output Flip Flop. Values are for BUFGE #s 3, 4, 7, and 8. | $T_{ICKEOF}$ | XC4002XL | 1.3 | 7.8 | 6.8 | 5.9 | 5.3 | | ns |
| | | XC4005XL | 1.5 | 8.1 | 7.1 | 6.5 | 6.1 | | ns |
| | | XC4010XL | 1.6 | 8.5 | 7.4 | 6.6 | 6.3 | | ns |
| | | XC4013XL | 1.6 | 8.8 | 7.6 | 6.7 | 6.4 | 5.7 | ns |
| | | XC4020XL | 1.7 | 9.1 | 7.9 | 7.2 | 6.8 | | ns |
| | | XC4028XL | 1.7 | 9.4 | 8.2 | 7.2 | 6.9 | | ns |
| | | XC4036XL | 1.8 | 9.7 | 8.5 | 7.5 | 7.2 | 6.4 | ns |
| | | XC4044XL | 1.9 | 10.1 | 8.8 | 7.8 | 7.3 | | ns |
| | | XC4052XL | 2.0 | 10.5 | 9.1 | 8.1 | 7.9 | | ns |
| | | XC4062XL | 2.0 | 10.9 | 9.5 | 8.6 | 8.1 | 7.3 | ns |
| | | XC4085XL | 2.2 | 11.8 | 10.3 | 9.3 | 8.8 | | ns |

Notes: Clock-to-out minimum delay is measured with the fastest route and the lightest load, Clock-to-out maximum delay is measured using the farthest distance and a reference load of one clock pin (IK or OK) per IOB as well as driving all accessible CLB flip-flops. For designs with a smaller number of clock loads, the pad-to-IOB clock pin delay as determined by the static timing analyzer (TRCE) can be added to the AC parameter Tokpof and used as a worst-case pin-to-pin clock-to-out delay for clocked outputs for FAST mode configurations.

Output timing is measured at ~50% $V_{CC}$ threshold with 50 pF external capacitive load. For different loads, see Figure 1.

Product Obsolete/Under Obsolescence
XC4013XL-1PQ208C Xilinx Inc. IC FPGA 160 I/O 208QFP


## XC4000XL Pin-to-Pin Input Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. Values are expressed in nanoseconds unless otherwise noted

### Global Low Skew Clock, Set-Up and Hold

| | | Speed Grade | -3 | -2 | -1 | -09 | -08 | Units |
|---|---|---|---|---|---|---|---|---|
| **Description** | **Symbol** | **Device** | **Min** | **Min** | **Min** | **Min** | **Min** | |
| Input Setup and Hold Times | | | | | | | | |
| **No Delay** | $T_{PSN}/T_{PHN}$ | XC4002XL | 2.5 / 1.5 | 2.2 / 1.3 | 1.9 / 1.2 | 1.7 / 1.0 | | ns |
| Global Low Skew Clock and IFF | | XC4005XL | 1.2 / 2.6 | 1.1 / 2.2 | 0.9 / 2.0 | 0.8 / 1.7 | | ns |
| Global Low Skew Clock and FCL | | XC4010XL | 1.2 / 3.0 | 1.1 / 2.6 | 0.9 / 2.3 | 0.8 / 2.0 | | ns |
| | | XC4013XL | 1.2 / 3.2 | 1.1 / 2.8 | 0.9 / 2.4 | 0.8 / 2.1 | 0.8 / 2.1 | ns |
| | | XC4020XL | 1.2 / 3.7 | 1.1 / 3.2 | 0.9 / 2.8 | 0.8 / 2.4 | | ns |
| | | XC4028XL | 1.2 / 4.4 | 1.1 / 3.8 | 0.9 / 3.3 | 0.8 / 2.9 | | ns |
| | | XC4036XL | 1.2 / 5.5 | 1.1 / 4.8 | 0.9 / 4.1 | 0.8 / 3.6 | 0.8 / 3.6 | ns |
| | | XC4044XL | 1.2 / 5.8 | 1.1 / 5.0 | 0.9 / 4.4 | 0.8 / 3.8 | | ns |
| | | XC4052XL | 1.2 / 7.1 | 1.1 / 6.2 | 0.9 / 5.4 | 0.8 / 4.7 | | ns |
| | | XC4062XL | 1.2 / 7.0 | 1.1 / 6.1 | 0.9 / 5.3 | 0.8 / 4.6 | 0.8 / 4.6 | ns |
| | | XC4085XL | 1.2 / 9.4 | 1.1 / 8.2 | 0.9 / 7.1 | 0.8 / 6.2 | | ns |
| **Partial Delay** | $T_{PSP}/T_{PHP}$ | XC4002XL | 8.4 / 0.0 | 7.3 / 0.0 | 6.3 / 0.0 | 5.5 / 0.0 | | ns |
| Global Low Skew Clock and IFF | | XC4005XL | 10. 5 / 0.0 | 9.1 / 0.0 | 7.9 / 0.0 | 6.9 / 0.0 | | ns |
| Global Low Skew Clock and FCL | | XC4010XL | 11.1 / 0.0 | 9.7 / 0.0 | 8.4 / 0.0 | 7.3 / 0.0 | | ns |
| | | XC4013XL* | 6.1 / 1.0 | 5.3 / 1.0 | 4.6 / 1.0 | 4.0 / 1.0 | 3.7 / 0.5 | ns |
| | | XC4020XL | 11.9 / 1.0 | 10.3 / 1.0 | 9.0 / 1.0 | 7.8 / 1.0 | | ns |
| | | XC4028XL | 12.3 / 1.0 | 10.7 / 1.0 | 9.3 / 1.0 | 8.1 / 1.0 | | ns |
| | | XC4036XL* | 6.4 / 1.0 | 5.6 / 1.0 | 4.8 / 1.0 | 4.2 / 1.0 | 4.0/ 0.8 | ns |
| | | XC4044XL | 13.1 / 1.0 | 11.4 / 1.0 | 9.9 / 1.0 | 8.6 / 1.0 | | ns |
| | | XC4052XL | 11.9 / 1.0 | 10.3 / 1.0 | 9.0 / 1.0 | 7.8 / 1.0 | | ns |
| | | XC4062XL* | 6.7 / 1.2 | 5.8 / 1.2 | 5.1 / 1.2 | 4.4 / 1.2 | 4.2/ 1.0 | ns |
| | | XC4085XL | 12.9 / 1.2 | 11.2 / 1.2 | 9.8 / 1.2 | 8.5 / 1.2 | | ns |
| **Full Delay** | $T_{PSD}/T_{PHD}$ | XC4002XL | 6.8 / 0.0 | 6.0 / 0.0 | 5.2 / 0.0 | 4.5 / 0.0 | | ns |
| Global Low Skew Clock and IFF | | XC4005XL | 8.8 / 0.0 | 7.6 / 0.0 | 6.6 / 0.0 | 5.6 / 0.0 | | ns |
| | | XC4010XL | 9.0 / 0.0 | 7.8 / 0.0 | 6.8 / 0.0 | 5.8 / 0.0 | | ns |
| | | XC4013XL* | 6.4 / 0.0 | 6.0 / 0.0 | 5.6 / 0.0 | 4.8 / 0.0 | 4.8 / 0.0 | ns |
| | | XC4020XL | 8.8 / 0.0 | 7.6 / 0.0 | 6.6 / 0.0 | 6.2 / 0.0 | | ns |
| | | XC4028XL | 9.3 / 0.0 | 8.1 / 0.0 | 7.0 / 0.0 | 6.4 / 0.0 | | ns |
| | | XC4036XL* | 6.6 / 0.0 | 6.2 / 0.0 | 5.8 / 0.0 | 5.3 / 0.0 | 5.3 / 0.0 | ns |
| | | XC4044XL | 10.6 / 0.0 | 9.2 / 0.0 | 8.0 / 0.0 | 6.8 / 0.0 | | ns |
| | | XC4052XL | 11.2 / 0.0 | 9.7 / 0.0 | 8.4 / 0.0 | 7.0 / 0.0 | | ns |
| | | XC4062XL* | 6.8 / 0.0 | 6.4 / 0.0 | 6.0 / 0.0 | 5.5 / 0.0 | 5.5 / 0.0 | ns |
| | | XC4085XL | 12.7 / 0.0 | 11.0 / 0.0 | 9.6 / 0.0 | 8.4 / 0.0 | | ns |

IFF = Input Flip-Flop or Latch

* The XC4013XL, XC4036XL, and 4062XL have significantly faster partial and full delay setup times than other devices.

Notes: Input setup time is measured with the fastest route and the lightest load.

Input hold time is measured using the furthest distance and a reference load of one clock pin per IOB as well as driving all accessible CLB flip-flops. For designs with a smaller number of clock loads, the pad-to-IOB clock pin delay as determined by the static timing analyzer (TRCE) can be used as a worst-case pin-to-pin no-delay input hold specification.

## Global Early Clock BUFGEs 1, 2, 5, and 6 Set-up and Hold for IFF and FCL

| | | Speed Grade | -3 | -2 | -1 | -09 | -08 | Units |
|---|---|---|---|---|---|---|---|---|
| **Description** | **Symbol** | **Device** | **Min** | **Min** | **Min** | **Min** | **Min** | |
| Input Setup and Hold Times | | | | | | | | |
| **No Delay** | | XC4002XL | 2.8 / 1.5 | 2.5 / 1.3 | 2.2 / 1.2 | 1.9 / 1.0 | | ns |
| Global Early Clock and IFF | $T_{PSEN}/T_{PHEN}$ | XC4005XL | 1.2 / 4.1 | 1.1 / 3.6 | 0.9 / 3.1 | 0.8 / 2.7 | | ns |
| Global Early Clock and | $T_{PFSEN}/T_{PFHEN}$ | XC4010XL | 1.2 / 4.4 | 1.1 / 3.8 | 0.9 / 3.3 | 0.8 / 2.9 | | ns |
| FCL | | XC4013XL | 1.2 / 4.7 | 1.1 / 4.1 | 0.9 / 3.6 | 0.8 / 3.1 | 0.5 / 2.7 | ns |
| | | XC4020XL | 1.2 / 4.6 | 1.1 / 4.0 | 0.9 / 3.5 | 0.8 / 3.0 | | ns |
| | | XC4028XL | 1.2 / 5.3 | 1.1 / 4.6 | 0.9 / 4.0 | 0.8 / 3.5 | | ns |
| | | XC4036XL | 1.2 / 6.7 | 1.1 / 5.8 | 0.9 / 5.1 | 0.8 / 4.4 | 0.5 / 3.7 | ns |
| | | XC4044XL | 1.2 / 6.5 | 1.1 / 5.7 | 0.9 / 4.9 | 0.8 / 4.3 | | ns |
| | | XC4052XL | 1.2 / 6.7 | 1.1 / 5.8 | 0.9 / 5.1 | 0.8 / 4.4 | | ns |
| | | XC4062XL | 1.2 / 8.4 | 1.1 / 7.3 | 0.9 / 6.3 | 0.8 / 5.5 | 0.5 / 4.7 | ns |
| | | XC4085XL | 1.2 / 8.7 | 1.1 / 7.5 | 0.9 / 6.6 | 0.8 / 5.7 | | ns |
| **Partial Delay** | | XC4002XL | 8.1 / 0.9 | 7.0 / 0.8 | 6.1 / 0.7 | 5.3 / 0.6 | | ns |
| Global Early Clock and IFF | $T_{PSEP}/T_{PHEP}$ | XC4005XL | 9.0 / 0.0 | 8.5 / 0.0 | 8.0 / 0.0 | 7.5 / 0.0 | | ns |
| Global Early Clock and | $T_{PFSEP}/T_{PFHEP}$ | XC4010XL | 11.9 / 0.0 | 10.4 / 0.0 | 9.0 / 0.0 | 8.0 / 0.0 | | ns |
| FCL | | XC4013XL* | 6.4 / 0.0 | 5.9 / 0.0 | 5.4 / 0.0 | 4.9 / 0.0 | 4.4 / 0.0 | ns |
| | | XC4020XL | 10.8 / 0.0 | 10.3 / 0.0 | 9.8 / 0.0 | 9.0 / 0.0 | | ns |
| | | XC4028XL | 14.0 / 0.0 | 12.2 / 0.0 | 10.6 / 0.0 | 9.8 / 0.0 | | ns |
| | | XC4036XL* | 7.0 / 0.0 | 6.6 / 0.0 | 6.2 / 0.0 | 5.2 / 0.0 | 4.7 / 0.0 | ns |
| | | XC4044XL | 14.6 / 0.0 | 12.7 / 0.0 | 11.0 / 0.0 | 10.8 / 0.0 | | ns |
| | | XC4052XL | 16.4 / 0.0 | 14.3 / 0.0 | 12.4 / 0.0 | 11.4 / 0.0 | | ns |
| | | XC4062XL* | 9.0 / 0.8 | 8.6 / 0.8 | 8.2 / 0.8 | 7.0 / 0.8 | 6.3 / 0.5 | ns |
| | | XC4085XL | 16.7 / 0.0 | 14.5 / 0.0 | 12.6 / 0.0 | 11.6 / 0.0 | | ns |
| **Full Delay** | | XC4002XL | 6.7 / 0.0 | 5.8 / 0.0 | 5.1 / 0.0 | 4.4 / 0.0 | | ns |
| Global Early Clock and IFF | $T_{PSED}/T_{PHED}$ | XC4005XL | 10.8 / 0.0 | 9.4 / 0.0 | 8.2 / 0.0 | 7.1 / 0.0 | | ns |
| | | XC4010XL | 10.3 / 0.0 | 9.0 / 0.0 | 7.8 / 0.0 | 6.8 / 0.0 | | ns |
| | | XC4013XL* | 10.0 / 0.0 | 8.7 / 0.0 | 7.6 / 0.0 | 6.6 / 0.0 | 6.0 / 0.0 | ns |
| | | XC4020XL | 12.0 / 0.0 | 10.4 / 0.0 | 9.1 / 0.0 | 7.9 / 0.0 | | ns |
| | | XC4028XL | 12.6 / 0.0 | 11.0 / 0.0 | 9.5 / 0.0 | 8.3 / 0.0 | | ns |
| | | XC4036XL* | 12.2 / 0.0 | 10.6 / 0.0 | 9.2 / 0.0 | 8.0 / 0.0 | 7.2 / 0.0 | ns |
| | | XC4044XL | 13.8 / 0.0 | 12.0 / 0.0 | 10.5 / 0.0 | 9.1 / 0.0 | | ns |
| | | XC4052XL | 14.1 / 0.0 | 12.3 / 0.0 | 10.7 / 0.0 | 9.3 / 0.0 | | ns |
| | | XC4062XL* | 13.1 / 0.0 | 11.4 / 0.0 | 9.9 / 0.0 | 8.6 / 0.0 | 7.8 / 0.0 | ns |
| | | XC4085XL | 17.9 / 0.0 | 15.6 / 0.0 | 13.6 / 0.0 | 11.8 / 0.0 | | ns |

IFF = Input Flip-Flop or Latch, FCL = Fast Capture Latch
* The XC4013XL, XC4036XL, and 4062XL have significantly faster partial and full delay setup times than other devices.
Notes: Input setup time is measured with the fastest route and the lightest load.
Input hold time is measured using the furthest distance and a reference load of one clock pin per IOB as well as driving all accessible CLB flip-flops. For designs with a smaller number of clock loads, the pad-to-IOB clock pin delay as determined by the static timing analyzer (TRCE) can be used as a worst-case pin-to-pin no-delay input hold specification.

Product Obsolete/Under Obsolescence
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## Global Early Clock BUFGEs 3, 4, 7, and 8 Set-up and Hold for IFF and FCL

| | | Speed Grade | -3 | -2 | -1 | -09 | -08 | Units |
|---|---|---|---|---|---|---|---|---|
| **Description** | **Symbol** | **Device** | **Min** | **Min** | **Min** | **Min** | **Min** | |
| Input Setup & Hold Times | | | | | | | | |
| **No Delay** | | XC4002XL | 3.0 / 2.0 | 2.6 / 1.7 | 2.3 / 1.5 | 2.0 / 1.3 | | ns |
| Global Early Clock and | $T_{PSEN}/T_{PHEN}$ | XC4005XL | 1.2 / 4.1 | 1.1 / 3.6 | 0.9 / 3.1 | 0.8 / 2.7 | | ns |
| IFF | $T_{PFSEN}/T_{PFHEN}$ | XC4010XL | 1.2 / 4.4 | 1.1 / 3.8 | 0.9 / 3.3 | 0.8 / 2.9 | | ns |
| Global Early Clock and | | XC4013XL | 1.2 / 4.7 | 1.1 / 4.1 | 0.9 / 3.6 | 0.8 / 3.1 | 0.5 / 2.7 | ns |
| FCL | | XC4020XL | 1.2 / 4.6 | 1.1 / 4.0 | 0.9 / 3.5 | 0.8 / 3.0 | | ns |
| | | XC4028XL | 1.2 / 5.3 | 1.1 / 4.6 | 0.9 / 4.0 | 0.8 / 3.5 | | ns |
| | | XC4036XL | 1.2 / 6.7 | 1.1 / 5.8 | 0.9 / 5.1 | 0.8 / 4.4 | 0.5 / 3.7 | ns |
| | | XC4044XL | 1.2 / 6.5 | 1.1 / 5.7 | 0.9 / 4.9 | 0.8 / 4.3 | | ns |
| | | XC4052XL | 1.2 / 6.7 | 1.1 / 5.8 | 0.9 / 5.1 | 0.8 / 4.4 | | ns |
| | | XC4062XL | 1.2 / 8.4 | 1.1 / 7.3 | 0.9 / 6.3 | 0.8 / 5.5 | 0.5 / 4.7 | ns |
| | | XC4085XL | 1.2 / 8.7 | 1.1 / 7.5 | 0.9 / 6.6 | 0.8 / 5.7 | | ns |
| **Partial Delay** | | XC4002XL | 7.3 / 1.5 | 6.4 / 1.3 | 5.5 / 1.2 | 4.8 / 1.0 | | ns |
| Global Early Clock and | $T_{PSEP}/T_{PHEP}$ | XC4005XL | 8.4 / 0.0 | 7.9 / 0.0 | 7.4 / 0.0 | 7.2 / 0.0 | | ns |
| IFF | $T_{PFSEP}/T_{PFHEP}$ | XC4010XL | 10.3 / 0.0 | 9.0 / 0.0 | 7.8 / 0.0 | 7.4 / 0.0 | | ns |
| Global Early Clock and | | XC4013XL* | 5.4 / 0.0 | 4.9 / 0.0 | 4.4 / 0.0 | 4.3 / 0.0 | 4.0 / 0.0 | ns |
| FCL | | XC4020XL | 9.8 / 0.0 | 9.3 / 0.0 | 8.8 / 0.0 | 8.5 / 0.0 | | ns |
| | | XC4028XL | 12.7 / 0.0 | 11.0 / 0.0 | 9.6 / 0.0 | 9.3 / 0.0 | | ns |
| | | XC4036XL* | 6.4 / 0.8 | 5.9 / 0.8 | 5.4 / 0.8 | 5.0 / 0.8 | 4.6 / 0.2 | ns |
| | | XC4044XL | 13.8 / 0.0 | 12.0 / 0.0 | 10.4 / 0.0 | 10.2 / 0.0 | | ns |
| | | XC4052XL | 14.5 / 0.0 | 12.7 / 0.0 | 11.0 / 0.0 | 10.7 / 0.0 | | ns |
| | | XC4062XL* | 8.4 / 1.5 | 7.9 / 1.5 | 7.4 / 1.5 | 6.8 / 1.5 | 6.2 / 0.0 | ns |
| | | XC4085XL | 14.5 / 0.0 | 12.7 / 0.0 | 11.0 / 0.0 | 10.8 / 0.0 | | ns |
| **Full Delay** | | XC4002XL | 5.9 / 0.0 | 5.2 / 0.0 | 4.5 / 0.0 | 3.9 / 0.0 | | ns |
| Global Early Clock and | $T_{PSED}/T_{PHED}$ | XC4005XL | 10.8 / 0.0 | 9.4 / 0.0 | 8.2 / 0.0 | 7.1 / 0.0 | | ns |
| IFF | | XC4010XL | 10.3 / 0.0 | 9.0 / 0.0 | 7.8 / 0.0 | 6.8 / 0.0 | | ns |
| | | XC4013XL* | 10.0 / 0.0 | 8.7 / 0.0 | 7.6 / 0.0 | 6.6 / 0.0 | 6.0 / 0.0 | ns |
| | | XC4020XL | 12.0 / 0.0 | 10.4 / 0.0 | 9.1 / 0.0 | 7.9 / 0.0 | | ns |
| | | XC4028XL | 12.6 / 0.0 | 11.0 / 0.0 | 9.5 / 0.0 | 8.3 / 0.0 | | ns |
| | | XC4036XL* | 12.2 / 0.0 | 10.6 / 0.0 | 9.2 / 0.0 | 8.0 / 0.0 | 7.2 / 0.0 | ns |
| | | XC4044XL | 13.8 / 0.0 | 12.0 / 0.0 | 10.5 / 0.0 | 9.1 / 0.0 | | ns |
| | | XC4052XL | 14.1 / 0.0 | 12.3 / 0.0 | 10.7 / 0.0 | 9.3 / 0.0 | | ns |
| | | XC4062XL* | 13.1 / 0.0 | 11.4 / 0.0 | 9.9 / 0.0 | 8.6 / 0.0 | 7.8 / 0.0 | ns |
| | | XC4085XL | 17.9 / 0.0 | 15.6 / 0.0 | 13.6 / 0.0 | 11.8 / 0.0 | | ns |

* The XC4013XL, XC4036XL, and 4062XL have significantly faster partial and full delay setup times than other devices.
IFF = Input Flip Flop or Latch. FCL = Fast Capture Latch
Notes: Input setup time is measured with the fastest route and the lightest load.
Input hold time is measured using the furthest distance and a reference load of one clock pin per IOB as well as driving all accessible CLB flip-flops. For designs with a smaller number of clock loads, the pad-to-IOB clock pin delay as determined by the static timing analyzer (TRCE) can be used as a worst-case pin-to-pin no-delay input hold specification.

## XC4000XL IOB Input Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

| | | Speed Grade | -3 | -2 | -1 | -09 | -08 | Units |
|---|---|---|---|---|---|---|---|---|
| **Description** | **Symbol** | **Device** | **Min** | **Min** | **Min** | **Min** | **Min** | |
| **Clocks** | | | | | | | | |
| Clock Enable (EC) to Clock (IK) | $T_{ECIK}$ | All devices | 0.1 | 0.1 | 0.1 | 0.1 | 0.1 | ns |
| Delay from FCL enable (OK) active edge to IFF clock (IK) active edge | $T_{OKIK}$ | XC4002XL | 3.0 | 2.7 | 2.3 | 2.3 | | ns |
| | | XC4013, 36, 62XL | 2.2 | 1.9 | 1.6 | 1.6 | 1.6 | ns |
| | | Balance of Family | 2.2 | 1.9 | 1.6 | 1.6 | | ns |
| **Setup Times** | | | | | | | | |
| Pad to Clock (IK), no delay | $T_{PICK}$ | XC4002XL | 2.6 | 2.3 | 2.0 | 2.0 | | ns |
| | | XC4013, 36, 62XL | 1.7 | 1.5 | 1.3 | 1.3 | 1.2 | ns |
| | | Balance of Family | 1.7 | 1.5 | 1.3 | 1.3 | | ns |
| Pad to Clock (IK), via transparent Fast Capture Latch, no delay | $T_{PICKF}$ | XC4002XL | 3.2 | 2.9 | 2.5 | 2.4 | | ns |
| | | XC4013, 36, 62XL | 2.3 | 2.0 | 1.8 | 1.7 | 1.6 | ns |
| | | Balance of Family | 2.3 | 2.0 | 1.8 | 1.7 | | ns |
| Pad to Fast Capture Latch Enable (OK), no delay | $T_{POCK}$ | XC4013, 36, 62XL | 1.2 | 1.0 | 0.9 | 0.9 | 0.9 | ns |
| | | Balance of Family | 1.2 | 1.0 | 0.9 | 0.9 | | ns |
| **Hold Times** | | | | | | | | |
| All Hold Times | | All Devices | 0 | 0 | 0 | 0 | 0 | |
| **Global Set/Reset** | | | | | | | | |
| Minimum GSR Pulse Width | $T_{MRW}$ | All devices | 19.8 | 17.3 | 15.0 | 14.0 | 14.0 | ns |
| **Global Set/Reset** | | | Max | Max | Max | Max | Max | |
| Delay from GSR input to any Q | $T_{RRI}$* | XC4002XL | 9.8 | 8.5 | 7.4 | 7.0 | | ns |
| | | XC4005XL | 11.3 | 9.8 | 8.5 | 8.1 | | ns |
| | | XC4010XL | 13.9 | 12.1 | 10.5 | 10.0 | | ns |
| | | XC4013XL | 15.9 | 13.8 | 12.0 | 11.4 | 10.9 | ns |
| | | XC4020XL | 18.6 | 16.1 | 14.0 | 13.3 | | ns |
| | | XC4028XL | 20.5 | 17.9 | 15.5 | 14.3 | | ns |
| | | XC4036XL | 22.5 | 19.6 | 17.0 | 16.2 | 16.2 | ns |
| | | XC4044XL | 25.1 | 21.9 | 19.0 | 18.1 | | ns |
| | | XC4052XL | 27.2 | 23.6 | 20.5 | 19.5 | | ns |
| | | XC4062XL | 29.1 | 25.3 | 22.0 | 20.9 | 20.4 | ns |
| | | XC4085XL | 34.4 | 29.9 | 26.0 | 24.7 | | ns |
| **Propagation Delays** | | | | | | | | |
| Pad to I1, I2 | $T_{PID}$ | All devices | 1.6 | 1.4 | 1.2 | 1.1 | 1.0 | ns |
| Pad to I1, I2 via transparent input latch, no delay | $T_{PLI}$ | XC4002XL | 4.7 | 4.2 | 3.6 | 3.5 | | ns |
| | | XC4013, 36, 62XL | 3.1 | 2.7 | 2.4 | 2.2 | 2.1 | ns |
| | | Balance of Family | 3.1 | 2.7 | 2.4 | 2.2 | | ns |
| Pad to I1, I2 via transparent FCL and input latch, no delay | $T_{PFLI}$ | X4002XL | 5.4 | 4.7 | 4.1 | 3.9 | | ns |
| | | XC4013, 36, 62XL | 3.7 | 3.3 | 2.8 | 2.7 | 2.5 | ns |
| | | Balance of Family | 3.7 | 3.3 | 2.8 | 2.7 | | ns |
| Clock (IK) to I1, I2 (flip-flop) | $T_{IKRI}$ | All devices | 1.7 | 1.5 | 1.3 | 1.2 | 1.2 | ns |
| Clock (IK) to I1, I2 (latch enable, active Low) | $T_{IKLI}$ | All devices | 1.8 | 1.6 | 1.4 | 1.3 | 1.3 | ns |
| FCL Enable (OK) active edge to I1, I2 (via transparent standard input latch) | $T_{OKLI}$ | XC4002XL | 5.2 | 4.6 | 4.0 | 3.8 | | ns |
| | | XC4013, 36, 62XL | 3.6 | 3.1 | 2.7 | 2.6 | 2.5 | ns |
| | | Balance of Family | 3.6 | 3.1 | 2.7 | 2.6 | | ns |

IFF = Input Flip-Flop or Latch, FCL = Fast Capture Latch
* Indicates Minimum Amount of Time to Assure Valid Data.

Product Obsolete/Under Obsolescence
XC4013XL-1PQ208C Xilinx Inc. IC FPGA 160 I/O 208QFP


## XC4000XL IOB Output Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). For Propagation Delays, slew-rate = fast unless otherwise noted. Values are expressed in nanoseconds unless otherwise noted.

| | | -3 | | -2 | | -1 | | -09 | | -08 | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Description** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** |
| **Clocks** | | | | | | | | | | | |
| Clock High | $T_{CH}$ | 3.0 | | 2.8 | | 2.5 | | 2.3 | | 2.1 | |
| Clock Low | $T_{CL}$ | 3.0 | | 2.8 | | 2.5 | | 2.3 | | 2.1 | |
| **Propagation Delays** | | | | | | | | | | | |
| Clock (OK) to Pad | $T_{OKPOF}$ | | 5.0 | | 4.3 | | 3.8 | | 3.5 | | 3.3 |
| Output (O) to Pad | $T_{OPF}$ | | 4.1 | | 3.6 | | 3.1 | | 3.0 | | 2.8 |
| 3-state to Pad hi-Z (slew-rate independent) | $T_{TSHZ}$ | | 4.0 | | 3.5 | | 3.0 | | 2.9 | | 2.9 |
| 3-state to Pad active and valid | $T_{TSONF}$ | | 4.4 | | 3.8 | | 3.3 | | 3.3 | | 3.3 |
| Output (O) to Pad via Fast Output MUX | $T_{OFPF}$ | | 5.5 | | 4.8 | | 4.2 | | 4.0 | | 3.7 |
| Select (OK) to Pad via Fast MUX | $T_{OKFPF}$ | | 5.1 | | 4.5 | | 3.9 | | 3.7 | | 3.4 |
| **Setup and Hold Times** | | | | | | | | | | | |
| Output (O) to clock (OK) setup time | $T_{OOK}$ | 0.5 | | 0.4 | | 0.3 | | 0.3 | | 0.3 | |
| Output (O) to clock (OK) hold time | $T_{OKO}$ | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | |
| Clock Enable (EC) to clock (OK) setup time | $T_{ECOK}$ | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | |
| Clock Enable (EC) to clock (OK) hold time | $T_{OKEC}$ | 0.3 | | 0.2 | | 0.1 | | 0.0 | | 0.0 | |
| **Global Set/Reset** | | | | | | | | | | | |
| Minimum GSR pulse width | $T_{MRW}$ | 19.8 | | 17.3 | | 15.0 | | 14.0 | | 14.0 | |
| Delay from GSR input to any Pad | $T_{RPO}$* | | | | | | | | | | |
| XC4002XL | | | 14.3 | | 12.5 | | 10.9 | | 10.3 | | |
| XC4005XL | | | 15.9 | | 13.8 | | 12.0 | | 11.4 | | |
| XC4010XL | | | 18.5 | | 16.1 | | 14.0 | | 13.3 | | |
| XC4013XL | | | 20.5 | | 17.8 | | 15.5 | | 14.7 | | 14.0 |
| XC4020XL | | | 23.2 | | 20.1 | | 17.5 | | 16.6 | | |
| XC4028XL | | | 25.1 | | 21.9 | | 19.0 | | 17.6 | | |
| XC4036XL | | | 27.1 | | 23.6 | | 20.5 | | 19.4 | | 19.3 |
| XC4044XL | | | 29.7 | | 25.9 | | 22.5 | | 21.4 | | |
| XC4052XL | | | 31.7 | | 27.6 | | 24.0 | | 22.8 | | |
| XC4062XL | | | 33.7 | | 29.3 | | 25.5 | | 24.2 | | 23.5 |
| XC4085XL | | | 39.0 | | 33.9 | | 29.5 | | 28.0 | | |
| **Slew Rate Adjustment** | | | | | | | | | | | |
| For output SLOW option add | $T_{SLOW}$ | | 3.0 | | 2.5 | | 2.0 | | 1.7 | | 1.6 |

Note: Output timing is measured at ~50% $V_{CC}$ threshold, with 50 pF external capacitive loads.
* Indicates Minimum Amount of Time to Assure Valid Data.

Product Obsolete/Under Obsolescence
XC4013XL-1PQ208C Xilinx Inc. IC FPGA 160 I/O 208QFP


## Revision Control

| Version | Nature of Changes |
|---|---|
| 02/01/1999 (1.5) | Release included in the 1999 data book, section 6 |
| 05/14/1999 (1.6) | Replaced Electrical Specification and pinout pages for E, EX, and XL families with separate updates and added URL link on placeholder page for electrical specifications/pinouts for WebLINX users |
| 09/30/1999 (1.7) | Added Power-on specification. |
| 10/18/1999 (1.8) | Corrected posted file to include missing page (IOB Output Parameters). |
| 03/01/2013 (2.0) | The products listed in this data sheet are obsolete. See XCN08011 for further information. |

Product Obsolete/Under Obsolescence
XC4013XL-1PQ208C Xilinx Inc. IC FPGA 160 I/O 208QFP

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## OUR CERTIFICATE

A long-term cooperative relationship can be built between global customers and us by providing excellent products

| | |
|---|---|
| Business Type | Trading Company, Distributor/Wholesaler |
| Main Products | Electronic Integrated Circuit |
| Certifications | ISO9001 |
| Total Annual Revenue | US$2.5 Million - US$5 Million |
| Country / Region | Hongkong, China |
| Total Employees | 100 - 200 People |
| Year Established | 2018 |
| Main Markets | North America<br>South Asia<br>Western Europe |

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