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# Zynq-7000 SoC (Z-7007S, Z-7012S, Z-7014S, Z-7010, Z-7015, and Z-7020): DC and AC Switching Characteristics

DS187 (v1.20.1) July 2, 2018 **Product Specification**

## Introduction

The Zynq®-7000 SoCs are available in -3, -2, -1, and -1LI speed grades, with -3 having the highest performance. The -1LI devices can operate at either of two programmable logic (PL) $V_{CCINT}/V_{CCBRAM}$ voltages, 0.95V and 1.0V, and are screened for lower maximum static power. The speed specification of a -1LI device is the same as the -1 speed grade. When operated at PL $V_{CCINT}/V_{CCBRAM}$ = 0.95V, the -1LI static and dynamic power is reduced. Zynq-7000 device DC and AC characteristics are specified in commercial, extended, industrial and expanded (Q-temp) temperature ranges. Except for the operating temperature range or unless otherwise noted, all the DC and AC electrical parameters are the same for a particular speed grade (that is, the timing characteristics of a -1 speed grade industrial device are the same as for a -1 speed grade commercial device). However, only selected speed grades and/or devices are available in the commercial, extended, industrial, or Q-temp temperature ranges.

All supply voltage and junction temperature specifications are representative of worst-case conditions. The parameters included are common to popular designs and typical applications.

The available device/package combinations are outlined in:

- *Zynq-7000 SoC Overview* (DS190)
- *XA Zynq-7000 SoC Overview* (DS188)
- *Defense-grade Zynq-7000Q SoC Overview* (DS196)

This Zynq-7000 SoC data sheet, which covers the specifications for the XC7Z007S, XC7Z012S, XC7Z014S, XC7Z010, XA7Z010, XC7Z015, XC7Z020, XA7Z020, and XQ7Z020, complements the Zynq-7000 SoC documentation suite available on the Xilinx website at www.xilinx.com/zynq.

## DC Characteristics

*Table 1:* **Absolute Maximum Ratings(1)**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| **Processing System (PS)** | | | | |
| $V_{CCPINT}$ | PS internal logic supply voltage | –0.5 | 1.1 | V |
| $V_{CCPAUX}$ | PS auxiliary supply voltage | –0.5 | 2.0 | V |
| $V_{CCPLL}$ | PS PLL supply | –0.5 | 2.0 | V |
| $V_{CCO_DDR}$ | PS DDR I/O supply voltage | –0.5 | 2.0 | V |
| $V_{CCO_MIO}$(2) | PS MIO I/O supply voltage | –0.5 | 3.6 | V |
| $V_{PREF}$ | PS input reference voltage | –0.5 | 2.0 | V |
| $V_{PIN}$(2)(3)(4)(5) | PS MIO I/O input voltage | –0.40 | $V_{CCO_MIO}$ + 0.55 | V |
| | PS DDR I/O input voltage | –0.55 | $V_{CCO_DDR}$ + 0.55 | V |
| **Programmable Logic (PL)** | | | | |
| $V_{CCINT}$ | PL internal supply voltage | –0.5 | 1.1 | V |
| $V_{CCAUX}$ | PL auxiliary supply voltage | –0.5 | 2.0 | V |
| $V_{CCBRAM}$ | PL supply voltage for the block RAM memories | –0.5 | 1.1 | V |
| $V_{CCO}$ | PL supply voltage for HR I/O banks | –0.5 | 3.6 | V |
| $V_{REF}$ | Input reference voltage | –0.5 | 2.0 | V |

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*Table 1:* **Absolute Maximum Ratings(1) *(Cont'd)***

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $V_{IN}$(3)(4)(5) | I/O input voltage for HR I/O banks | –0.40 | $V_{CCO}$ + 0.55 | V |
| | I/O input voltage (when $V_{CCO}$ = 3.3V) for $V_{REF}$ and differential I/O standards except TMDS_33(6) | –0.40 | 2.625 | V |
| $V_{CCBATT}$ | Key memory battery backup supply | –0.5 | 2.0 | V |
| **GTP Transceiver (XC7Z015 Only)** | | | | |
| $V_{MGTAVCC}$ | Analog supply voltage for the GTP transmitter and receiver circuits | –0.5 | 1.1 | V |
| $V_{MGTAVTT}$ | Analog supply voltage for the GTP transmitter and receiver termination circuits | –0.5 | 1.32 | V |
| $V_{MGTREFCLK}$ | Reference clock absolute input voltage | –0.5 | 1.32 | V |
| $V_{IN}$ | Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage | –0.5 | 1.26 | V |
| $I_{DCIN-FLOAT}$ | DC input current for receiver input pins DC coupled RX termination = floating | – | 14 | mA |
| $I_{DCIN-MGTAVTT}$ | DC input current for receiver input pins DC coupled RX termination = $V_{MGTAVTT}$ | – | 12 | mA |
| $I_{DCIN-GND}$ | DC input current for receiver input pins DC coupled RX termination = GND | – | 6.5 | mA |
| $I_{DCOUT-FLOAT}$ | DC output current for transmitter pins DC coupled RX termination = floating | – | 14 | mA |
| $I_{DCOUT-MGTAVTT}$ | DC output current for transmitter pins DC coupled RX termination = $V_{MGTAVTT}$ | – | 12 | mA |
| **XADC** | | | | |
| $V_{CCADC}$ | XADC supply relative to GNDADC | –0.5 | 2.0 | V |
| $V_{REFP}$ | XADC reference input relative to GNDADC | –0.5 | 2.0 | V |
| **Temperature** | | | | |
| $T_{STG}$ | Storage temperature (ambient) | –65 | 150 | °C |
| $T_{SOL}$ | Maximum soldering temperature for Pb/Sn component bodies(7) | – | +220 | °C |
| | Maximum soldering temperature for Pb-free component bodies(7) | – | +260 | °C |
| $T_j$ | Maximum junction temperature(7) | – | +125 | °C |

**Notes:**

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. Applies to both MIO supply banks $V_{CCO_MIO0}$ and $V_{CCO_MIO1}$.
3. The lower absolute voltage specification always applies.
4. For I/O operation, refer to the *7 Series FPGAs SelectIO Resources User Guide* (UG471) or the *Zynq-7000 SoC Technical Reference Manual* (UG585).
5. The maximum limit applies to DC signals. For maximum undershoot and overshoot AC specifications, see Table 4.
6. See Table 11 for TMDS_33 specifications.
7. For soldering guidelines and thermal considerations, see the *Zynq-7000 SoC Packaging and Pinout Specification* (UG865).

*Table 2:* **Recommended Operating Conditions(1)(2)**

| Symbol | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| **PS** | | | | | |
| $V_{CCPINT}$ | PS internal logic supply voltage | 0.95 | 1.00 | 1.05 | V |
| $V_{CCPAUX}$ | PS auxiliary supply voltage | 1.71 | 1.80 | 1.89 | V |
| $V_{CCPLL}$ | PS PLL supply | 1.71 | 1.80 | 1.89 | V |
| $V_{CCO_DDR}$ | PS DDR I/O supply voltage | 1.14 | – | 1.89 | V |
| $V_{CCO_MIO}$(3) | PS MIO I/O supply voltage for MIO banks | 1.71 | – | 3.465 | V |

*Table 2:* **Recommended Operating Conditions(1)(2) *(Cont'd)***

| Symbol | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $V_{PIN}$(4) | PS DDR and MIO I/O input voltage | –0.20 | – | $V_{CCO_DDR}$ + 0.20<br>$V_{CCO_MIO}$ + 0.20 | V |
| **PL** | | | | | |
| $V_{CCINT}$(5) | PL internal supply voltage | 0.95 | 1.00 | 1.05 | V |
| | PL -1LI (0.95V) internal supply voltage | 0.92 | 0.95 | 0.98 | V |
| $V_{CCAUX}$ | PL auxiliary supply voltage | 1.71 | 1.80 | 1.89 | V |
| $V_{CCBRAM}$(5) | PL block RAM supply voltage | 0.95 | 1.00 | 1.05 | V |
| | PL -1LI (0.95V) block RAM supply voltage | 0.92 | 0.95 | 0.98 | V |
| $V_{CCO}$(6)(7) | PL supply voltage for HR I/O banks | 1.14 | – | 3.465 | V |
| $V_{IN}$(4) | I/O input voltage | –0.20 | – | $V_{CCO}$ + 0.20 | V |
| | I/O input voltage (when $V_{CCO}$ = 3.3V) for $V_{REF}$ and differential I/O standards except TMDS_33(8) | –0.20 | – | 2.625 | V |
| $I_{IN}$(9) | Maximum current through any (PS or PL) pin in a powered or unpowered bank when forward biasing the clamp diode | – | – | 10 | mA |
| $V_{CCBATT}$(10) | Battery voltage | 1.0 | – | 1.89 | V |
| **GTP Transceiver (XC7Z015 Only)** | | | | | |
| $V_{MGTAVCC}$(11) | Analog supply voltage for the GTP transmitter and receiver circuits | 0.97 | 1.0 | 1.03 | V |
| $V_{MGTAVTT}$(11) | Analog supply voltage for the GTP transmitter and receiver termination circuits | 1.17 | 1.2 | 1.23 | V |
| **XADC** | | | | | |
| $V_{CCADC}$ | XADC supply relative to GNDADC | 1.71 | 1.80 | 1.89 | V |
| $V_{REFP}$ | Externally supplied reference voltage | 1.20 | 1.25 | 1.30 | V |
| **Temperature** | | | | | |
| $T_j$ | Junction temperature operating range for commercial (C) temperature devices | 0 | – | 85 | °C |
| | Junction temperature operating range for extended (E) temperature devices | 0 | – | 100 | °C |
| | Junction temperature operating range for industrial (I) temperature devices | –40 | – | 100 | °C |
| | Junction temperature operating range for expanded (Q) temperature devices | –40 | – | 125 | °C |

**Notes:**

1. All voltages are relative to ground. The PL and PS share a common ground.
2. For the design of the power distribution system consult the *Zynq-7000 SoC PCB Design Guide* (UG933).
3. Applies to both MIO supply banks $V_{CCO_MIO0}$ and $V_{CCO_MIO1}$.
4. The lower absolute voltage specification always applies.
5. $V_{CCINT}$ and $V_{CCBRAM}$ should be connected to the same supply.
6. Configuration data is retained even if $V_{CCO}$ drops to 0V.
7. Includes $V_{CCO}$ of 1.2V, 1.35V, 1.5V, 1.8V, 2.5V, and 3.3V at ±5%.
8. See Table 11 for TMDS_33 specifications.
9. A total of 200 mA per PS or PL bank should not be exceeded.
10. $V_{CCBATT}$ is required only when using bitstream encryption. If battery is not used, connect $V_{CCBATT}$ to either ground or $V_{CCAUX}$.
11. Each voltage listed requires the filter circuit described in the *7 Series FPGAs GTP Transceiver User Guide* (UG482).

*Table 3:* **DC Characteristics Over Recommended Operating Conditions**

| Symbol | Description | Min | Typ[1] | Max | Units |
|---|---|---|---|---|---|
| $V_{DRINT}$ | Data retention $V_{CCINT}$ voltage (below which configuration data might be lost) | 0.75 | – | – | V |
| $V_{DRI}$ | Data retention $V_{CCAUX}$ voltage (below which configuration data might be lost) | 1.5 | – | – | V |
| $I_{REF}$ | PS_DDR_VREF 0/1, PS_MIO_VREF, and $V_{REF}$ leakage current per pin | – | – | 15 | µA |
| $I_L$ | Input or output leakage current per pin (sample-tested) | – | – | 15 | µA |
| $C_{IN}$[2] | PL die input capacitance at the pad | – | – | 8 | pF |
| $C_{PIN}$[2] | PS die input capacitance at the pad | – | – | 8 | pF |
| $I_{RPU}$ | Pad pull-up (when selected) @ $V_{IN}$ = 0V, $V_{CCO}$ = 3.3V | 90 | – | 330 | µA |
| | Pad pull-up (when selected) @ $V_{IN}$ = 0V, $V_{CCO}$ = 2.5V | 68 | – | 250 | µA |
| | Pad pull-up (when selected) @ $V_{IN}$ = 0V, $V_{CCO}$ = 1.8V | 34 | – | 220 | µA |
| | Pad pull-up (when selected) @ $V_{IN}$ = 0V, $V_{CCO}$ = 1.5V | 23 | – | 150 | µA |
| | Pad pull-up (when selected) @ $V_{IN}$ = 0V, $V_{CCO}$ = 1.2V | 12 | – | 120 | µA |
| $I_{RPD}$ | Pad pull-down (when selected) @ $V_{IN}$ = 3.3V | 68 | – | 330 | µA |
| | Pad pull-down (when selected) @ $V_{IN}$ = 1.8V | 45 | – | 180 | µA |
| $I_{CCADC}$ | Analog supply current, analog circuits in powered up state | – | – | 25 | mA |
| $I_{BATT}$[3] | Battery supply current | – | – | 150 | nA |
| $R_{IN_TERM}$[4] | Thevenin equivalent resistance of programmable input termination to $V_{CCO}$/2 (UNTUNED_SPLIT_40) | 28 | 40 | 55 | Ω |
| | Thevenin equivalent resistance of programmable input termination to $V_{CCO}$/2 (UNTUNED_SPLIT_50) | 35 | 50 | 65 | Ω |
| | Thevenin equivalent resistance of programmable input termination to $V_{CCO}$/2 (UNTUNED_SPLIT_60) | 44 | 60 | 83 | Ω |
| n | Temperature diode ideality factor | – | 1.010 | – | – |
| r | Temperature diode series resistance | – | 2 | – | Ω |

**Notes:**

1. Typical values are specified at nominal voltage, 25°C.
2. This measurement represents the die capacitance at the pad, not including the package.
3. Maximum value specified for worst case process at 25°C.
4. Termination resistance to a $V_{CCO}$/2 level.

*Table 4:* **$V_{IN}$ Maximum Allowed AC Voltage Overshoot and Undershoot for PS I/O and PL HR I/O Banks(1)(2)**

| AC Voltage Overshoot | % of UI @–40°C to 125°C | AC Voltage Undershoot | % of UI @–40°C to 125°C |
|---|---|---|---|
| $V_{CCO}$ + 0.55 | 100 | –0.40 | 100 |
| | | –0.45 | 61.7 |
| | | –0.50 | 25.8 |
| | | –0.55 | 11.0 |
| $V_{CCO}$ + 0.60 | 46.6 | –0.60 | 4.77 |
| $V_{CCO}$ + 0.65 | 21.2 | –0.65 | 2.10 |
| $V_{CCO}$ + 0.70 | 9.75 | –0.70 | 0.94 |
| $V_{CCO}$ + 0.75 | 4.55 | –0.75 | 0.43 |
| $V_{CCO}$ + 0.80 | 2.15 | –0.80 | 0.20 |
| $V_{CCO}$ + 0.85 | 1.02 | –0.85 | 0.09 |
| $V_{CCO}$ + 0.90 | 0.49 | –0.90 | 0.04 |
| $V_{CCO}$ + 0.95 | 0.24 | –0.95 | 0.02 |

**Notes:**

1. A total of 200 mA per bank should not be exceeded.
2. The peak voltage of the overshoot or undershoot, and the duration above $V_{CCO}$+ 0.20V or below GND –0.20V, must not exceed the values in this table.

*Table 5:* **Typical Quiescent Supply Current**

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | -3 | -2 | -1 | -1LI | |
| $I_{CCPINTQ}$ | PS quiescent $V_{CCPINT}$ supply current | XC7Z007S | N/A | 122 | 122 | N/A | mA |
| | | XC7Z012S | N/A | 122 | 122 | N/A | mA |
| | | XC7Z014S | N/A | 122 | 122 | N/A | mA |
| | | XC7Z010 | 122 | 122 | 122 | 85 | mA |
| | | XC7Z015 | 122 | 122 | 122 | 85 | mA |
| | | XC7Z020 | 122 | 122 | 122 | 85 | mA |
| | | XA7Z010 | N/A | N/A | 122 | N/A | mA |
| | | XA7Z020 | N/A | N/A | 122 | N/A | mA |
| | | XQ7Z020 | N/A | 122 | 122 | 85 | mA |
| $I_{CCPAUXQ}$ | PS quiescent $V_{CCPAUX}$ supply current | XC7Z007S | N/A | 13 | 13 | N/A | mA |
| | | XC7Z012S | N/A | 13 | 13 | N/A | mA |
| | | XC7Z014S | N/A | 13 | 13 | N/A | mA |
| | | XC7Z010 | 13 | 13 | 13 | 11 | mA |
| | | XC7Z015 | 13 | 13 | 13 | 11 | mA |
| | | XC7Z020 | 13 | 13 | 13 | 11 | mA |
| | | XA7Z010 | N/A | N/A | 13 | N/A | mA |
| | | XA7Z020 | N/A | N/A | 13 | N/A | mA |
| | | XQ7Z020 | N/A | 13 | 13 | 11 | mA |

*Table 5:* **Typical Quiescent Supply Current *(Cont'd)***

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | -3 | -2 | -1 | -1LI | |
| $I_{CCDDRQ}$ | PS quiescent $V_{CCO_DDR}$ supply current | XC7Z007S | N/A | 4 | 4 | N/A | mA |
| | | XC7Z012S | N/A | 4 | 4 | N/A | mA |
| | | XC7Z014S | N/A | 4 | 4 | N/A | mA |
| | | XC7Z010 | 4 | 4 | 4 | 4 | mA |
| | | XC7Z015 | 4 | 4 | 4 | 4 | mA |
| | | XC7Z020 | 4 | 4 | 4 | 4 | mA |
| | | XA7Z010 | N/A | N/A | 4 | N/A | mA |
| | | XA7Z020 | N/A | N/A | 4 | N/A | mA |
| | | XQ7Z020 | N/A | 4 | 4 | 4 | mA |
| $I_{CCINTQ}$ | PL quiescent $V_{CCINT}$ supply current | XC7Z007S | N/A | 34 | 34 | N/A | mA |
| | | XC7Z012S | N/A | 77 | 77 | N/A | mA |
| | | XC7Z014S | N/A | 78 | 78 | N/A | mA |
| | | XC7Z010 | 34 | 34 | 34 | 21/23(4) | mA |
| | | XC7Z015 | 77 | 77 | 77 | 47/53(4) | mA |
| | | XC7Z020 | 78 | 78 | 78 | 48/54(4) | mA |
| | | XA7Z010 | N/A | N/A | 34 | N/A | mA |
| | | XA7Z020 | N/A | N/A | 78 | N/A | mA |
| | | XQ7Z020 | N/A | 78 | 78 | 48/54(4) | mA |
| $I_{CCAUXQ}$ | PL quiescent $V_{CCAUX}$ supply current | XC7Z007S | N/A | 18 | 18 | N/A | mA |
| | | XC7Z012S | N/A | 35 | 35 | N/A | mA |
| | | XC7Z014S | N/A | 38 | 38 | N/A | mA |
| | | XC7Z010 | 18 | 18 | 18 | 16 | mA |
| | | XC7Z015 | 35 | 35 | 35 | 31 | mA |
| | | XC7Z020 | 38 | 38 | 38 | 34 | mA |
| | | XA7Z010 | N/A | N/A | 18 | N/A | mA |
| | | XA7Z020 | N/A | N/A | 38 | N/A | mA |
| | | XQ7Z020 | N/A | 38 | 38 | 34 | mA |
| $I_{CCOQ}$ | PL quiescent $V_{CCO}$ supply current | XC7Z007S | N/A | 3 | 3 | N/A | mA |
| | | XC7Z012S | N/A | 3 | 3 | N/A | mA |
| | | XC7Z014S | N/A | 3 | 3 | N/A | mA |
| | | XC7Z010 | 3 | 3 | 3 | 3 | mA |
| | | XC7Z015 | 3 | 3 | 3 | 3 | mA |
| | | XC7Z020 | 3 | 3 | 3 | 3 | mA |
| | | XA7Z010 | N/A | N/A | 3 | N/A | mA |
| | | XA7Z020 | N/A | N/A | 3 | N/A | mA |
| | | XQ7Z020 | N/A | 3 | 3 | 3 | mA |

*Table 5:* **Typical Quiescent Supply Current *(Cont'd)***

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | -3 | -2 | -1 | -1LI | |
| $I_{CCBRAMQ}$ | PL quiescent $V_{CCBRAM}$ supply current | XC7Z007S | N/A | 3 | 3 | N/A | mA |
| | | XC7Z012S | N/A | 4 | 4 | N/A | mA |
| | | XC7Z014S | N/A | 6 | 6 | N/A | mA |
| | | XC7Z010 | 3 | 3 | 3 | 1/2(4) | mA |
| | | XC7Z015 | 4 | 4 | 4 | 2/2(4) | mA |
| | | XC7Z020 | 6 | 6 | 6 | 3/4(4) | mA |
| | | XA7Z010 | N/A | N/A | 3 | N/A | mA |
| | | XA7Z020 | N/A | N/A | 6 | N/A | mA |
| | | XQ7Z020 | N/A | 6 | 6 | 3/4(4) | mA |

**Notes:**

1. Typical values are specified at nominal voltage, 85°C junction temperatures ($T_j$) with single-ended SelectIO™ resources.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. The Xilinx Power Estimator (XPE) spreadsheet tool (download at http://www.xilinx.com/power) estimates operating current. When the required power-on current exceeds the estimated operating current, XPE can display the power-on current.
4. The first value is at 0.95V, and the second value is at 1.0V.

## PS Power-On/Off Power Supply Sequencing

The recommended power-on sequence is $V_{CCPINT}$, then $V_{CCPAUX}$ and $V_{CCPLL}$ together, then the PS $V_{CCO}$ supplies ($V_{CCO_MIO0}$, $V_{CCO_MIO1}$, and $V_{CCO_DDR}$) to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The PS_POR_B input is required to be asserted to GND during the power-on sequence until $V_{CCPINT}$, $V_{CCPAUX}$ and $V_{CCO_MIO0}$ have reached minimum operating levels to ensure PS eFUSE integrity. For additional information about PS_POR_B timing requirements refer to Resets.

The recommended power-off sequence is the reverse of the power-on sequence. If $V_{CCPAUX}$, $V_{CCPLL}$, and the PS $V_{CCO}$ supplies ($V_{CCO_MIO0}$, $V_{CCO_MIO1}$, and $V_{CCO_DDR}$) have the same recommended voltage levels, then they can be powered by the same supply and ramped simultaneously. Xilinx recommends powering $V_{CCPLL}$ with the same supply as $V_{CCPAUX}$, with an optional ferrite bead filter. Before $V_{CCPINT}$ reaches 0.80V at least one of the four following conditions is required during the power-off stage: the PS_POR_B input is asserted to GND, the reference clock to the PS_CLK input is disabled, $V_{CCPAUX}$ is lower than 0.70V, or $V_{CCO_MIO0}$ is lower than 0.90V. The condition must be held until $V_{CCPINT}$ reaches 0.40V to ensure PS eFUSE integrity.

For $V_{CCO_MIO0}$ and $V_{CCO_MIO1}$ voltages of 3.3V:

- The voltage difference between $V_{CCO_MIO0}$ /$V_{CCO_MIO1}$ and $V_{CCPAUX}$ must not exceed 2.625V for longer than $T_{VCCO2VCCAUX}$ for each power-on/off cycle to maintain device reliability levels.
- The $T_{VCCO2VCCAUX}$ time can be allocated in any percentage between the power-on and power-off ramps.

## PL Power-On/Off Power Supply Sequencing

The recommended power-on sequence for the PL is $V_{CCINT}$, $V_{CCBRAM}$, $V_{CCAUX}$, and $V_{CCO}$ to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If $V_{CCINT}$ and $V_{CCBRAM}$ have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously. If $V_{CCAUX}$ and $V_{CCO}$ have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously.

For $V_{CCO}$ voltages of 3.3V in HR I/O banks and configuration bank 0:

- The voltage difference between $V_{CCO}$ and $V_{CCAUX}$ must not exceed 2.625V for longer than $T_{VCCO2VCCAUX}$ for each power-on/off cycle to maintain device reliability levels.
- The $T_{VCCO2VCCAUX}$ time can be allocated in any percentage between the power-on and power-off ramps.

#### *GTP Transceivers (XC7Z015 Only)*

The recommended power-on sequence to achieve minimum current draw for the GTP transceivers (XC7Z015 only) is $V_{CCINT}$, $V_{MGTAVCC}$, $V_{MGTAVTT}$ OR $V_{MGTAVCC}$, $V_{CCINT}$, $V_{MGTAVTT}$. Both $V_{MGTAVCC}$ and $V_{CCINT}$ can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw.

If these recommended sequences are not met, current drawn from $V_{MGTAVTT}$ can be higher than specifications during power-up and power-down.

- When $V_{MGTAVTT}$ is powered before $V_{MGTAVCC}$ and $V_{MGTAVTT} - V_{MGTAVCC} > 150$ mV and $V_{MGTAVCC} < 0.7$V, the $V_{MGTAVTT}$ current draw can increase by 460 mA per transceiver during $V_{MGTAVCC}$ ramp up. The duration of the current draw can be up to 0.3 x $T_{MGTAVCC}$ (ramp time from GND to 90% of $V_{MGTAVCC}$). The reverse is true for power-down.
- When $V_{MGTAVTT}$ is powered before $V_{CCINT}$ and $V_{MGTAVTT} - V_{CCINT} > 150$ mV and $V_{CCINT} < 0.7$V, the $V_{MGTAVTT}$ current draw can increase by 50 mA per transceiver during $V_{CCINT}$ ramp up. The duration of the current draw can be up to 0.3 x $T_{VCCINT}$ (ramp time from GND to 90% of $V_{CCINT}$). The reverse is true for power-down.

There is no recommended sequence for supplies not shown.

## PS—PL Power Sequencing

The PS and PL power supplies are fully independent. PS power supplies ($V_{CCPINT}$, $V_{CCPAUX}$, $V_{CCPLL}$, $V_{CCO_DDR}$, $V_{CCO_MIO0}$, and $V_{CCO_MIO1}$) can be powered before or after any PL power supplies. The PS and PL power regions are isolated to prevent damage.

## Power Supply Requirements

Table 6 shows the minimum current, in addition to $I_{CCQ}$, that is required by Zynq-7000 devices for proper power-on and configuration. If the current minimums shown in Table 5 and Table 6 are met, the device powers on after all four PL supplies have passed through their power-on reset threshold voltages. The Zynq-7000 device must not be configured until after $V_{CCINT}$ is applied. Once initialized and configured, use the Xilinx Power Estimator (XPE) spreadsheet tool (download at www.xilinx.com/power) to estimate current drain on these supplies.

*Table 6:* **Power-On Current for Zynq-7000 Devices**

| Device | $I_{CCPINTMIN}$ | $I_{CCPAUXMIN}$ | $I_{CCDDRMIN}$ | $I_{CCINTMIN}$ | $I_{CCAUXMIN}$ | $I_{CCOMIN}$ | $I_{CCBRAMMIN}$ | Units |
|---|---|---|---|---|---|---|---|---|
| XC7Z007S | $I_{CCPINTQ}$ +70 | $I_{CCPAUXQ}$ +40 | $I_{CCDDRQ}$ + 100 mA per bank | $I_{CCINTQ}$ +40 | $I_{CCAUXQ}$ +60 | $I_{CCOQ}$ + 90 mA per bank | $I_{CCBRAMQ}$ +40 | mA |
| XC7Z012S | $I_{CCPINTQ}$ +70 | $I_{CCPAUXQ}$ +40 | $I_{CCDDRQ}$ + 100 mA per bank | $I_{CCINTQ}$ +130 | $I_{CCAUXQ}$ +60 | $I_{CCOQ}$ + 90 mA per bank | $I_{CCBRAMQ}$ +40 | mA |
| XC7Z014S | $I_{CCPINTQ}$ +70 | $I_{CCPAUXQ}$ +40 | $I_{CCDDRQ}$ + 100 mA per bank | $I_{CCINTQ}$ +70 | $I_{CCAUXQ}$ +60 | $I_{CCOQ}$ + 90 mA per bank | $I_{CCBRAMQ}$ +40 | mA |
| XC7Z010<br>XA7Z010 | $I_{CCPINTQ}$ +70 | $I_{CCPAUXQ}$ +40 | $I_{CCDDRQ}$ + 100 mA per bank | $I_{CCINTQ}$ +40 | $I_{CCAUXQ}$ +60 | $I_{CCOQ}$ + 90 mA per bank | $I_{CCBRAMQ}$ +40 | mA |
| XC7Z015 | $I_{CCPINTQ}$ +70 | $I_{CCPAUXQ}$ +40 | $I_{CCDDRQ}$ + 100 mA per bank | $I_{CCINTQ}$ +130 | $I_{CCAUXQ}$ +60 | $I_{CCOQ}$ + 90 mA per bank | $I_{CCBRAMQ}$ +40 | mA |
| XC7Z020<br>XA7Z020<br>XQ7Z020 | $I_{CCPINTQ}$ +70 | $I_{CCPAUXQ}$ +40 | $I_{CCDDRQ}$ + 100 mA per bank | $I_{CCINTQ}$ +70 | $I_{CCAUXQ}$ +60 | $I_{CCOQ}$ + 90 mA per bank | $I_{CCBRAMQ}$ +40 | mA |

*Table 7:* **Power Supply Ramp Time**

| Symbol | Description | Conditions | Min | Max | Units |
|---|---|---|---|---|---|
| $T_{VCCPINT}$ | Ramp time from GND to 90% of $V_{CCPINT}$ | | 0.2 | 50 | ms |
| $T_{VCCPAUX}$ | Ramp time from GND to 90% of $V_{CCPAUX}$ | | 0.2 | 50 | ms |
| $T_{VCCO_DDR}$ | Ramp time from GND to 90% of $V_{CCO_DDR}$ | | 0.2 | 50 | ms |
| $T_{VCCO_MIO}$ | Ramp time from GND to 90% of $V_{CCO_MIO}$ | | 0.2 | 50 | ms |
| $T_{VCCINT}$ | Ramp time from GND to 90% of $V_{CCINT}$ | | 0.2 | 50 | ms |
| $T_{VCCO}$ | Ramp time from GND to 90% of $V_{CCO}$ | | 0.2 | 50 | ms |
| $T_{VCCAUX}$ | Ramp time from GND to 90% of $V_{CCAUX}$ | | 0.2 | 50 | ms |
| $T_{VCCBRAM}$ | Ramp time from GND to 90% of $V_{CCBRAM}$ | | 0.2 | 50 | ms |
| $T_{VCCO2VCCAUX}$ | Allowed time per power cycle for $V_{CCO} - V_{CCAUX} > 2.625V$ and $V_{CCO_MIO} - V_{CCPAUX} > 2.625V$ | $T_j = 125°C$(1) | – | 300 | ms |
| | | $T_j = 100°C$(1) | – | 500 | |
| | | $T_j = 85°C$(1) | – | 800 | |
| $T_{MGTAVCC}$ | Ramp time from GND to 90% of $V_{MGTAVCC}$ | | 0.2 | 50 | ms |
| $T_{MGTAVTT}$ | Ramp time from GND to 90% of $V_{MGTAVTT}$ | | 0.2 | 50 | ms |

**Notes:**

1. Based on 240,000 power cycles with nominal $V_{CCO}$ of 3.3V or 36,500 power cycles with worst case $V_{CCO}$ of 3.465V.

## DC Input and Output Levels

Values for $V_{IL}$ and $V_{IH}$ are recommended input voltages. Values for $I_{OL}$ and $I_{OH}$ are guaranteed over the recommended operating conditions at the $V_{OL}$ and $V_{OH}$ test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum $V_{CCO}$ with the respective $V_{OL}$ and $V_{OH}$ voltage levels shown. Other standards are sample tested.

### PS I/O Levels

*Table 8:* **PS DC Input and Output Levels(1)**

| Bank | I/O Standard | $V_{IL}$ | | $V_{IH}$ | | $V_{OL}$ | $V_{OH}$ | $I_{OL}$ | $I_{OH}$ |
|---|---|---|---|---|---|---|---|---|---|
| | | V, Min | V, Max | V, Min | V, Max | V, Max | V, Min | mA | mA |
| MIO | LVCMOS18 | –0.300 | 35% $V_{CCO_MIO}$ | 65% $V_{CCO_MIO}$ | $V_{CCO_MIO}$ + 0.300 | 0.450 | $V_{CCO_MIO}$ – 0.450 | 8 | –8 |
| MIO | LVCMOS25 | –0.300 | 0.700 | 1.700 | $V_{CCO_MIO}$ + 0.300 | 0.400 | $V_{CCO_MIO}$ – 0.400 | 8 | –8 |
| MIO | LVCMOS33 | –0.300 | 0.800 | 2.000 | 3.450 | 0.400 | $V_{CCO_MIO}$ – 0.400 | 8 | –8 |
| MIO | HSTL_I_18 | –0.300 | $V_{PREF}$ – 0.100 | $V_{PREF}$ + 0.100 | $V_{CCO_MIO}$ + 0.300 | 0.400 | $V_{CCO_MIO}$ – 0.400 | 8 | –8 |
| DDR | SSTL18_I | –0.300 | $V_{PREF}$ – 0.125 | $V_{PREF}$ + 0.125 | $V_{CCO_DDR}$ + 0.300 | $V_{CCO_DDR}$/2 – 0.470 | $V_{CCO_DDR}$/2 + 0.470 | 8 | –8 |
| DDR | SSTL15 | –0.300 | $V_{PREF}$ – 0.100 | $V_{PREF}$ + 0.100 | $V_{CCO_DDR}$ + 0.300 | $V_{CCO_DDR}$/2 – 0.175 | $V_{CCO_DDR}$/2 + 0.175 | 13.0 | –13.0 |
| DDR | SSTL135 | –0.300 | $V_{PREF}$ – 0.090 | $V_{PREF}$ + 0.090 | $V_{CCO_DDR}$ + 0.300 | $V_{CCO_DDR}$/2 – 0.150 | $V_{CCO_DDR}$/2 + 0.150 | 13.0 | –13.0 |
| DDR | HSUL_12 | –0.300 | $V_{PREF}$ – 0.130 | $V_{PREF}$ + 0.130 | $V_{CCO_DDR}$ + 0.300 | 20% $V_{CCO_DDR}$ | 80% $V_{CCO_DDR}$ | 0.1 | –0.1 |

**Notes:**

1. Tested according to relevant specifications.

*Table 9:* **PS Complementary Differential DC Input and Output Levels**

| Bank | I/O Standard | $V_{ICM}$(1) | | | $V_{ID}$(2) | | $V_{OL}$(3) | $V_{OH}$(4) | $I_{OL}$ | $I_{OH}$ |
|---|---|---|---|---|---|---|---|---|---|---|
| | | V, Min | V,Typ | V, Max | V,Min | V, Max | V, Max | V, Min | mA, Max | mA, Min |
| DDR | DIFF_HSUL_12 | 0.300 | 0.600 | 0.850 | 0.100 | – | 20% $V_{CCO}$ | 80% $V_{CCO}$ | 0.100 | –0.100 |
| DDR | DIFF_SSTL135 | 0.300 | 0.675 | 1.000 | 0.100 | – | ($V_{CCO_DDR}$/2) – 0.150 | ($V_{CCO_DDR}$/2) + 0.150 | 13.0 | –13.0 |
| DDR | DIFF_SSTL15 | 0.300 | 0.750 | 1.125 | 0.100 | – | ($V_{CCO_DDR}$/2) – 0.175 | ($V_{CCO_DDR}$/2) + 0.175 | 13.0 | –13.0 |
| DDR | DIFF_SSTL18_I | 0.300 | 0.900 | 1.425 | 0.100 | – | ($V_{CCO_DDR}$/2) – 0.470 | ($V_{CCO_DDR}$/2) + 0.470 | 8.00 | –8.00 |

**Notes:**

1. $V_{ICM}$ is the input common mode voltage.
2. $V_{ID}$ is the input differential voltage (Q–$\overline{Q}$).
3. $V_{OL}$ is the single-ended low-output voltage.
4. $V_{OH}$ is the single-ended high-output voltage.

## PL I/O Levels

*Table 10:* **SelectIO DC Input and Output Levels**[1][2]

| I/O Standard | $V_{IL}$ | | $V_{IH}$ | | $V_{OL}$ | $V_{OH}$ | $I_{OL}$ | $I_{OH}$ |
|---|---|---|---|---|---|---|---|---|
| | V, Min | V, Max | V, Min | V, Max | V, Max | V, Min | mA | mA |
| HSTL_I | –0.300 | $V_{REF}$ – 0.100 | $V_{REF}$ + 0.100 | $V_{CCO}$ + 0.300 | 0.400 | $V_{CCO}$ – 0.400 | 8.00 | –8.00 |
| HSTL_I_18 | –0.300 | $V_{REF}$ – 0.100 | $V_{REF}$ + 0.100 | $V_{CCO}$ + 0.300 | 0.400 | $V_{CCO}$ – 0.400 | 8.00 | –8.00 |
| HSTL_II | –0.300 | $V_{REF}$ – 0.100 | $V_{REF}$ + 0.100 | $V_{CCO}$ + 0.300 | 0.400 | $V_{CCO}$ – 0.400 | 16.00 | –16.00 |
| HSTL_II_18 | –0.300 | $V_{REF}$ – 0.100 | $V_{REF}$ + 0.100 | $V_{CCO}$ + 0.300 | 0.400 | $V_{CCO}$ – 0.400 | 16.00 | –16.00 |
| HSUL_12 | –0.300 | $V_{REF}$ – 0.130 | $V_{REF}$ + 0.130 | $V_{CCO}$ + 0.300 | 20% $V_{CCO}$ | 80% $V_{CCO}$ | 0.10 | –0.10 |
| LVCMOS12 | –0.300 | 35% $V_{CCO}$ | 65% $V_{CCO}$ | $V_{CCO}$ + 0.300 | 0.400 | $V_{CCO}$ – 0.400 | Note 3 | Note 3 |
| LVCMOS15 | –0.300 | 35% $V_{CCO}$ | 65% $V_{CCO}$ | $V_{CCO}$ + 0.300 | 25% $V_{CCO}$ | 75% $V_{CCO}$ | Note 4 | Note 4 |
| LVCMOS18 | –0.300 | 35% $V_{CCO}$ | 65% $V_{CCO}$ | $V_{CCO}$ + 0.300 | 0.450 | $V_{CCO}$ – 0.450 | Note 5 | Note 5 |
| LVCMOS25 | –0.300 | 0.7 | 1.700 | $V_{CCO}$ + 0.300 | 0.400 | $V_{CCO}$ – 0.400 | Note 4 | Note 4 |
| LVCMOS33 | –0.300 | 0.8 | 2.000 | 3.450 | 0.400 | $V_{CCO}$ – 0.400 | Note 4 | Note 4 |
| LVTTL | –0.300 | 0.8 | 2.000 | 3.450 | 0.400 | 2.400 | Note 5 | Note 5 |
| MOBILE_DDR | –0.300 | 20% $V_{CCO}$ | 80% $V_{CCO}$ | $V_{CCO}$ + 0.300 | 10% $V_{CCO}$ | 90% $V_{CCO}$ | 0.10 | –0.10 |
| PCI33_3 | –0.400 | 30% $V_{CCO}$ | 50% $V_{CCO}$ | $V_{CCO}$ + 0.500 | 10% $V_{CCO}$ | 90% $V_{CCO}$ | 1.50 | –0.50 |
| SSTL135 | –0.300 | $V_{REF}$ – 0.090 | $V_{REF}$ + 0.090 | $V_{CCO}$ + 0.300 | $V_{CCO}$/2 – 0.150 | $V_{CCO}$/2 + 0.150 | 13.00 | –13.00 |
| SSTL135_R | –0.300 | $V_{REF}$ – 0.090 | $V_{REF}$ + 0.090 | $V_{CCO}$ + 0.300 | $V_{CCO}$/2 – 0.150 | $V_{CCO}$/2 + 0.150 | 8.90 | –8.90 |
| SSTL15 | –0.300 | $V_{REF}$ – 0.100 | $V_{REF}$ + 0.100 | $V_{CCO}$ + 0.300 | $V_{CCO}$/2 – 0.175 | $V_{CCO}$/2 + 0.175 | 13.00 | –13.00 |
| SSTL15_R | –0.300 | $V_{REF}$ – 0.100 | $V_{REF}$ + 0.100 | $V_{CCO}$ + 0.300 | $V_{CCO}$/2 – 0.175 | $V_{CCO}$/2 + 0.175 | 8.90 | –8.90 |
| SSTL18_I | –0.300 | $V_{REF}$ – 0.125 | $V_{REF}$ + 0.125 | $V_{CCO}$ + 0.300 | $V_{CCO}$/2 – 0.470 | $V_{CCO}$/2 + 0.470 | 8.00 | –8.00 |
| SSTL18_II | –0.300 | $V_{REF}$ – 0.125 | $V_{REF}$ + 0.125 | $V_{CCO}$ + 0.300 | $V_{CCO}$/2 – 0.600 | $V_{CCO}$/2 + 0.600 | 13.40 | –13.40 |

**Notes:**

1. Tested according to relevant specifications.
2. 3.3V and 2.5V standards are only supported in HR I/O banks.
3. Supported drive strengths of 4, 8, or 12 mA in HR I/O banks.
4. Supported drive strengths of 4, 8, 12, or 16 mA in HR I/O banks.
5. Supported drive strengths of 4, 8, 12, 16, or 24 mA in HR I/O banks.
6. For detailed interface specific DC voltage levels, see the *7 Series FPGAs SelectIO Resources User Guide* (UG471).

*Table 11:* **Differential SelectIO DC Input and Output Levels**

| I/O Standard | $V_{ICM}$[1] | | | $V_{ID}$[2] | | | $V_{OCM}$[3] | | | $V_{OD}$[4] | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | V, Min | V, Typ | V, Max | V, Min | V, Typ | V, Max | V, Min | V, Typ | V, Max | V, Min | V, Typ | V, Max |
| BLVDS_25 | 0.300 | 1.200 | 1.425 | 0.100 | – | – | – | 1.250 | – | Note 5 | | |
| MINI_LVDS_25 | 0.300 | 1.200 | $V_{CCAUX}$ | 0.200 | 0.400 | 0.600 | 1.000 | 1.200 | 1.400 | 0.300 | 0.450 | 0.600 |
| PPDS_25 | 0.200 | 0.900 | $V_{CCAUX}$ | 0.100 | 0.250 | 0.400 | 0.500 | 0.950 | 1.400 | 0.100 | 0.250 | 0.400 |
| RSDS_25 | 0.300 | 0.900 | 1.500 | 0.100 | 0.350 | 0.600 | 1.000 | 1.200 | 1.400 | 0.100 | 0.350 | 0.600 |
| TMDS_33 | 2.700 | 2.965 | 3.230 | 0.150 | 0.675 | 1.200 | $V_{CCO}$–0.405 | $V_{CCO}$–0.300 | $V_{CCO}$–0.190 | 0.400 | 0.600 | 0.800 |

**Notes:**

1. $V_{ICM}$ is the input common mode voltage.
2. $V_{ID}$ is the input differential voltage (Q–$\overline{Q}$).
3. $V_{OCM}$ is the output common mode voltage.
4. $V_{OD}$ is the output differential voltage (Q–$\overline{Q}$).
5. $V_{OD}$ for BLVDS will vary significantly depending on topology and loading.
6. LVDS_25 is specified in Table 13.

*Table 12:* **Complementary Differential SelectIO DC Input and Output Levels**

| I/O Standard | $V_{ICM}$[1] | | | $V_{ID}$[2] | | $V_{OL}$[3] | $V_{OH}$[4] | $I_{OL}$ | $I_{OH}$ |
|---|---|---|---|---|---|---|---|---|---|
| | V, Min | V,Typ | V, Max | V,Min | V, Max | V, Max | V, Min | mA, Max | mA, Min |
| DIFF_HSTL_I | 0.300 | 0.750 | 1.125 | 0.100 | – | 0.400 | $V_{CCO}$–0.400 | 8.00 | –8.00 |
| DIFF_HSTL_I_18 | 0.300 | 0.900 | 1.425 | 0.100 | – | 0.400 | $V_{CCO}$–0.400 | 8.00 | –8.00 |
| DIFF_HSTL_II | 0.300 | 0.750 | 1.125 | 0.100 | – | 0.400 | $V_{CCO}$–0.400 | 16.00 | –16.00 |
| DIFF_HSTL_II_18 | 0.300 | 0.900 | 1.425 | 0.100 | – | 0.400 | $V_{CCO}$–0.400 | 16.00 | –16.00 |
| DIFF_HSUL_12 | 0.300 | 0.600 | 0.850 | 0.100 | – | 20% $V_{CCO}$ | 80% $V_{CCO}$ | 0.100 | –0.100 |
| DIFF_MOBILE_DDR | 0.300 | 0.900 | 1.425 | 0.100 | – | 10% $V_{CCO}$ | 90% $V_{CCO}$ | 0.100 | –0.100 |
| DIFF_SSTL135 | 0.300 | 0.675 | 1.000 | 0.100 | – | ($V_{CCO}$/2) – 0.150 | ($V_{CCO}$/2) + 0.150 | 13.0 | –13.0 |
| DIFF_SSTL135_R | 0.300 | 0.675 | 1.000 | 0.100 | – | ($V_{CCO}$/2) – 0.150 | ($V_{CCO}$/2) + 0.150 | 8.9 | –8.9 |
| DIFF_SSTL15 | 0.300 | 0.750 | 1.125 | 0.100 | – | ($V_{CCO}$/2) – 0.175 | ($V_{CCO}$/2) + 0.175 | 13.0 | –13.0 |
| DIFF_SSTL15_R | 0.300 | 0.750 | 1.125 | 0.100 | – | ($V_{CCO}$/2) – 0.175 | ($V_{CCO}$/2) + 0.175 | 8.9 | –8.9 |
| DIFF_SSTL18_I | 0.300 | 0.900 | 1.425 | 0.100 | – | ($V_{CCO}$/2) – 0.470 | ($V_{CCO}$/2) + 0.470 | 8.00 | –8.00 |
| DIFF_SSTL18_II | 0.300 | 0.900 | 1.425 | 0.100 | – | ($V_{CCO}$/2) – 0.600 | ($V_{CCO}$/2) + 0.600 | 13.4 | –13.4 |

**Notes:**

1. $V_{ICM}$ is the input common mode voltage.
2. $V_{ID}$ is the input differential voltage (Q–$\overline{Q}$).
3. $V_{OL}$ is the single-ended low-output voltage.
4. $V_{OH}$ is the single-ended high-output voltage.

## LVDS DC Specifications (LVDS_25)

*Table 13:* **LVDS_25 DC Specifications**[1]

| Symbol | DC Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{CCO}$ | Supply voltage | | 2.375 | 2.5 | 2.625 | V |
| $V_{OH}$ | Output High voltage for Q and $\overline{Q}$ | $R_T$ = 100Ω across Q and $\overline{Q}$ signals | – | – | 1.675 | V |
| $V_{OL}$ | Output Low voltage for Q and $\overline{Q}$ | $R_T$ = 100Ω across Q and $\overline{Q}$ signals | 0.700 | – | – | V |
| $V_{ODIFF}$ | Differential output voltage:<br>(Q – $\overline{Q}$), Q = High<br>($\overline{Q}$ – Q), $\overline{Q}$ = High | $R_T$ = 100Ω across Q and $\overline{Q}$ signals | 247 | 350 | 600 | mV |
| $V_{OCM}$ | Output common-mode voltage | $R_T$ = 100Ω across Q and $\overline{Q}$ signals | 1.00 | 1.25 | 1.425 | V |
| $V_{IDIFF}$ | Differential input voltage:<br>(Q – $\overline{Q}$), Q = High<br>($\overline{Q}$ – Q), $\overline{Q}$ = High | | 100 | 350 | 600 | mV |
| $V_{ICM}$ | Input common-mode voltage | | 0.3 | 1.2 | 1.500 | V |

**Notes:**

1. Differential inputs for LVDS_25 can be placed in banks with $V_{CCO}$ levels that are different from the required level for outputs. Consult the *7 Series FPGAs SelectIO Resources User Guide* (UG471) for more information.

## AC Switching Characteristics

All values represented in this data sheet are based on the speed specifications in the ISE® Design Suite 14.7 and Vivado® Design Suite 2016.3 as outlined in Table 14.

*Table 14:* **Zynq-7000 SoC Speed Specification Version By Device**

| ISE 14.7 | Vivado 2016.3 | Device |
|---|---|---|
| 1.08 | 1.11 | XC7Z010 and XC7Z020 |
| N/A | 1.11 | XC7Z007S, XC7Z012S, XC7Z014S, and XC7Z015 |
| 1.06 | 1.09 | XA7Z010 and XA7Z020 |
| 1.06 | 1.10 | XQ7Z020 |

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

***Advance Product Specification***

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

***Preliminary Product Specification***

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

***Production Product Specification***

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

### Testing of AC Switching Characteristics

Internal timing parameters are derived from measuring internal test patterns. All AC switching characteristics are representative of worst-case supply voltage and junction temperature conditions.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Zynq-7000 devices.

### Speed Grade Designations

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. Table 15 correlates the current status of each Zynq-7000 device on a per speed grade basis.

*Table 15:* **Zynq-7000 Device Speed Grade Designations**

| Device | Speed Grade Designations | | |
|---|---|---|---|
| | Advance | Preliminary | Production |
| XC7Z007S | | | -2E, -2I, -1C, -1I |
| XC7Z012S | | | -2E, -2I, -1C, -1I |
| XC7Z014S | | | -2E, -2I, -1C, -1I |
| XC7Z010 | | | -3E, -2E, -2I, -1C, -1I, -1LI |
| XC7Z015 | | | -3E, -2E, -2I, -1C, -1I, -1LI |

*Table 15:* **Zynq-7000 Device Speed Grade Designations *(Cont'd)***

| Device | Speed Grade Designations | | |
|---|---|---|---|
| | Advance | Preliminary | Production |
| XC7Z020 | | | -3E, -2E, -2I, -1C, -1I, -1LI |
| XA7Z010 | | | -1I, -1Q |
| XA7Z020 | | | -1I, -1Q |
| XQ7Z020 | | | -2I, -1I, -1Q, -1LI |

## Production Silicon and Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases.

Table 16 lists the production released Zynq-7000 device, speed grade, and the minimum corresponding supported speed specification version and software revisions. The software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

*Table 16:* **Zynq-7000 Device Production Software and Speed Specification Release**

| Device | Speed Grade Designations | | | | | | |
|---|---|---|---|---|---|---|---|
| | -3E | -2E | -2I | -1C | -1I | -1LI | -1Q |
| XC7Z007S | N/A | Vivado tools 2016.3 v1.11 | | | | N/A | N/A |
| XC7Z012S | N/A | Vivado tools 2016.3 v1.11 | | | | N/A | N/A |
| XC7Z014S | N/A | Vivado tools 2016.3 v1.11 | | | | N/A | N/A |
| XC7Z010 | ISE tools 14.5 v1.06 and Vivado tools 2013.1 v1.06 | ISE tools 14.4 and the 14.4 device pack v1.05 and Vivado tools 2013.1 v1.06 | | | | Vivado tools 2014.4 v1.11 | N/A |
| XC7Z015 | Vivado tools 2013.4 v1.09 | | | | | Vivado tools 2014.4 v1.11 | N/A |
| XC7Z020 | ISE tools 14.5 v1.06 and Vivado tools 2013.1 v1.06 | ISE tools 14.4 and the 14.4 device pack v1.05 and Vivado tools 2013.1 v1.06 | | | | Vivado tools 2014.4 v1.11 | N/A |
| XA7Z010 | N/A | | | | ISE tools 14.5 v1.04 and Vivado tools 2013.1 v1.04 | N/A | ISE tools 14.6 v1.05 and Vivado tools 2013.2 v1.05 |
| XA7Z020 | N/A | | | | ISE tools 14.5 v1.04 and Vivado tools 2013.1 v1.04 | N/A | ISE tools 14.6 v1.05 and Vivado tools 2013.2 v1.05 |
| XQ7Z020 | N/A | | ISE tools 14.6 v1.05 and Vivado tools 2013.2 v1.05 | N/A | ISE tools 14.6 v1.05 and Vivado tools 2013.2 v1.05 | Vivado tools 2015.4 v1.10 | ISE tools 14.7 v1.06 and Vivado tools 2013.3 v1.06 |

### Selecting the Correct Speed Grade and Voltage in the Vivado Tools

It is important to select the correct device speed grade and voltage in the Vivado tools for the device that you are selecting.

To select the -3, -2, or -1 (PL 1.0V) speed specifications in the Vivado tools, select the **Zynq-7000**, **XA Zynq-7000**, or **Defense Grade Zynq-7000** sub-family, and then select the part name that is the device name followed by the package name followed by the speed grade. For example, select the **xc7z020clg484-3** part name for the XC7Z020 device in the CLG484 package and -3 speed grade.

To select the -1LI (PL 0.95V) speed specifications in the Vivado tools, select the **Zynq-7000** sub-family and then select the part name that is the device name followed by an *i* followed by the package name followed by the speed grade. For example, select the **xc7z020iclg484-1L** part name for the XC7Z020 device in the CLG484 package and -1LI (PL 0.95V) speed grade. The -1LI (PL 0.95V) speed specifications are not supported in the ISE tools.

A similar part naming convention applies to the speed specifications selection in the ISE tools for supported devices. See Table 16 for the subset of the Zynq-7000 devices supported in the ISE tools.

## PS Performance Characteristics

For further design requirement details, refer to the *Zynq-7000 SoC Technical Reference Manual* (UG585).

*Table 17:* **CPU Clock Domains Performance**

| Symbol | Clock Ratio | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | -3 | -2 | -1C/-1I/-1LI | -1Q | |
| $F_{CPU_6X4X_621_MAX}$(1) | 6:2:1 | Maximum CPU clock frequency | 866 | 766 | 667 | 667 | MHz |
| $F_{CPU_3X2X_621_MAX}$ | | Maximum CPU_3X clock frequency | 433 | 383 | 333 | 333 | MHz |
| $F_{CPU_2X_621_MAX}$ | | Maximum CPU_2X clock frequency | 288 | 255 | 222 | 222 | MHz |
| $F_{CPU_1X_621_MAX}$ | | Maximum CPU_1X clock frequency | 144 | 127 | 111 | 111 | MHz |
| $F_{CPU_6X4X_421_MAX}$(1) | 4:2:1 | Maximum CPU clock frequency | 710 | 600 | 533 | 533 | MHz |
| $F_{CPU_3X2X_421_MAX}$ | | Maximum CPU_3X clock frequency | 355 | 300 | 267 | 267 | MHz |
| $F_{CPU_2X_421_MAX}$ | | Maximum CPU_2X clock frequency | 355 | 300 | 267 | 267 | MHz |
| $F_{CPU_1X_421_MAX}$ | | Maximum CPU_1X clock frequency | 178 | 150 | 133 | 133 | MHz |

**Notes:**

1. The maximum frequency during BootROM execution is 500 MHz across all speed specifications.

*Table 18:* **PS DDR Clock Domains Performance**(1)

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1C/-1I/-1LI | -1Q | |
| $F_{DDR3_MAX}$ | Maximum DDR3 interface performance | 1066 | 1066 | 1066 | 1066 | Mb/s |
| $F_{DDR3L_MAX}$ | Maximum DDR3L interface performance | 1066 | 1066 | 1066 | 1066 | Mb/s |
| $F_{DDR2_MAX}$ | Maximum DDR2 interface performance | 800 | 800 | 800 | 800 | Mb/s |
| $F_{LPDDR2_MAX}$ | Maximum LPDDR2 interface performance | 800 | 800 | 800 | 800 | Mb/s |
| $F_{DDRCLK_2XMAX}$ | Maximum DDR_2X clock frequency | 444 | 408 | 355 | 355 | MHz |

**Notes:**

1. All performance numbers apply to both internal and external $V_{REF}$ configurations.

*Table 19:* **PS-PL Interface Performance**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $F_{EMIOGEMCLK}$ | EMIO gigabit Ethernet controller maximum frequency | – | 125 | MHz |
| $F_{EMIOSDCLK}$ | EMIO SD controller maximum frequency | – | 25 | MHz |
| $F_{EMIOSPICLK}$ | EMIO SPI controller maximum frequency | – | 25 | MHz |
| $F_{EMIOJTAGCLK}$ | EMIO JTAG controller maximum frequency | – | 20 | MHz |
| $F_{EMIOTRACECLK}$ | EMIO trace controller maximum frequency | – | 125 | MHz |
| $F_{FTMCLK}$ | Fabric trace monitor maximum frequency | – | 125 | MHz |
| $F_{EMIODMACLK}$ | DMA maximum frequency | – | 100 | MHz |
| $F_{AXI_MAX}$ | Maximum AXI interface performance | – | 250 | MHz |

# PS Switching Characteristics

## Clocks

*Table 20:* **System Reference Clock Input Requirements**

| Symbol | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $T_{JTPSCLK}$ | PS_CLK RMS clock jitter tolerance | – | – | ±0.5 | % |
| $T_{DCPSCLK}$ | PS_CLK duty cycle | 40 | – | 60 | % |
| $T_{RFPSCLK}$ | PS_CLK rise and fall time | – | – | 6 | ns |
| $F_{PSCLK}$ | PS_CLK frequency | 30 | – | 60 | MHz |

*Table 21:* **PS PLL Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1C/-1I/-1LI | -1Q | |
| $T_{LOCK_PSPLL}$ | PLL maximum lock time | 60 | 60 | 60 | 60 | µs |
| $F_{PSPLL_MAX}$ | PLL maximum output frequency | 2000 | 1800 | 1600 | 1600 | MHz |
| $F_{PSPLL_MIN}$ | PLL minimum output frequency | 780 | 780 | 780 | 780 | MHz |

## Resets

*Table 22:* **PS Reset Assertion Timing Requirements**

| Symbol | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $T_{PSPOR}$ | Required PS_POR_B assertion time(1) | 100 | – | – | µs |
| $T_{PSRST}$ | Required PS_SRST_B assertion time | 3 | – | – | PS_CLK Clock Cycles |

**Notes:**

1. PS_POR_B needs to be asserted Low until $T_{PSPOR}$ after PS supply voltages reach minimum levels.

The PS_POR_B deassertion must meet the following requirements to avoid coinciding with the secure lockdown window. Figure 1 shows the timing relationship between PS_POR_B and the last power supply ramp ($V_{CCINT}$, $V_{CCBRAM}$, $V_{CCAUX}$, or $V_{CCO}$ in bank 0). $T_{SLW}$ minimum and maximum parameters define the beginning and end, respectively, of the secure lockdown window relative to the last PL power supply reaching 250 mV. The PS_POR_B must not be deasserted within the secure lockdown window.

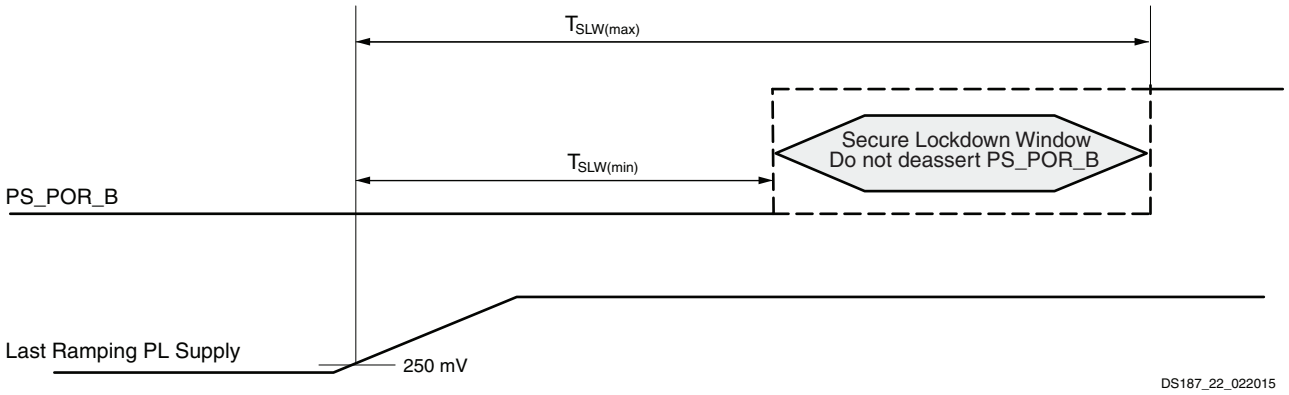


*Figure 1:* **PS_POR_B and Power Supply Ramp Timing Requirements**

*Table 23:* **PS Reset/Power Supply Timing Requirements**

| Symbol | Description | PS_CLK Frequency (MHz) | Min | Max | Units |
|---|---|---|---|---|---|
| $T_{SLW}$[1] | 128 KB CRC eFUSE disabled and PLL enabled. Default configuration | 30 | 12 | 39 | ms |
| | | 33.33 | 12 | 40 | ms |
| | | 60 | 13 | 40 | ms |
| | 128 KB CRC eFUSE disabled and PLL in bypass. | 30 | –32 | 13 | ms |
| | | 33.33 | –27 | 13 | ms |
| | | 60 | –9 | 25 | ms |
| | 128 KB CRC eFUSE enabled and PLL enabled.[2] | 30 | –19 | 9 | ms |
| | | 33.33 | –16 | 12 | ms |
| | | 60 | –3 | 25 | ms |
| | 128 KB CRC eFUSE enabled and PLL in bypass.[2] | 30 | –830 | –788 | ms |
| | | 33.33 | –746 | –705 | ms |
| | | 60 | –408 | –374 | ms |

**Notes:**

1. Valid for power supply ramp times of less than 6 ms. For ramp times longer than 6 ms, see the BootROM Performance section of the *Zynq-7000 SoC Technical Reference Manual* (UG585).
2. If any PS and PL power supplies are tied together, observe the PS_POR_B assertion time requirement ($T_{PSPOR}$) in Table 22 and its accompanying note.

## PS Configuration

*Table 24:* **Processor Configuration Access Port Switching Characteristics**

| Symbol | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $F_{PCAPCK}$ | Maximum processor configuration access port (PCAP) frequency | – | – | 100 | MHz |

## DDR Memory Interfaces

*Table 25:* **DDR3 Interface Switching Characteristics (1066 Mb/s)[1]**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $T_{DQVALID}$[2] | Input data valid window | 450 | – | ps |
| $T_{DQDS}$[3] | Output DQ to DQS skew | 131 | – | ps |
| $T_{DQDH}$[4] | Output DQS to DQ skew | 288 | – | ps |
| $T_{DQSS}$ | Output clock to DQS skew | –0.11 | 0.09 | $T_{CK}$ |
| $T_{CACK}$[5] | Command/address output setup time with respect to CLK | 532 | – | ps |
| $T_{CKCA}$[6] | Command/address output hold time with respect to CLK | 637 | – | ps |

**Notes:**

1. Recommended $V_{CCO_DDR}$ = 1.5V ±5%.
2. Measurement is taken from $V_{REF}$ to $V_{REF}$.
3. Measurement is taken from either the rising edge of DQ that crosses $V_{IH}$(AC) or the falling edge of DQ that crosses $V_{IL}$(AC) to $V_{REF}$ of DQS.
4. Measurement is taken from either the rising edge of DQ that crosses $V_{IL}$(DC) or the falling edge of DQ that crosses $V_{IH}$(DC) to $V_{REF}$ of DQS.
5. Measurement is taken from either the rising edge of CMD/ADDR that crosses $V_{IH}$(AC) or the falling edge of CMD/ADDR that crosses $V_{IL}$(AC) to $V_{REF}$ of CLK.
6. Measurement is taken from either the rising edge of CMD/ADDR that crosses $V_{IL}$(DC) or the falling edge of CMD/ADDR that crosses $V_{IH}$(DC) to $V_{REF}$ of CLK.

*Table 26:* **DDR3 Interface Switching Characteristics (800 Mb/s)(1)**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $T_{DQVALID}$(2) | Input data valid window | 500 | – | ps |
| $T_{DQDS}$(3) | Output DQ to DQS skew | 232 | – | ps |
| $T_{DQDH}$(4) | Output DQS to DQ skew | 401 | – | ps |
| $T_{DQSS}$ | Output clock to DQS skew | –0.10 | 0.06 | $T_{CK}$ |
| $T_{CACK}$(5) | Command/address output setup time with respect to CLK | 722 | – | ps |
| $T_{CKCA}$(6) | Command/address output hold time with respect to CLK | 882 | – | ps |

**Notes:**

1. Recommended $V_{CCO_DDR}$ = 1.5V ±5%.
2. Measurement is taken from $V_{REF}$ to $V_{REF}$.
3. Measurement is taken from either the rising edge of DQ that crosses $V_{IH}$(AC) or the falling edge of DQ that crosses $V_{IL}$(AC) to $V_{REF}$ of DQS.
4. Measurement is taken from either the rising edge of DQ that crosses $V_{IL}$(DC) or the falling edge of DQ that crosses $V_{IH}$(DC) to $V_{REF}$ of DQS.
5. Measurement is taken from either the rising edge of CMD/ADDR that crosses $V_{IH}$(AC) or the falling edge of CMD/ADDR that crosses $V_{IL}$(AC) to $V_{REF}$ of CLK.
6. Measurement is taken from either the rising edge of CMD/ADDR that crosses $V_{IL}$(DC) or the falling edge of CMD/ADDR that crosses $V_{IH}$(DC) to $V_{REF}$ of CLK.

*Table 27:* **DDR3L Interface Switching Characteristics (1066 Mb/s)(1)**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $T_{DQVALID}$(2) | Input data valid window | 450 | – | ps |
| $T_{DQDS}$(3) | Output DQ to DQS skew | 189 | – | ps |
| $T_{DQDH}$(4) | Output DQS to DQ skew | 267 | – | ps |
| $T_{DQSS}$ | Output clock to DQS skew | –0.13 | 0.04 | $T_{CK}$ |
| $T_{CACK}$(5) | Command/address output setup time with respect to CLK | 410 | – | ps |
| $T_{CKCA}$(6) | Command/address output hold time with respect to CLK | 629 | – | ps |

**Notes:**

1. Recommended $V_{CCO_DDR}$ = 1.35V ±5%.
2. Measurement is taken from $V_{REF}$ to $V_{REF}$.
3. Measurement is taken from either the rising edge of DQ that crosses $V_{IH}$(AC) or the falling edge of DQ that crosses $V_{IL}$(AC) to $V_{REF}$ of DQS.
4. Measurement is taken from either the rising edge of DQ that crosses $V_{IL}$(DC) or the falling edge of DQ that crosses $V_{IH}$(DC) to $V_{REF}$ of DQS.
5. Measurement is taken from either the rising edge of CMD/ADDR that crosses $V_{IH}$(AC) or the falling edge of CMD/ADDR that crosses $V_{IL}$(AC) to $V_{REF}$ of CLK.
6. Measurement is taken from either the rising edge of CMD/ADDR that crosses $V_{IL}$(DC) or the falling edge of CMD/ADDR that crosses $V_{IH}$(DC) to $V_{REF}$ of CLK.

*Table 28:* **DDR3L Interface Switching Characteristics (800 Mb/s)(1)**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $T_{DQVALID}$(2) | Input data valid window | 500 | – | ps |
| $T_{DQDS}$(3) | Output DQ to DQS skew | 321 | – | ps |
| $T_{DQDH}$(4) | Output DQS to DQ skew | 380 | – | ps |
| $T_{DQSS}$ | Output clock to DQS skew | –0.12 | 0.04 | $T_{CK}$ |
| $T_{CACK}$(5) | Command/address output setup time with respect to CLK | 636 | – | ps |

*Table 28:* **DDR3L Interface Switching Characteristics (800 Mb/s)(1) *(Cont'd)***

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $T_{CKCA}$(6) | Command/address output hold time with respect to CLK | 853 | – | ps |

**Notes:**

1. Recommended $V_{CCO_DDR}$ = 1.35V ±5%.
2. Measurement is taken from $V_{REF}$ to $V_{REF}$.
3. Measurement is taken from either the rising edge of DQ that crosses $V_{IH}$(AC) or the falling edge of DQ that crosses $V_{IL}$(AC) to $V_{REF}$ of DQS.
4. Measurement is taken from either the rising edge of DQ that crosses $V_{IL}$(DC) or the falling edge of DQ that crosses $V_{IH}$(DC) to $V_{REF}$ of DQS.
5. Measurement is taken from either the rising edge of CMD/ADDR that crosses $V_{IH}$(AC) or the falling edge of CMD/ADDR that crosses $V_{IL}$(AC) to $V_{REF}$ of CLK.
6. Measurement is taken from either the rising edge of CMD/ADDR that crosses $V_{IL}$(DC) or the falling edge of CMD/ADDR that crosses $V_{IH}$(DC) to $V_{REF}$ of CLK.

*Table 29:* **LPDDR2 Interface Switching Characteristics (800 Mb/s)(1)**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $T_{DQVALID}$(2) | Input data valid window | 500 | – | ps |
| $T_{DQDS}$(3) | Output DQ to DQS skew | 196 | – | ps |
| $T_{DQDH}$(4) | Output DQS to DQ skew | 328 | – | ps |
| $T_{DQSS}$ | Output clock to DQS skew | 0.90 | 1.06 | $T_{CK}$ |
| $T_{CACK}$(5) | Command/address output setup time with respect to CLK | 202 | – | ps |
| $T_{CKCA}$(6) | Command/address output hold time with respect to CLK | 353 | – | ps |

**Notes:**

1. Recommended $V_{CCO_DDR}$ = 1.2V ±5%.
2. Measurement is taken from $V_{REF}$ to $V_{REF}$.
3. Measurement is taken from either the rising edge of DQ that crosses $V_{IH}$(AC) or the falling edge of DQ that crosses $V_{IL}$(AC) to $V_{REF}$ of DQS.
4. Measurement is taken from either the rising edge of DQ that crosses $V_{IL}$(DC) or the falling edge of DQ that crosses $V_{IH}$(DC) to $V_{REF}$ of DQS.
5. Measurement is taken from either the rising edge of CMD/ADDR that crosses $V_{IH}$(AC) or the falling edge of CMD/ADDR that crosses $V_{IL}$(AC) to $V_{REF}$ of CLK.
6. Measurement is taken from either the rising edge of CMD/ADDR that crosses $V_{IL}$(DC) or the falling edge of CMD/ADDR that crosses $V_{IH}$(DC) to $V_{REF}$ of CLK.

*Table 30:* **LPDDR2 Interface Switching Characteristics (400 Mb/s)(1)**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $T_{DQVALID}$(2) | Input data valid window | 500 | – | ps |
| $T_{DQDS}$(3) | Output DQ to DQS skew | 664 | – | ps |
| $T_{DQDH}$(4) | Output DQS to DQ skew | 766 | – | ps |
| $T_{DQSS}$ | Output clock to DQS skew | 0.90 | 1.06 | $T_{CK}$ |
| $T_{CACK}$(5) | Command/address output setup time with respect to CLK | 731 | – | ps |
| $T_{CKCA}$(6) | Command/address output hold time with respect to CLK | 907 | – | ps |

**Notes:**

1. Recommended $V_{CCO_DDR}$ = 1.2V ±5%.
2. Measurement is taken from $V_{REF}$ to $V_{REF}$.
3. Measurement is taken from either the rising edge of DQ that crosses $V_{IH}$(AC) or the falling edge of DQ that crosses $V_{IL}$(AC) to $V_{REF}$ of DQS.
4. Measurement is taken from either the rising edge of DQ that crosses $V_{IL}$(DC) or the falling edge of DQ that crosses $V_{IH}$(DC) to $V_{REF}$ of DQS.
5. Measurement is taken from either the rising edge of CMD/ADDR that crosses $V_{IH}$(AC) or the falling edge of CMD/ADDR that crosses $V_{IL}$(AC) to $V_{REF}$ of CLK.
6. Measurement is taken from either the rising edge of CMD/ADDR that crosses $V_{IL}$(DC) or the falling edge of CMD/ADDR that crosses $V_{IH}$(DC) to $V_{REF}$ of CLK.

*Table 31:* **DDR2 Interface Switching Characteristics (800 Mb/s)(1)**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $T_{DQVALID}$(2) | Input data valid window | 500 | – | ps |
| $T_{DQDS}$(3) | Output DQ to DQS skew | 147 | – | ps |
| $T_{DQDH}$(4) | Output DQS to DQ skew | 376 | – | ps |
| $T_{DQSS}$ | Output clock to DQS skew | –0.07 | 0.08 | $T_{CK}$ |
| $T_{CACK}$(5) | Command/address output setup time with respect to CLK | 732 | – | ps |
| $T_{CKCA}$(6) | Command/address output hold time with respect to CLK | 938 | – | ps |

**Notes:**

1. Recommended $V_{CCO_DDR}$ = 1.8V ±5%.
2. Measurement is taken from $V_{REF}$ to $V_{REF}$.
3. Measurement is taken from either the rising edge of DQ that crosses $V_{IH}$(AC) or the falling edge of DQ that crosses $V_{IL}$(AC) to $V_{REF}$ of DQS.
4. Measurement is taken from either the rising edge of DQ that crosses $V_{IL}$(DC) or the falling edge of DQ that crosses $V_{IH}$(DC) to $V_{REF}$ of DQS.
5. Measurement is taken from either the rising edge of CMD/ADDR that crosses $V_{IH}$(AC) or the falling edge of CMD/ADDR that crosses $V_{IL}$(AC) to $V_{REF}$ of CLK.
6. Measurement is taken from either the rising edge of CMD/ADDR that crosses $V_{IL}$(DC) or the falling edge of CMD/ADDR that crosses $V_{IH}$(DC) to $V_{REF}$ of CLK.

*Table 32:* **DDR2 Interface Switching Characteristics (400 Mb/s)(1)**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $T_{DQVALID}$(2) | Input data valid window | 500 | – | ps |
| $T_{DQDS}$(3) | Output DQ to DQS skew | 385 | – | ps |
| $T_{DQDH}$(4) | Output DQS to DQ skew | 662 | – | ps |
| $T_{DQSS}$ | Output clock to DQS skew | –0.11 | 0.06 | $T_{CK}$ |
| $T_{CACK}$(5) | Command/address output setup time with respect to CLK | 1760 | – | ps |
| $T_{CKCA}$(6) | Command/address output hold time with respect to CLK | 1739 | – | ps |

**Notes:**

1. Recommended $V_{CCO_DDR}$ = 1.8V ±5%.
2. Measurement is taken from $V_{REF}$ to $V_{REF}$.
3. Measurement is taken from either the rising edge of DQ that crosses $V_{IH}$(AC) or the falling edge of DQ that crosses $V_{IL}$(AC) to $V_{REF}$ of DQS.
4. Measurement is taken from either the rising edge of DQ that crosses $V_{IL}$(DC) or the falling edge of DQ that crosses $V_{IH}$(DC) to $V_{REF}$ of DQS.
5. Measurement is taken from either the rising edge of CMD/ADDR that crosses $V_{IH}$(AC) or the falling edge of CMD/ADDR that crosses $V_{IL}$(AC) to $V_{REF}$ of CLK.
6. Measurement is taken from either the rising edge of CMD/ADDR that crosses $V_{IL}$(DC) or the falling edge of CMD/ADDR that crosses $V_{IH}$(DC) to $V_{REF}$ of CLK.

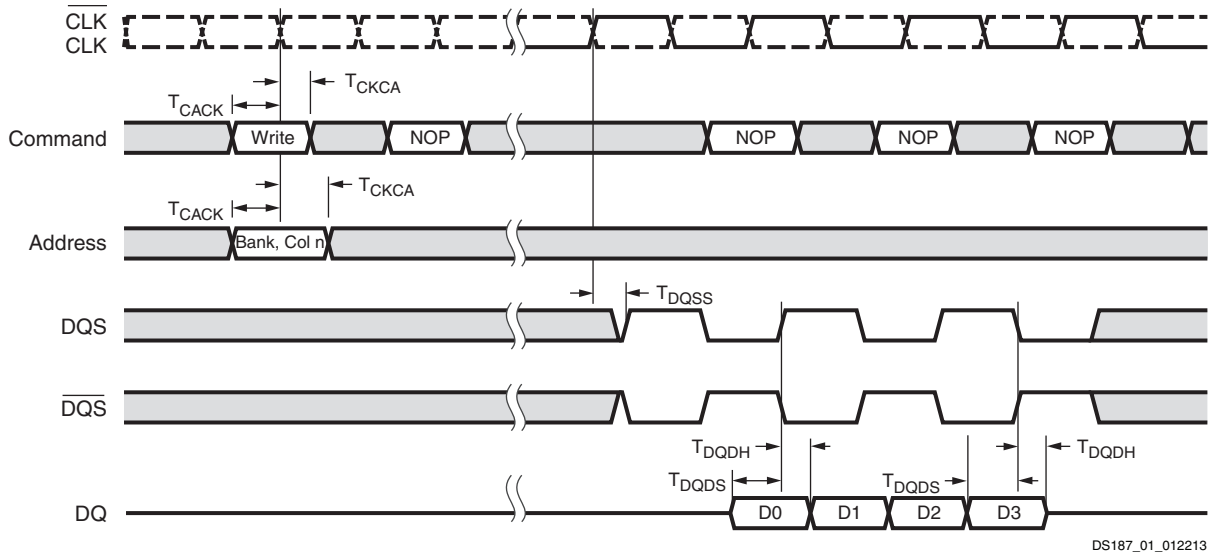


*Figure 2:* **DDR Output Timing Diagram**

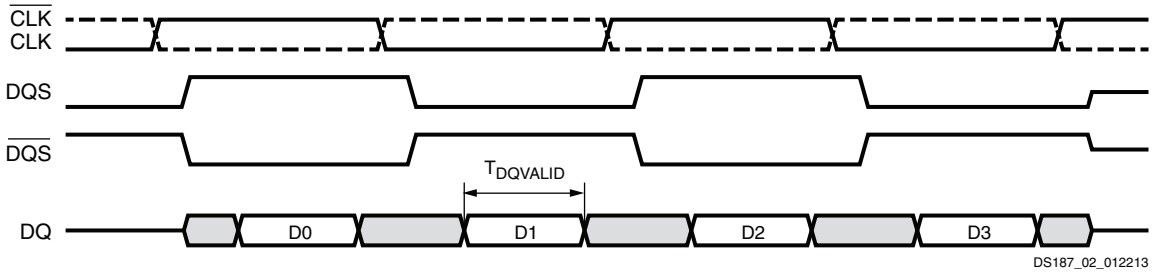


*Figure 3:* **DDR Input Timing Diagram**

## Static Memory Controller

*Table 33:* **SMC Interface Delay Characteristics(1)(2)**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $T_{NANDDOUT}$ | NAND_IO output delay from last register to pad | 4.12 | 6.45 | ns |
| $T_{NANDALE}$ | NAND_ALE output delay from last register to pad | 5.08 | 6.33 | ns |
| $T_{NANDCLE}$ | NAND_CLE output delay from last register to pad | 4.87 | 6.40 | ns |
| $T_{NANDWE}$ | NAND_WE_B output delay from last register to pad | 4.69 | 5.89 | ns |
| $T_{NANDRE}$ | NAND_RE_B output delay from last register to pad | 5.12 | 6.44 | ns |
| $T_{NANDCE}$ | NAND_CE_B output delay from last register to pad | 4.68 | 5.89 | ns |
| $T_{NANDDIN}$ | NAND_IO setup time and input delay from pad to first register | 1.48 | 3.09 | ns |
| $T_{NANDBUSY}$ | NAND_BUSY setup time and input delay from pad to first register | 2.48 | 3.33 | ns |
| $T_{SRAMA}$ | SRAM_A output delay from last register to pad | 3.94 | 5.73 | ns |
| $T_{SRAMDOUT}$ | SRAM_DQ output delay from last register to pad | 4.66 | 6.45 | ns |
| $T_{SRAMCE}$ | SRAM_CE output delay from last register to pad | 4.57 | 5.95 | ns |
| $T_{SRAMOE}$ | SRAM_OE_B output delay from last register to pad | 4.79 | 6.13 | ns |
| $T_{SRAMBLS}$ | SRAM_BLS_B output delay from last register to pad | 5.25 | 6.74 | ns |
| $T_{SRAMWE}$ | SRAM_WE_B output delay from last register to pad | 5.12 | 6.48 | ns |
| $T_{SRAMDIN}$ | SRAM_DQ setup time and input delay from pad to first register | 1.93 | 3.05 | ns |
| $T_{SRAMWAIT}$ | SRAM_WAIT setup time and input delay from pad to first register | 2.26 | 3.15 | ns |
| $F_{SMC_REF_CLK}$ | SMC reference clock frequency | – | 100 | MHz |

**Notes:**

1. All parameters do not include the package flight time and register controlled delays.
2. Refer to the ARM® PrimeCell® Static Memory Controller (PL350 series) Technical Reference Manual for more SMC timing details.

## Quad-SPI Interfaces

*Table 34:* **Quad-SPI Interface Switching Characteristics**

| Symbol | Description | Load Conditions | Min | Max | Units |
|---|---|---|---|---|---|
| **Feedback Clock Enabled** | | | | | |
| $T_{DCQSPICLK1}$ | Quad-SPI clock duty cycle | All(1)(2) | 44 | 56 | % |
| $T_{QSPICKO1}$ | Data and slave select output delay | 15 pF(1) | –0.10(3) | 2.30 | ns |
| | | 30 pF(2) | –1.00 | 3.80 | |
| $T_{QSPIDCK1}$ | Input data setup time | 15 pF(1) | 2.00 | – | ns |
| | | 30 pF(2) | 3.30 | – | |
| $T_{QSPICKD1}$ | Input data hold time | 15 pF(1) | 1.30 | – | ns |
| | | 30 pF(2) | 1.50 | – | |
| $T_{QSPISSCLK1}$ | Slave select asserted to next clock edge | All(1)(2) | 1 | – | $F_{QSPI_REF_CLK}$ cycle |
| $T_{QSPICLKSS1}$ | Clock edge to slave select deasserted | All(1)(2) | 1 | – | $F_{QSPI_REF_CLK}$ cycle |
| $F_{QSPICLK1}$ | Quad-SPI device clock frequency | 15 pF(1) | – | 100(4) | MHz |
| | | 30 pF(2) | – | 70(4) | |
| **Feedback Clock Disabled** | | | | | |
| $T_{DCQSPICLK2}$ | Quad-SPI clock duty cycle | All(1)(2) | 44 | 56 | % |
| $T_{QSPICKO2}$ | Data and slave select output delay | 15 pF(1) | –0.10 | 3.80 | ns |
| | | 30 pF(2) | –1.00 | 3.80 | ns |
| $T_{QSPIDCK2}$ | Input data setup time | All(1)(2) | 6 | – | ns |
| $T_{QSPICKD2}$ | Input data hold time | All(1)(2) | 12.5 | – | ns |
| $T_{QSPISSCLK2}$ | Slave select asserted to next clock edge | All(1)(2) | 1 | – | $F_{QSPI_REF_CLK}$ cycle |
| $T_{QSPICLKSS2}$ | Clock edge to slave select deasserted | All(1)(2) | 1 | – | $F_{QSPI_REF_CLK}$ cycle |
| $F_{QSPICLK2}$ | Quad-SPI device clock frequency | All(1)(2) | – | 40 | MHz |
| **Feedback Clock Enabled or Disabled** | | | | | |
| $F_{QSPI_REF_CLK}$ | Quad-SPI reference clock frequency | All(1)(2) | – | 200 | MHz |

**Notes:**

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads, feedback clock pin has no load. Quad-SPI single slave select 4-bit I/O mode.
2. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 30 pF loads in 4-bit stacked I/O configuration, feedback clock pin has no load. Quad-SPI single slave select 4-bit I/O mode.
3. The $T_{QSPICKO1}$ is an effective value. Use it to compute the available memory device input setup and hold timing budgets based on the given device clock-out duty-cycle limits.
4. Requires appropriate component selection/board design.

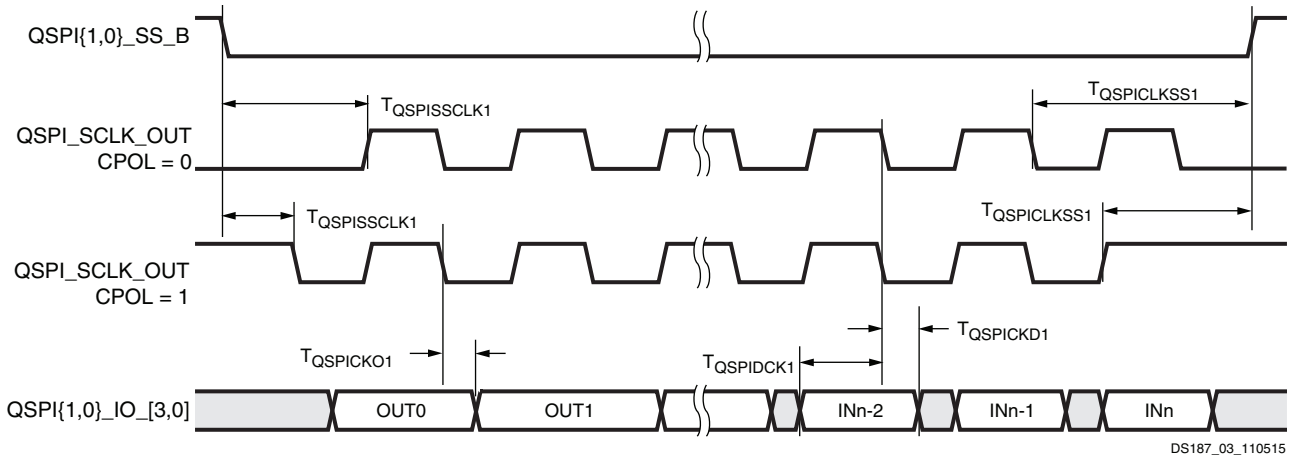


*Figure 4:* **Quad-SPI Interface (Feedback Clock Enabled) Timing Diagram**

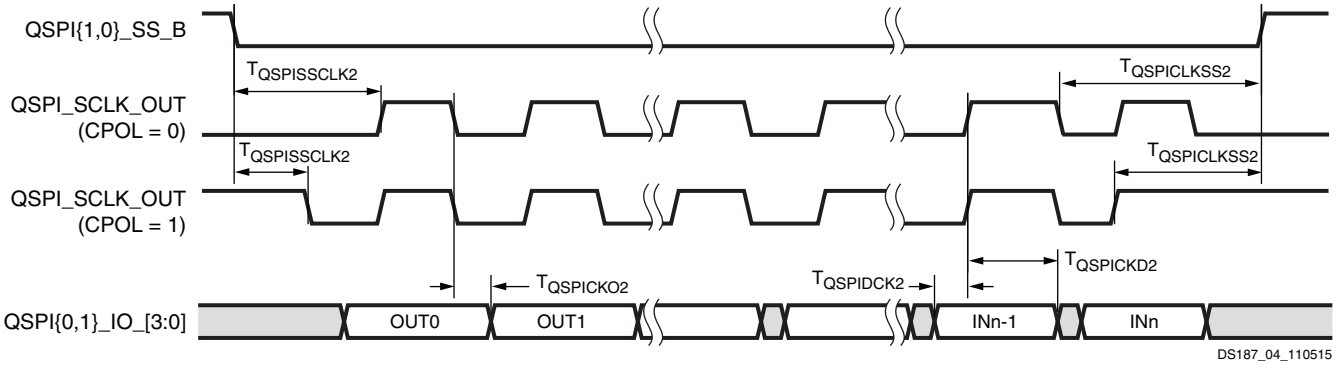


*Figure 5:* **Quad-SPI Interface (Feedback Clock Disabled) Timing Diagram**

## ULPI Interfaces

*Table 35:* **ULPI Interface Clock Receiving Mode Switching Characteristics**(1)(2)

| Symbol | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $T_{ULPIDCK}$ | Input setup to ULPI clock, all inputs | 3.00 | – | – | ns |
| $T_{ULPICKD}$ | Input hold to ULPI clock, all inputs | 1.00 | – | – | ns |
| $T_{ULPICKO}$ | ULPI clock to output valid, all outputs | 1.70 | – | 8.86 | ns |
| $F_{ULPICLK}$ | ULPI device clock frequency | – | 60 | – | MHz |

**Notes:**

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads, 60 MHz device clock frequency.
2. All timing values assume an ideal external input clock. Actual design system timing budgets should account for additional external clock jitter.

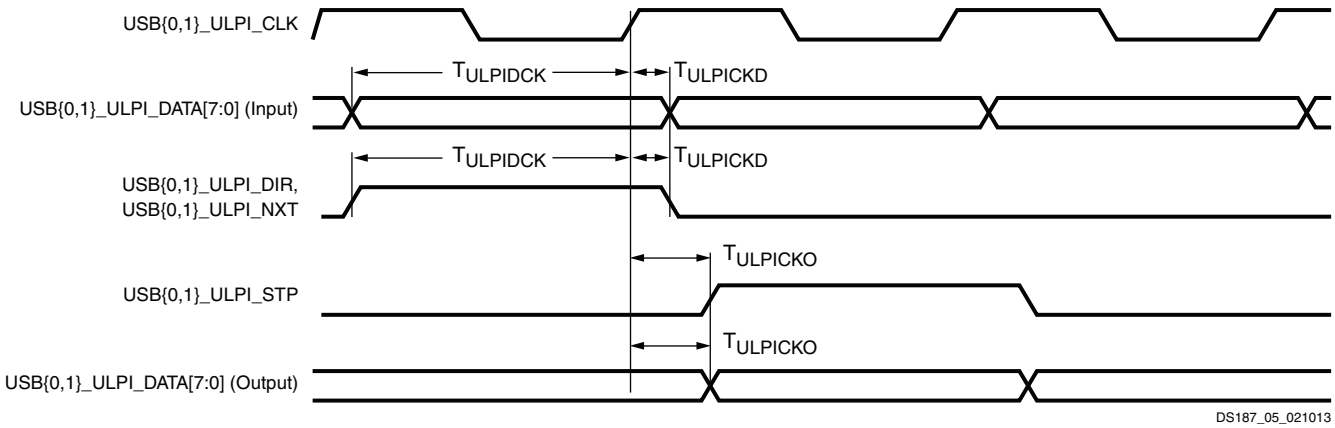


*Figure 6:* **ULPI Interface Timing Diagram**

## RGMII and MDIO Interfaces

*Table 36:* **RGMII and MDIO Interface Switching Characteristics(1)(2)(3)**

| Symbol | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $T_{DCGETXCLK}$ | Transmit clock duty cycle | 45 | – | 55 | % |
| $T_{GEMTXCKO}$ | RGMII_TX_D[3:0], RGMII_TX_CTL output clock to out time | –0.50 | – | 0.50 | ns |
| $T_{GEMRXDCK}$ | RGMII_RX_D[3:0], RGMII_RX_CTL input setup time | 0.80 | – | – | ns |
| $T_{GEMRXCKD}$ | RGMII_RX_D[3:0], RGMII_RX_CTL input hold time | 0.80 | – | – | ns |
| $T_{MDIOCLK}$ | MDC output clock period | 400 | – | – | ns |
| $T_{MDIOCKH}$ | MDC clock High time | 160 | – | – | ns |
| $T_{MDIOCKL}$ | MDC clock Low time | 160 | – | – | ns |
| $T_{MDIODCK}$ | MDIO input data setup time | 80 | – | – | ns |
| $T_{MDIOCKD}$ | MDIO input data hold time | 0 | – | – | ns |
| $T_{MDIOCKO}$ | MDIO data output delay | –20 | – | 170 | ns |
| $F_{GETXCLK}$ | RGMII_TX_CLK transmit clock frequency | – | 125 | – | MHz |
| $F_{GERXCLK}$ | RGMII_RX_CLK receive clock frequency | – | 125 | – | MHz |
| $F_{ENET_REF_CLK}$ | Ethernet reference clock frequency | – | 125 | – | MHz |

**Notes:**

1. Test conditions: LVCMOS25, fast slew rate, 8 mA drive strength, 15 pF loads. Values in this table are specified during 1000 Mb/s operation.
2. LVCMOS25 slow slew rate and LVCMOS33 are not supported.
3. All timing values assume an ideal external input clock. Actual design system timing budgets should account for additional external clock jitter.

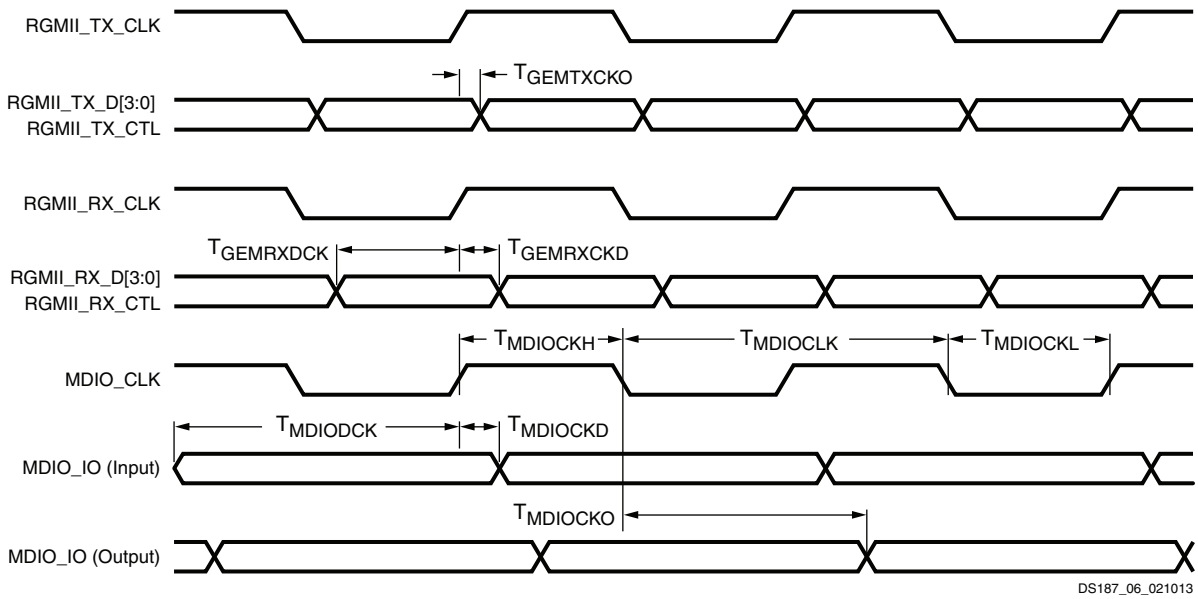


*Figure 7:* **RGMII Interface Timing Diagram**

## SD/SDIO Interfaces

*Table 37:* **SD/SDIO Interface High Speed Mode Switching Characteristics(1)**

| Symbol | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $T_{DCSDHSCLK}$ | SD device clock duty cycle | – | 50 | – | % |
| $T_{SDHSCKO}$ | Clock to output delay, all outputs | 2.00 | – | 12.00 | ns |
| $T_{SDHSDCK}$ | Input setup time, all inputs | 3.00 | – | – | ns |
| $T_{SDHSCKD}$ | Input hold time, all inputs | 1.05 | – | – | ns |
| $F_{SD_REF_CLK}$ | SD reference clock frequency | – | – | 125 | MHz |
| $F_{SDHSCLK}$ | High speed mode SD device clock frequency | 0 | – | 50 | MHz |

**Notes:**

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.

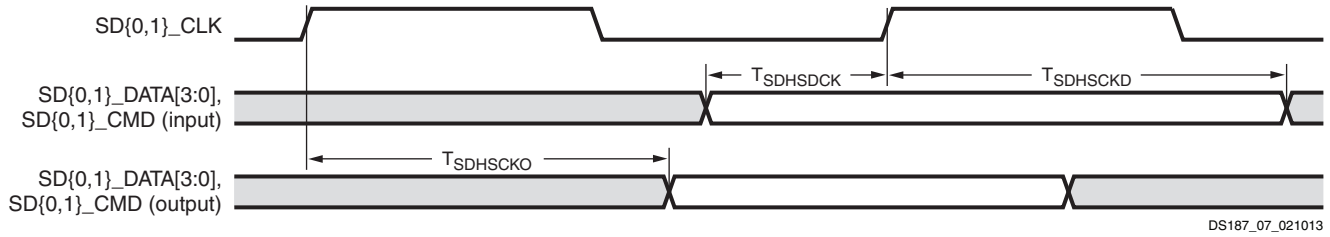


*Figure 8:* **SD/SDIO Interface High Speed Mode Timing Diagram**

*Table 38:* **SD/SDIO Interface Switching Characteristics(1)**

| Symbol | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $T_{DCSDSCLK}$ | SD device clock duty cycle | – | 50 | – | % |
| $T_{SDSCKO}$ | Clock to output delay, all outputs | 2.00 | – | 12.00 | ns |
| $T_{SDSDCK}$ | Input setup time, all inputs | 4.00 | – | – | ns |
| $T_{SDSCKD}$ | Input hold time, all inputs | 3.00 | – | – | ns |
| $F_{SD_REF_CLK}$ | SD reference clock frequency | – | – | 125 | MHz |
| $F_{SDIDCLK}$ | Clock frequency in identification mode | – | – | 400 | KHz |
| $F_{SDSCLK}$ | Standard mode SD device clock frequency | 0 | – | 25 | MHz |

**Notes:**

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.

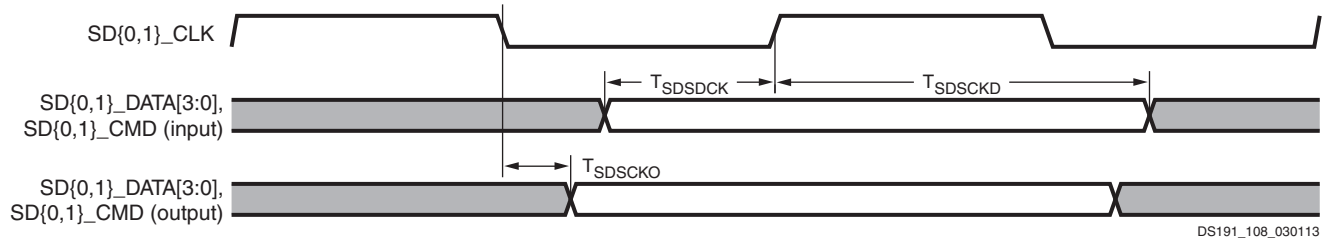


*Figure 9:* **SD/SDIO Interface Standard Mode Timing Diagram**

## I2C Interfaces

*Table 39:* **I2C Fast Mode Interface Switching Characteristics(1)**

| Symbol | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $T_{DCI2CFCLK}$ | I2C{0,1}SCL duty cycle | – | 50 | – | % |
| $T_{I2CFCKO}$ | I2C{0,1}SDAO clock to out delay | – | – | 900 | ns |
| $T_{I2CFDCK}$ | I2C{0,1}SDAI setup time | 100 | – | – | ns |
| $F_{I2CFCLK}$ | I2C{0,1}SCL clock frequency | – | – | 400 | KHz |

**Notes:**

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.

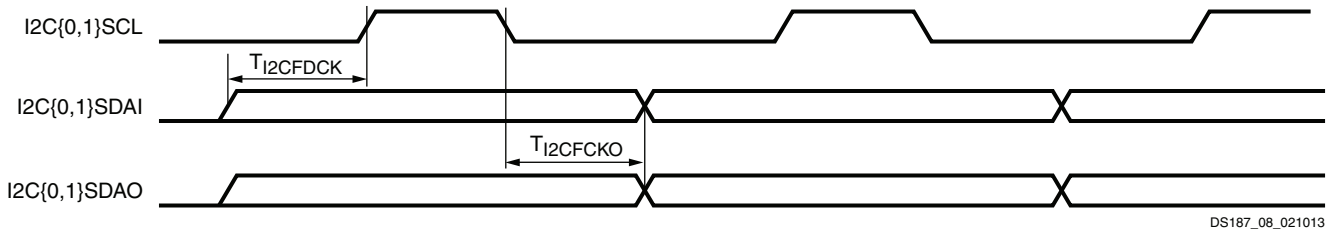


*Figure 10:* **I2C Fast Mode Interface Timing Diagram**

*Table 40:* **I2C Standard Mode Interface Switching Characteristics(1)**

| Symbol | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $T_{DCI2CSCLK}$ | I2C{0,1}SCL duty cycle | – | 50 | – | % |
| $T_{I2CSCKO}$ | I2C{0,1}SDAO clock to out delay | – | – | 3450 | ns |
| $T_{I2CSDCK}$ | I2C{0,1}SDAI setup time | 250 | – | – | ns |
| $F_{I2CSCLK}$ | I2C{0,1}SCL clock frequency | – | – | 100 | KHz |

**Notes:**

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.

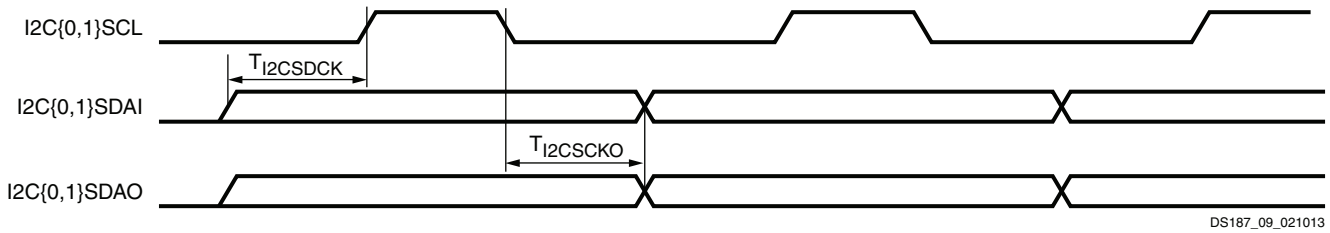


*Figure 11:* **I2C Standard Mode Interface Timing Diagram**

## SPI Interfaces

*Table 41:* **SPI Master Mode Interface Switching Characteristics(1)**

| Symbol | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $T_{DCMSPICLK}$ | SPI master mode clock duty cycle | – | 50 | – | % |
| $T_{MSPIDCK}$ | Input setup time for SPI{0,1}_MISO | 2.00 | – | – | ns |
| $T_{MSPICKD}$ | Input hold time for SPI{0,1}_MISO | 8.20 | – | – | ns |
| $T_{MSPICKO}$ | Output delay for SPI{0,1}_MOSI and SPI{0,1}_SS | –3.10 | – | 3.90 | ns |
| $T_{MSPISSCLK}$ | Slave select asserted to first active clock edge | 1 | – | – | $F_{SPI_REF_CLK}$ cycles |
| $T_{MSPICLKSS}$ | Last active clock edge to slave select deasserted | 0.5 | – | – | $F_{SPI_REF_CLK}$ cycles |
| $F_{MSPICLK}$ | SPI master mode device clock frequency | – | – | 50.00 | MHz |
| $F_{SPI_REF_CLK}$ | SPI reference clock frequency | – | – | 200.00 | MHz |

**Notes:**

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.

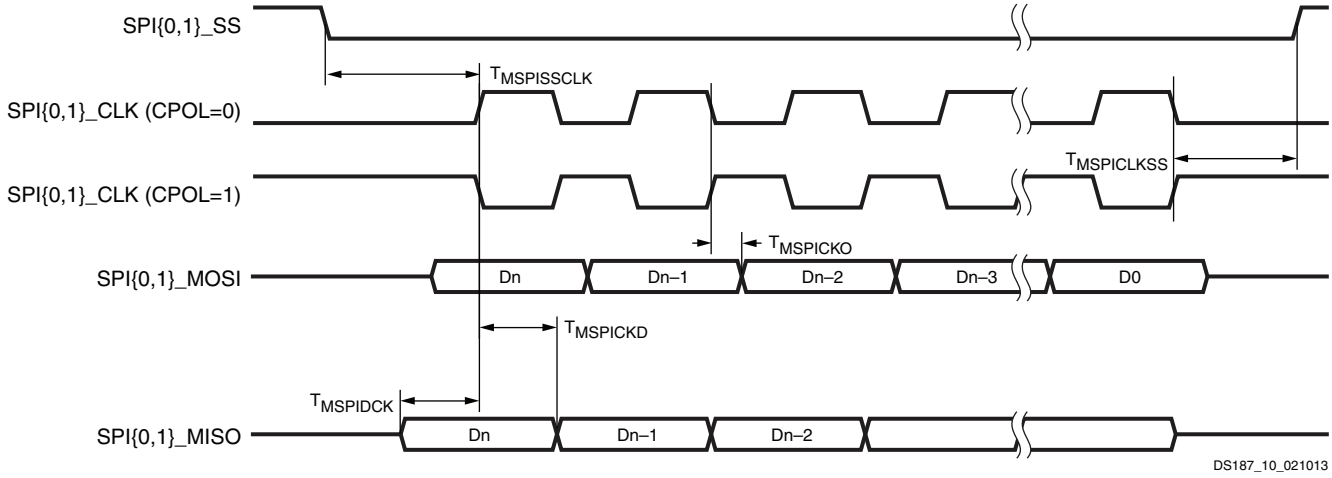


*Figure 12:* **SPI Master (CPHA = 0) Interface Timing Diagram**

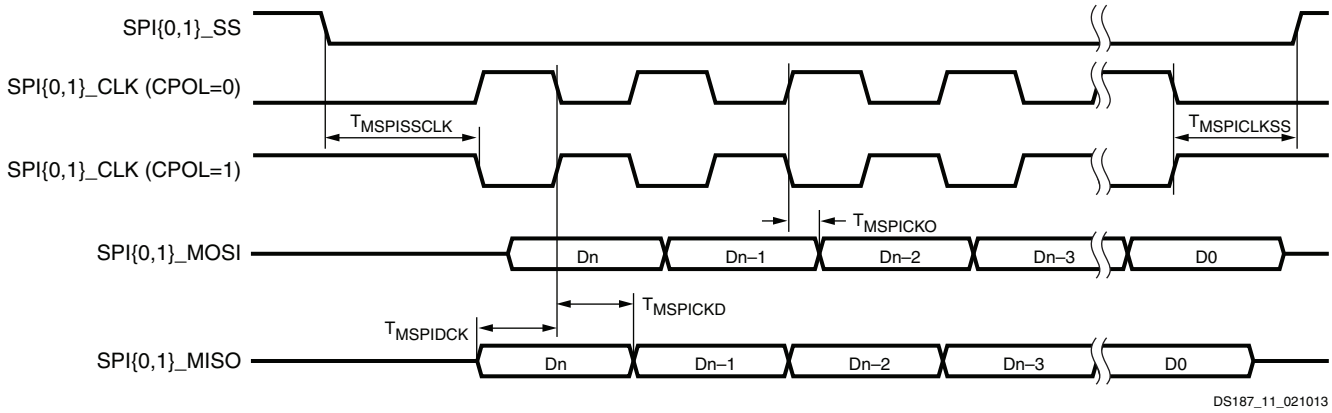


*Figure 13:* **SPI Master (CPHA = 1) Interface Timing Diagram**

*Table 42:* **SPI Slave Mode Interface Switching Characteristics(1)(2)**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $T_{SSPIDCK}$ | Input setup time for SPI{0,1}_MOSI and SPI{0,1}_SS | 1 | – | $F_{SPI_REF_CLK}$ cycles |
| $T_{SSPICKD}$ | Input hold time for SPI{0,1}_MOSI and SPI{0,1}_SS | 1 | – | $F_{SPI_REF_CLK}$ cycles |
| $T_{SSPICKO}$ | Output delay for SPI{0,1}_MISO | 0 | 2.6 | $F_{SPI_REF_CLK}$ cycles |
| $T_{SSPISSCLK}$ | Slave select asserted to first active clock edge | 1 | – | $F_{SPI_REF_CLK}$ cycles |
| $T_{SSPICLKSS}$ | Last active clock edge to slave select deasserted | 1 | – | $F_{SPI_REF_CLK}$ cycles |
| $F_{SSPICLK}$ | SPI slave mode device clock frequency | – | 25 | MHz |
| $F_{SPI_REF_CLK}$ | SPI reference clock frequency | – | 200 | MHz |

**Notes:**

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.
2. All timing values assume an ideal external input clock. Actual design system timing budgets should account for additional external clock jitter.

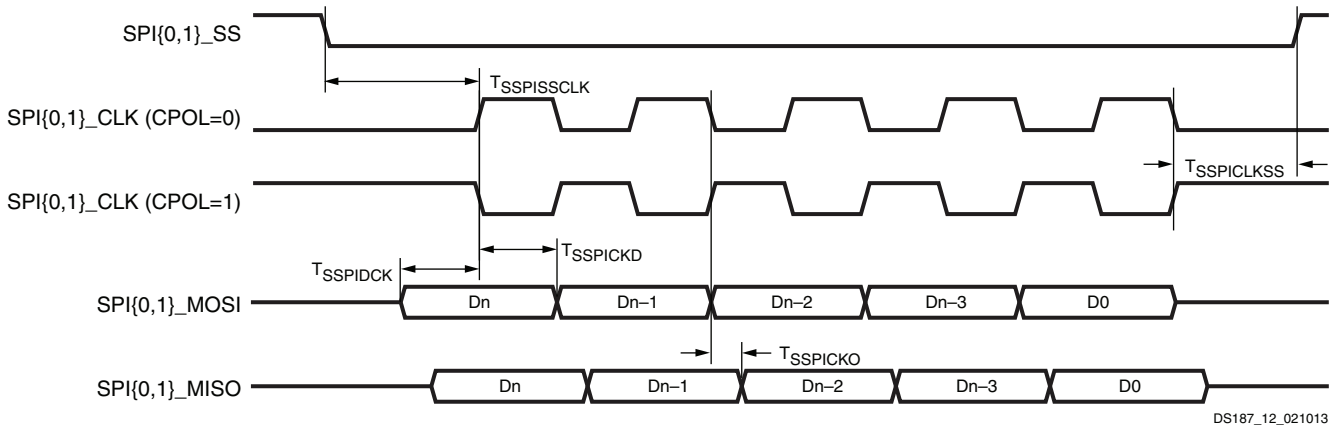


*Figure 14:* **SPI Slave (CPHA = 0) Interface Timing Diagram**

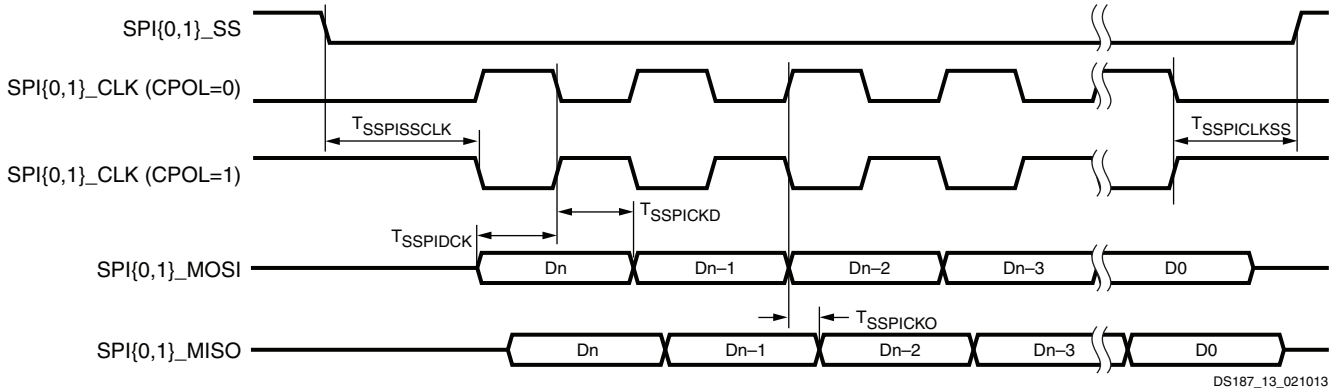


*Figure 15:* **SPI Slave (CPHA = 1) Interface Timing Diagram**

## CAN Interfaces

*Table 43:* **CAN Interface Switching Characteristics(1)**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $T_{PWCANRX}$ | Minimum receive pulse width | 1 | – | µs |
| $T_{PWCANTX}$ | Minimum transmit pulse width | 1 | – | µs |
| $F_{CAN_REF_CLK}$ | Internally sourced CAN reference clock frequency | – | 100 | MHz |
| | Externally sourced CAN reference clock frequency | – | 40 | MHz |

**Notes:**

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.

## PJTAG Interfaces

*Table 44:* **PJTAG Interface(1)(2)**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $T_{PJTAGDCK}$ | PJTAG input setup time | 2.4 | – | ns |
| $T_{PJTAGCKD}$ | PJTAG input hold time | 2.0 | – | ns |
| $T_{PJTAGCKO}$ | PJTAG clock to out delay | – | 12.5 | ns |
| $T_{PJTAGCLK}$ | PJTAG clock frequency | – | 20 | MHz |

**Notes:**

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.
2. All timing values assume an ideal external input clock. Actual design system timing budgets should account for additional external clock jitter.

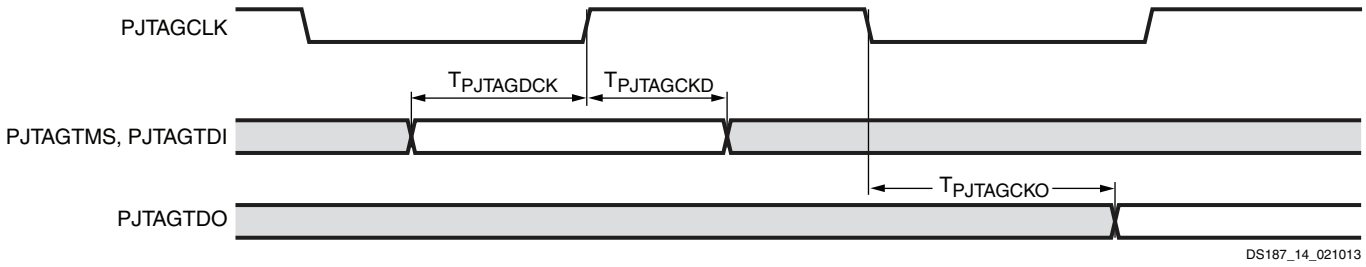


*Figure 16:* **PJTAG Interface Timing Diagram**

## UART Interfaces

*Table 45:* **UART Interface Switching Characteristics(1)**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $BAUD_{TXMAX}$ | Maximum transmit baud rate | – | 1 | Mb/s |
| $BAUD_{RXMAX}$ | Maximum receive baud rate | – | 1 | Mb/s |
| $F_{UART_REF_CLK}$ | UART reference clock frequency | – | 100 | MHz |

**Notes:**

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.

## GPIO Interfaces

*Table 46:* **GPIO Banks Switching Characteristics(1)**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $T_{PWGPIOH}$ | Input high pulse width | 10 x 1/cpu1x | – | µs |
| $T_{PWGPIOL}$ | Input low pulse width | 10 x 1/cpu1x | – | µs |

**Notes:**

1. Pulse width requirement for interrupt.

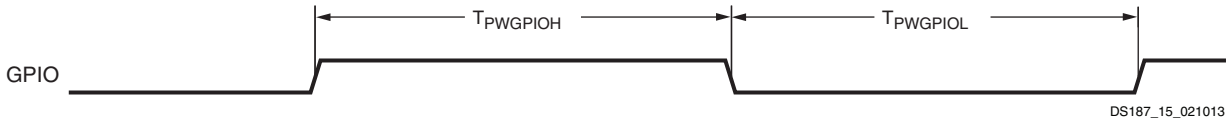


*Figure 17:* **GPIO Interface Timing Diagram**

## Trace Interface

*Table 47:* **Trace Interface Switching Characteristics(1)**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $T_{TCECKO}$ | Trace clock to output delay, all outputs | –1.4 | 1.5 | ns |
| $T_{DCTCECLK}$ | Trace clock duty cycle | 40 | 60 | % |
| $F_{TCECLK}$ | Trace clock frequency | – | 80 | MHz |

**Notes:**

1. Test conditions: LVCMOS25, fast slew rate, 8 mA drive strength, 15 pF loads.

## Triple Timer Counter Interface

*Table 48:* **Triple Timer Counter interface Switching Characteristics(1)**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $T_{PWTTCOCLK}$ | Triple timer counter output clock pulse width | 2 x 1/cpu1x | – | ns |
| $F_{TTCOCLK}$ | Triple timer counter output clock frequency | – | cpu1x/4 | MHz |
| $T_{TTCICLKH}$ | Triple timer counter input clock high pulse width | 1.5 x 1/cpu1x | – | ns |
| $T_{TTCICLKL}$ | Triple timer counter input clock low pulse width | 1.5 x 1/cpu1x | – | ns |
| $F_{TTCICLK}$ | Triple timer counter input clock frequency | – | cpu1x/3 | MHz |

**Notes:**

1. All timing values assume an ideal external input clock. Actual design system timing budgets should account for additional external clock jitter.

## Watchdog Timer

*Table 49:* **Watchdog Timer Switching Characteristics**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $F_{WDTCLK}$(1) | Watchdog timer input clock frequency | – | 10 | MHz |

**Notes:**

1. Applies to external input clock through MIO pin only.

## PL Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in the PL. The numbers reported here are worst-case values; they have all been fully characterized. These values are subject to the same guidelines as the AC Switching Characteristics, page 13.

*Table 50:* **PL Networking Applications Interface Performances**

| Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|
| | -3 | -2 | -1C/-1I/-1LI | -1Q | |
| SDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 8) | 680 | 680 | 600 | 600 | Mb/s |
| DDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 14) | 1250 | 1250 | 950 | 950 | Mb/s |
| SDR LVDS receiver (SFI-4.1)(1) | 680 | 680 | 600 | 600 | Mb/s |
| DDR LVDS receiver (SPI-4.2)(1) | 1250 | 1250 | 950 | 950 | Mb/s |

**Notes:**

1. LVDS receivers are typically bounded with certain applications where specific dynamic phase-alignment (DPA) algorithms dominate deterministic performance.

*Table 51:* **Maximum Physical Interface (PHY) Rate for Memory Interfaces IP available with the Memory Interface Generator(1)(2)**

| Memory Standard | Speed Grade | | | | Units |
|---|---|---|---|---|---|
| | -3 | -2 | -1C/-1I/-1LI | -1Q | |
| **4:1 Memory Controllers** | | | | | |
| DDR3 | 1066(3) | 800 | 800 | 667 | Mb/s |
| DDR3L | 800 | 800 | 667 | N/A | Mb/s |
| DDR2 | 800 | 800 | 667 | 533 | Mb/s |
| **2:1 Memory Controllers** | | | | | |
| DDR3 | 800 | 700 | 620 | 620 | Mb/s |
| DDR3L | 800 | 700 | 620 | N/A | Mb/s |
| DDR2 | 800 | 700 | 620 | 533 | Mb/s |
| LPDDR2 | 667 | 667 | 533 | 400 | Mb/s |

**Notes:**

1. $V_{REF}$ tracking is required. For more information, see the *Zynq-7000 SoC and 7 Series Devices Memory Interface Solutions User Guide* (UG586).
2. When using the internal $V_{REF}$, the maximum data rate is 800 Mb/s (400 MHz).
3. The maximum PHY rate is 800 Mb/s in bank 13 of the XC7Z015, XC7Z020, XA7Z020, and XQ7Z020 devices.

# PL Switching Characteristics

## IOB Pad Input/Output/3-State

Table 52 summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard), and 3-state delays.

- $T_{IOPI}$ is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.
- $T_{IOOP}$ is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.
- $T_{IOTP}$ is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer. In HR I/O banks, the IN_TERM termination turn-on time is always faster than $T_{IOTP}$ when the INTERMDISABLE pin is used.

*Table 52:* **IOB High Range (HR) Switching Characteristics**

| I/O Standard | $T_{IOPI}$ | | | | $T_{IOOP}$ | | | | $T_{IOTP}$ | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Speed Grade | | | | Speed Grade | | | | Speed Grade | | | | |
| | -3 | -2 | -1C/-1I/ -1LI | -1Q | -3 | -2 | -1C/-1I/ -1LI | -1Q | -3 | -2 | -1C/-1I/ -1LI | -1Q | |
| LVTTL_S4 | 1.26 | 1.34 | 1.41 | 1.53 | 3.80 | 3.93 | 4.18 | 4.18 | 3.82 | 3.96 | 4.20 | 4.20 | ns |
| LVTTL_S8 | 1.26 | 1.34 | 1.41 | 1.53 | 3.54 | 3.66 | 3.92 | 3.92 | 3.56 | 3.69 | 3.93 | 3.93 | ns |
| LVTTL_S12 | 1.26 | 1.34 | 1.41 | 1.53 | 3.52 | 3.65 | 3.90 | 3.90 | 3.54 | 3.68 | 3.91 | 3.91 | ns |
| LVTTL_S16 | 1.26 | 1.34 | 1.41 | 1.53 | 3.07 | 3.19 | 3.45 | 3.45 | 3.09 | 3.22 | 3.46 | 3.46 | ns |
| LVTTL_S24 | 1.26 | 1.34 | 1.41 | 1.53 | 3.29 | 3.41 | 3.67 | 3.67 | 3.31 | 3.44 | 3.68 | 3.68 | ns |
| LVTTL_F4 | 1.26 | 1.34 | 1.41 | 1.53 | 3.26 | 3.38 | 3.64 | 3.64 | 3.28 | 3.41 | 3.65 | 3.65 | ns |
| LVTTL_F8 | 1.26 | 1.34 | 1.41 | 1.53 | 2.74 | 2.87 | 3.12 | 3.12 | 2.76 | 2.90 | 3.13 | 3.13 | ns |
| LVTTL_F12 | 1.26 | 1.34 | 1.41 | 1.53 | 2.73 | 2.85 | 3.10 | 3.10 | 2.74 | 2.88 | 3.12 | 3.12 | ns |
| LVTTL_F16 | 1.26 | 1.34 | 1.41 | 1.53 | 2.56 | 2.68 | 2.93 | 2.93 | 2.57 | 2.71 | 2.95 | 2.95 | ns |
| LVTTL_F24 | 1.26 | 1.34 | 1.41 | 1.53 | 2.52 | 2.65 | 2.90 | 3.23 | 2.54 | 2.68 | 2.91 | 3.24 | ns |
| LVDS_25 | 0.73 | 0.81 | 0.88 | 0.89 | 1.29 | 1.41 | 1.67 | 1.67 | 1.31 | 1.44 | 1.68 | 1.68 | ns |
| MINI_LVDS_25 | 0.73 | 0.81 | 0.88 | 0.89 | 1.27 | 1.40 | 1.65 | 1.65 | 1.29 | 1.43 | 1.66 | 1.66 | ns |
| BLVDS_25 | 0.73 | 0.81 | 0.88 | 0.88 | 1.84 | 1.96 | 2.21 | 2.76 | 1.85 | 1.99 | 2.23 | 2.77 | ns |
| RSDS_25 (point to point) | 0.73 | 0.81 | 0.88 | 0.89 | 1.27 | 1.40 | 1.65 | 1.65 | 1.29 | 1.43 | 1.66 | 1.66 | ns |
| PPDS_25 | 0.73 | 0.81 | 0.88 | 0.89 | 1.29 | 1.41 | 1.67 | 1.67 | 1.31 | 1.44 | 1.68 | 1.68 | ns |
| TMDS_33 | 0.73 | 0.81 | 0.88 | 0.92 | 1.41 | 1.54 | 1.79 | 1.79 | 1.43 | 1.57 | 1.80 | 1.80 | ns |
| PCI33_3 | 1.24 | 1.32 | 1.39 | 1.52 | 3.10 | 3.22 | 3.48 | 3.48 | 3.12 | 3.25 | 3.49 | 3.49 | ns |
| HSUL_12_S | 0.67 | 0.75 | 0.82 | 0.88 | 1.81 | 1.93 | 2.18 | 2.18 | 1.82 | 1.96 | 2.20 | 2.20 | ns |
| HSUL_12_F | 0.67 | 0.75 | 0.82 | 0.88 | 1.29 | 1.41 | 1.67 | 1.67 | 1.31 | 1.44 | 1.68 | 1.68 | ns |
| DIFF_HSUL_12_S | 0.68 | 0.76 | 0.83 | 0.86 | 1.81 | 1.93 | 2.18 | 2.18 | 1.82 | 1.96 | 2.20 | 2.20 | ns |
| DIFF_HSUL_12_F | 0.68 | 0.76 | 0.83 | 0.86 | 1.29 | 1.41 | 1.67 | 1.67 | 1.31 | 1.44 | 1.68 | 1.68 | ns |
| MOBILE_DDR_S | 0.76 | 0.84 | 0.91 | 0.91 | 1.68 | 1.80 | 2.06 | 2.06 | 1.70 | 1.83 | 2.07 | 2.07 | ns |
| MOBILE_DDR_F | 0.76 | 0.84 | 0.91 | 0.91 | 1.38 | 1.51 | 1.76 | 1.76 | 1.40 | 1.54 | 1.77 | 1.77 | ns |
| DIFF_MOBILE_DDR_S | 0.70 | 0.78 | 0.85 | 0.85 | 1.70 | 1.82 | 2.07 | 2.07 | 1.71 | 1.85 | 2.09 | 2.09 | ns |
| DIFF_MOBILE_DDR_F | 0.70 | 0.78 | 0.85 | 0.85 | 1.45 | 1.57 | 1.82 | 1.82 | 1.46 | 1.60 | 1.84 | 1.84 | ns |
| HSTL_I_S | 0.67 | 0.75 | 0.82 | 0.86 | 1.62 | 1.74 | 1.99 | 1.99 | 1.63 | 1.77 | 2.01 | 2.01 | ns |
| HSTL_II_S | 0.65 | 0.73 | 0.80 | 0.86 | 1.41 | 1.54 | 1.79 | 1.79 | 1.43 | 1.57 | 1.80 | 1.81 | ns |

*Table 52:* **IOB High Range (HR) Switching Characteristics *(Cont'd)***

| I/O Standard | $T_{IOPI}$ | | | | $T_{IOOP}$ | | | | $T_{IOTP}$ | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Speed Grade | | | | Speed Grade | | | | Speed Grade | | | | |
| | -3 | -2 | -1C/-1I/ -1LI | -1Q | -3 | -2 | -1C/-1I/ -1LI | -1Q | -3 | -2 | -1C/-1I/ -1LI | -1Q | |
| HSTL_I_18_S | 0.67 | 0.75 | 0.82 | 0.88 | 1.29 | 1.41 | 1.67 | 1.67 | 1.31 | 1.44 | 1.68 | 1.68 | ns |
| HSTL_II_18_S | 0.66 | 0.75 | 0.81 | 0.88 | 1.41 | 1.54 | 1.79 | 1.79 | 1.43 | 1.57 | 1.80 | 1.80 | ns |
| DIFF_HSTL_I_S | 0.68 | 0.76 | 0.83 | 0.86 | 1.59 | 1.71 | 1.96 | 1.96 | 1.60 | 1.74 | 1.98 | 1.98 | ns |
| DIFF_HSTL_II_S | 0.68 | 0.76 | 0.83 | 0.86 | 1.51 | 1.63 | 1.88 | 1.88 | 1.52 | 1.66 | 1.90 | 1.90 | ns |
| DIFF_HSTL_I_18_S | 0.71 | 0.79 | 0.86 | 0.86 | 1.38 | 1.51 | 1.76 | 1.76 | 1.40 | 1.54 | 1.77 | 1.77 | ns |
| DIFF_HSTL_II_18_S | 0.70 | 0.78 | 0.85 | 0.88 | 1.46 | 1.58 | 1.84 | 1.84 | 1.48 | 1.61 | 1.85 | 1.85 | ns |
| HSTL_I_F | 0.67 | 0.75 | 0.82 | 0.86 | 1.10 | 1.22 | 1.48 | 1.49 | 1.12 | 1.25 | 1.49 | 1.51 | ns |
| HSTL_II_F | 0.65 | 0.73 | 0.80 | 0.86 | 1.12 | 1.24 | 1.49 | 1.49 | 1.13 | 1.27 | 1.51 | 1.51 | ns |
| HSTL_I_18_F | 0.67 | 0.75 | 0.82 | 0.88 | 1.13 | 1.26 | 1.51 | 1.54 | 1.15 | 1.29 | 1.52 | 1.56 | ns |
| HSTL_II_18_F | 0.66 | 0.75 | 0.81 | 0.88 | 1.12 | 1.24 | 1.49 | 1.51 | 1.13 | 1.27 | 1.51 | 1.52 | ns |
| DIFF_HSTL_I_F | 0.68 | 0.76 | 0.83 | 0.86 | 1.18 | 1.30 | 1.56 | 1.56 | 1.20 | 1.33 | 1.57 | 1.57 | ns |
| DIFF_HSTL_II_F | 0.68 | 0.76 | 0.83 | 0.86 | 1.21 | 1.33 | 1.59 | 1.59 | 1.23 | 1.36 | 1.60 | 1.60 | ns |
| DIFF_HSTL_I_18_F | 0.71 | 0.79 | 0.86 | 0.86 | 1.21 | 1.33 | 1.59 | 1.59 | 1.23 | 1.36 | 1.60 | 1.60 | ns |
| DIFF_HSTL_II_18_F | 0.70 | 0.78 | 0.85 | 0.88 | 1.21 | 1.33 | 1.59 | 1.59 | 1.23 | 1.36 | 1.60 | 1.60 | ns |
| LVCMOS33_S4 | 1.26 | 1.34 | 1.41 | 1.52 | 3.80 | 3.93 | 4.18 | 4.18 | 3.82 | 3.96 | 4.20 | 4.20 | ns |
| LVCMOS33_S8 | 1.26 | 1.34 | 1.41 | 1.52 | 3.52 | 3.65 | 3.90 | 3.90 | 3.54 | 3.68 | 3.91 | 3.91 | ns |
| LVCMOS33_S12 | 1.26 | 1.34 | 1.41 | 1.52 | 3.09 | 3.21 | 3.46 | 3.46 | 3.10 | 3.24 | 3.48 | 3.48 | ns |
| LVCMOS33_S16 | 1.26 | 1.34 | 1.41 | 1.52 | 3.40 | 3.52 | 3.77 | 3.78 | 3.42 | 3.55 | 3.79 | 3.79 | ns |
| LVCMOS33_F4 | 1.26 | 1.34 | 1.41 | 1.52 | 3.26 | 3.38 | 3.64 | 3.64 | 3.28 | 3.41 | 3.65 | 3.65 | ns |
| LVCMOS33_F8 | 1.26 | 1.34 | 1.41 | 1.52 | 2.74 | 2.87 | 3.12 | 3.12 | 2.76 | 2.90 | 3.13 | 3.13 | ns |
| LVCMOS33_F12 | 1.26 | 1.34 | 1.41 | 1.52 | 2.56 | 2.68 | 2.93 | 2.93 | 2.57 | 2.71 | 2.95 | 2.95 | ns |
| LVCMOS33_F16 | 1.26 | 1.34 | 1.41 | 1.52 | 2.56 | 2.68 | 2.93 | 3.06 | 2.57 | 2.71 | 2.95 | 3.07 | ns |
| LVCMOS25_S4 | 1.12 | 1.20 | 1.27 | 1.38 | 3.13 | 3.26 | 3.51 | 3.51 | 3.15 | 3.29 | 3.52 | 3.52 | ns |
| LVCMOS25_S8 | 1.12 | 1.20 | 1.27 | 1.38 | 2.88 | 3.01 | 3.26 | 3.26 | 2.90 | 3.04 | 3.27 | 3.27 | ns |
| LVCMOS25_S12 | 1.12 | 1.20 | 1.27 | 1.38 | 2.48 | 2.60 | 2.85 | 2.85 | 2.49 | 2.63 | 2.87 | 2.87 | ns |
| LVCMOS25_S16 | 1.12 | 1.20 | 1.27 | 1.38 | 2.82 | 2.94 | 3.20 | 3.20 | 2.84 | 2.97 | 3.21 | 3.21 | ns |
| LVCMOS25_F4 | 1.12 | 1.20 | 1.27 | 1.38 | 2.74 | 2.87 | 3.12 | 3.12 | 2.76 | 2.90 | 3.13 | 3.13 | ns |
| LVCMOS25_F8 | 1.12 | 1.20 | 1.27 | 1.38 | 2.18 | 2.30 | 2.56 | 2.56 | 2.20 | 2.33 | 2.57 | 2.57 | ns |
| LVCMOS25_F12 | 1.12 | 1.20 | 1.27 | 1.38 | 2.16 | 2.29 | 2.54 | 2.54 | 2.18 | 2.32 | 2.55 | 2.56 | ns |
| LVCMOS25_F16 | 1.12 | 1.20 | 1.27 | 1.38 | 2.01 | 2.13 | 2.39 | 2.63 | 2.03 | 2.16 | 2.40 | 2.65 | ns |
| LVCMOS18_S4 | 0.74 | 0.83 | 0.89 | 0.97 | 1.62 | 1.74 | 1.99 | 1.99 | 1.63 | 1.77 | 2.01 | 2.01 | ns |
| LVCMOS18_S8 | 0.74 | 0.83 | 0.89 | 0.97 | 2.18 | 2.30 | 2.56 | 2.56 | 2.20 | 2.33 | 2.57 | 2.57 | ns |
| LVCMOS18_S12 | 0.74 | 0.83 | 0.89 | 0.97 | 2.18 | 2.30 | 2.56 | 2.56 | 2.20 | 2.33 | 2.57 | 2.57 | ns |
| LVCMOS18_S16 | 0.74 | 0.83 | 0.89 | 0.97 | 1.52 | 1.65 | 1.90 | 1.90 | 1.54 | 1.68 | 1.91 | 1.91 | ns |
| LVCMOS18_S24 | 0.74 | 0.83 | 0.89 | 0.97 | 1.60 | 1.72 | 1.98 | 2.40 | 1.62 | 1.75 | 1.99 | 2.41 | ns |
| LVCMOS18_F4 | 0.74 | 0.83 | 0.89 | 0.97 | 1.45 | 1.57 | 1.82 | 1.82 | 1.46 | 1.60 | 1.84 | 1.84 | ns |
| LVCMOS18_F8 | 0.74 | 0.83 | 0.89 | 0.97 | 1.68 | 1.80 | 2.06 | 2.06 | 1.70 | 1.83 | 2.07 | 2.07 | ns |
| LVCMOS18_F12 | 0.74 | 0.83 | 0.89 | 0.97 | 1.68 | 1.80 | 2.06 | 2.06 | 1.70 | 1.83 | 2.07 | 2.07 | ns |
| LVCMOS18_F16 | 0.74 | 0.83 | 0.89 | 0.97 | 1.40 | 1.52 | 1.77 | 1.78 | 1.42 | 1.55 | 1.79 | 1.79 | ns |

*Table 52:* **IOB High Range (HR) Switching Characteristics *(Cont'd)***

| I/O Standard | $T_{IOPI}$ | | | | $T_{IOOP}$ | | | | $T_{IOTP}$ | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Speed Grade | | | | Speed Grade | | | | Speed Grade | | | | |
| | -3 | -2 | -1C/-1I/-1LI | -1Q | -3 | -2 | -1C/-1I/-1LI | -1Q | -3 | -2 | -1C/-1I/-1LI | -1Q | |
| LVCMOS18_F24 | 0.74 | 0.83 | 0.89 | 0.97 | 1.34 | 1.46 | 1.71 | 2.28 | 1.35 | 1.49 | 1.73 | 2.29 | ns |
| LVCMOS15_S4 | 0.77 | 0.86 | 0.93 | 0.96 | 2.05 | 2.18 | 2.43 | 2.43 | 2.07 | 2.21 | 2.45 | 2.45 | ns |
| LVCMOS15_S8 | 0.77 | 0.86 | 0.93 | 0.96 | 2.09 | 2.21 | 2.46 | 2.46 | 2.10 | 2.24 | 2.48 | 2.48 | ns |
| LVCMOS15_S12 | 0.77 | 0.86 | 0.93 | 0.96 | 1.59 | 1.71 | 1.96 | 1.96 | 1.60 | 1.74 | 1.98 | 1.98 | ns |
| LVCMOS15_S16 | 0.77 | 0.86 | 0.93 | 0.96 | 1.59 | 1.71 | 1.96 | 1.96 | 1.60 | 1.74 | 1.98 | 1.98 | ns |
| LVCMOS15_F4 | 0.77 | 0.86 | 0.93 | 0.96 | 1.85 | 1.97 | 2.23 | 2.23 | 1.87 | 2.00 | 2.24 | 2.24 | ns |
| LVCMOS15_F8 | 0.77 | 0.86 | 0.93 | 0.96 | 1.60 | 1.72 | 1.98 | 1.98 | 1.62 | 1.75 | 1.99 | 1.99 | ns |
| LVCMOS15_F12 | 0.77 | 0.86 | 0.93 | 0.96 | 1.35 | 1.47 | 1.73 | 1.73 | 1.37 | 1.50 | 1.74 | 1.74 | ns |
| LVCMOS15_F16 | 0.77 | 0.86 | 0.93 | 0.96 | 1.34 | 1.46 | 1.71 | 2.07 | 1.35 | 1.49 | 1.73 | 2.09 | ns |
| LVCMOS12_S4 | 0.87 | 0.95 | 1.02 | 1.19 | 2.57 | 2.69 | 2.95 | 2.95 | 2.59 | 2.72 | 2.96 | 2.96 | ns |
| LVCMOS12_S8 | 0.87 | 0.95 | 1.02 | 1.19 | 2.09 | 2.21 | 2.46 | 2.46 | 2.10 | 2.24 | 2.48 | 2.48 | ns |
| LVCMOS12_S12 | 0.87 | 0.95 | 1.02 | 1.19 | 1.79 | 1.91 | 2.17 | 2.17 | 1.81 | 1.94 | 2.18 | 2.18 | ns |
| LVCMOS12_F4 | 0.87 | 0.95 | 1.02 | 1.19 | 1.98 | 2.10 | 2.35 | 2.35 | 1.99 | 2.13 | 2.37 | 2.37 | ns |
| LVCMOS12_F8 | 0.87 | 0.95 | 1.02 | 1.19 | 1.54 | 1.66 | 1.92 | 1.92 | 1.56 | 1.69 | 1.93 | 1.93 | ns |
| LVCMOS12_F12 | 0.87 | 0.95 | 1.02 | 1.19 | 1.38 | 1.51 | 1.76 | 1.76 | 1.40 | 1.54 | 1.77 | 1.77 | ns |
| SSTL135_S | 0.67 | 0.75 | 0.82 | 0.88 | 1.35 | 1.47 | 1.73 | 1.73 | 1.37 | 1.50 | 1.74 | 1.74 | ns |
| SSTL15_S | 0.60 | 0.68 | 0.75 | 0.75 | 1.30 | 1.43 | 1.68 | 1.71 | 1.32 | 1.46 | 1.69 | 1.73 | ns |
| SSTL18_I_S | 0.67 | 0.75 | 0.82 | 0.86 | 1.67 | 1.79 | 2.04 | 2.04 | 1.68 | 1.82 | 2.06 | 2.06 | ns |
| SSTL18_II_S | 0.67 | 0.75 | 0.82 | 0.88 | 1.31 | 1.43 | 1.68 | 1.68 | 1.32 | 1.46 | 1.70 | 1.70 | ns |
| DIFF_SSTL135_S | 0.68 | 0.76 | 0.83 | 0.88 | 1.35 | 1.47 | 1.73 | 1.73 | 1.37 | 1.50 | 1.74 | 1.74 | ns |
| DIFF_SSTL15_S | 0.68 | 0.76 | 0.83 | 0.88 | 1.30 | 1.43 | 1.68 | 1.71 | 1.32 | 1.46 | 1.69 | 1.73 | ns |
| DIFF_SSTL18_I_S | 0.71 | 0.79 | 0.86 | 0.88 | 1.68 | 1.80 | 2.06 | 2.06 | 1.70 | 1.83 | 2.07 | 2.07 | ns |
| DIFF_SSTL18_II_S | 0.71 | 0.79 | 0.86 | 0.88 | 1.38 | 1.51 | 1.76 | 1.76 | 1.40 | 1.54 | 1.77 | 1.77 | ns |
| SSTL135_F | 0.67 | 0.75 | 0.82 | 0.88 | 1.12 | 1.24 | 1.49 | 1.49 | 1.13 | 1.27 | 1.51 | 1.51 | ns |
| SSTL15_F | 0.60 | 0.68 | 0.75 | 0.75 | 1.07 | 1.19 | 1.45 | 1.45 | 1.09 | 1.22 | 1.46 | 1.46 | ns |
| SSTL18_I_F | 0.67 | 0.75 | 0.82 | 0.86 | 1.12 | 1.24 | 1.49 | 1.53 | 1.13 | 1.27 | 1.51 | 1.54 | ns |
| SSTL18_II_F | 0.67 | 0.75 | 0.82 | 0.88 | 1.12 | 1.24 | 1.49 | 1.51 | 1.13 | 1.27 | 1.51 | 1.52 | ns |
| DIFF_SSTL135_F | 0.68 | 0.76 | 0.83 | 0.88 | 1.12 | 1.24 | 1.49 | 1.49 | 1.13 | 1.27 | 1.51 | 1.51 | ns |
| DIFF_SSTL15_F | 0.68 | 0.76 | 0.83 | 0.88 | 1.07 | 1.19 | 1.45 | 1.45 | 1.09 | 1.22 | 1.46 | 1.46 | ns |
| DIFF_SSTL18_I_F | 0.71 | 0.79 | 0.86 | 0.88 | 1.23 | 1.35 | 1.60 | 1.60 | 1.24 | 1.38 | 1.62 | 1.62 | ns |
| DIFF_SSTL18_II_F | 0.71 | 0.79 | 0.86 | 0.88 | 1.21 | 1.33 | 1.59 | 1.59 | 1.23 | 1.36 | 1.60 | 1.60 | ns |

Table 53 specifies the values of $T_{IOTPHZ}$ and $T_{IOIBUFDISABLE}$. $T_{IOTPHZ}$ is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state). $T_{IOIBUFDISABLE}$ is described as the IOB delay from IBUFDISABLE to O output. In HR I/O banks, the internal IN_TERM termination turn-off time is always faster than $T_{IOTPHZ}$ when the INTERMDISABLE pin is used.

*Table 53:* **IOB 3-state Output Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1C/-1I/-1LI | -1Q | |
| $T_{IOTPHZ}$ | T input to pad high-impedance | 2.06 | 2.19 | 2.37 | 2.37 | ns |
| $T_{IOIBUFDISABLE}$ | IBUF turn-on time from IBUFDISABLE to O output | 2.11 | 2.30 | 2.60 | 2.60 | ns |

## I/O Standard Adjustment Measurement Methodology

### Input Delay Measurements

Table 54 shows the test setup parameters used for measuring input delay.

*Table 54:* **Input Delay Measurement Methodology**

| Description | I/O Standard Attribute | $V_L$ (1)(2) | $V_H$ (1)(2) | $V_{MEAS}$ (1)(4)(6) | $V_{REF}$ (1)(3)(5) |
|---|---|---|---|---|---|
| LVCMOS, 1.2V | LVCMOS12 | 0.1 | 1.1 | 0.6 | – |
| LVCMOS, 1.5V | LVCMOS15 | 0.1 | 1.4 | 0.75 | – |
| LVCMOS, 1.8V | LVCMOS18 | 0.1 | 1.7 | 0.9 | – |
| LVCMOS, 2.5V | LVCMOS25 | 0.1 | 2.4 | 1.25 | – |
| LVCMOS, 3.3V | LVCMOS33 | 0.1 | 3.2 | 1.65 | – |
| LVTTL, 3.3V | LVTTL | 0.1 | 3.2 | 1.65 | – |
| MOBILE_DDR, 1.8V | MOBILE_DDR | 0.1 | 1.7 | 0.9 | – |
| PCI33, 3.3V | PCI33_3 | 0.1 | 3.2 | 1.65 | – |
| HSTL (High-Speed Transceiver Logic), Class I, 1.2V | HSTL_I_12 | $V_{REF}$ – 0.5 | $V_{REF}$ + 0.5 | $V_{REF}$ | 0.60 |
| HSTL, Class I & II, 1.5V | HSTL_I, HSTL_II | $V_{REF}$ – 0.65 | $V_{REF}$ + 0.65 | $V_{REF}$ | 0.75 |
| HSTL, Class I & II, 1.8V | HSTL_I_18, HSTL_II_18 | $V_{REF}$ – 0.8 | $V_{REF}$ + 0.8 | $V_{REF}$ | 0.90 |
| HSUL (High-Speed Unterminated Logic), 1.2V | HSUL_12 | $V_{REF}$ – 0.5 | $V_{REF}$ + 0.5 | $V_{REF}$ | 0.60 |
| SSTL (Stub Terminated Transceiver Logic), 1.2V | SSTL12 | $V_{REF}$ – 0.5 | $V_{REF}$ + 0.5 | $V_{REF}$ | 0.60 |
| SSTL, 1.35V | SSTL135, SSTL135_R | $V_{REF}$ – 0.575 | $V_{REF}$ + 0.575 | $V_{REF}$ | 0.675 |
| SSTL, 1.5V | SSTL15, SSTL15_R | $V_{REF}$ – 0.65 | $V_{REF}$ + 0.65 | $V_{REF}$ | 0.75 |
| SSTL, Class I & II, 1.8V | SSTL18_I, SSTL18_II | $V_{REF}$ – 0.8 | $V_{REF}$ + 0.8 | $V_{REF}$ | 0.90 |
| DIFF_MOBILE_DDR, 1.8V | DIFF_MOBILE_DDR | 0.9 – 0.125 | 0.9 + 0.125 | 0 (6) | – |
| DIFF_HSTL, Class I, 1.2V | DIFF_HSTL_I_12 | 0.6 – 0.125 | 0.6 + 0.125 | 0 (6) | – |
| DIFF_HSTL, Class I & II,1.5V | DIFF_HSTL_I, DIFF_HSTL_II | 0.75 – 0.125 | 0.75 + 0.125 | 0 (6) | – |
| DIFF_HSTL, Class I & II, 1.8V | DIFF_HSTL_I_18, DIFF_HSTL_II_18 | 0.9 – 0.125 | 0.9 + 0.125 | 0 (6) | – |
| DIFF_HSUL, 1.2V | DIFF_HSUL_12 | 0.6 – 0.125 | 0.6 + 0.125 | 0 (6) | – |
| DIFF_SSTL, 1.2V | DIFF_SSTL12 | 0.6 – 0.125 | 0.6 + 0.125 | 0 (6) | – |
| DIFF_SSTL135/DIFF_SSTL135_R, 1.35V | DIFF_SSTL135, DIFF_SSTL135_R | 0.675 – 0.125 | 0.675 + 0.125 | 0 (6) | – |
| DIFF_SSTL15/DIFF_SSTL15_R, 1.5V | DIFF_SSTL15, DIFF_SSTL15_R | 0.75 – 0.125 | 0.75 + 0.125 | 0 (6) | – |
| DIFF_SSTL18_I/DIFF_SSTL18_II, 1.8V | DIFF_SSTL18_I, DIFF_SSTL18_II | 0.9 – 0.125 | 0.9 + 0.125 | 0 (6) | – |
| LVDS (Low-Voltage Differential Signaling), 1.8V | LVDS | 0.9 – 0.125 | 0.9 + 0.125 | 0 (6) | – |

*Table 54:* **Input Delay Measurement Methodology *(Cont'd)***

| Description | I/O Standard Attribute | $V_L$ (1)(2) | $V_H$ (1)(2) | $V_{MEAS}$ (1)(4)(6) | $V_{REF}$ (1)(3)(5) |
|---|---|---|---|---|---|
| LVDS_25, 2.5V | LVDS_25 | 1.2 – 0.125 | 1.2 + 0.125 | 0(6) | – |
| BLVDS_25, 2.5V | BLVDS_25 | 1.25 – 0.125 | 1.25 + 0.125 | 0(6) | – |
| MINI_LVDS_25, 2.5V | MINI_LVDS_25 | 1.25 – 0.125 | 1.25 + 0.125 | 0(6) | – |
| PPDS_25 | PPDS_25 | 1.25 – 0.125 | 1.25 + 0.125 | 0(6) | – |
| RSDS_25 | RSDS_25 | 1.25 – 0.125 | 1.25 + 0.125 | 0(6) | – |
| TMDS_33 | TMDS_33 | 3 – 0.125 | 3 + 0.125 | 0(6) | – |

**Notes:**

1. The input delay measurement methodology parameters for LVDCI are the same for LVCMOS standards of the same voltage. Input delay measurement methodology parameters for HSLVDCI are the same as for HSTL_II standards of the same voltage. Parameters for all other DCI standards are the same for the corresponding non-DCI standards.
2. Input waveform switches between $V_L$ and $V_H$.
3. Measurements are made at typical, minimum, and maximum $V_{REF}$ values. Reported delays reflect worst case of these measurements. $V_{REF}$ values listed are typical.
4. Input voltage level from which measurement starts.
5. This is an input voltage reference that bears no relation to the $V_{REF}$ / $V_{MEAS}$ parameters found in IBIS models and/or noted in Figure 18.
6. The value given is the differential input voltage.

### Output Delay Measurements

Output delays are measured with short output traces. Standard termination was used for all testing. The propagation delay of the trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setups shown in Figure 18 and Figure 19.

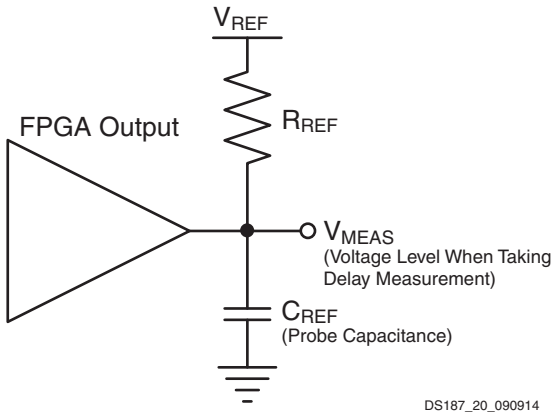


*Figure 18:* **Single-Ended Test Setup**

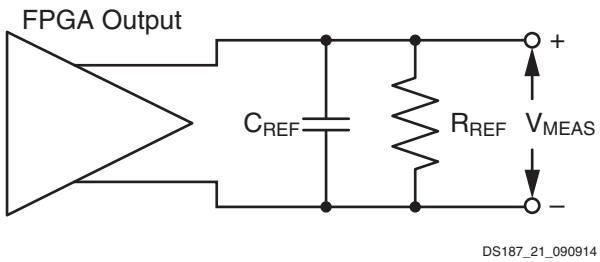


*Figure 19:* **Differential Test Setup**

Parameters $V_{REF}$, $R_{REF}$, $C_{REF}$, and $V_{MEAS}$ fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using this method:

1. Simulate the output driver of choice into the generalized test setup using values from Table 55.
2. Record the time to $V_{MEAS}$.
3. Simulate the output driver of choice into the actual PCB trace and load using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to $V_{MEAS}$.
5. Compare the results of step 2 and step 4. The increase or decrease in delay yields the actual propagation delay of the PCB trace.

*Table 55:* **Output Delay Measurement Methodology**

| Description | I/O Standard Attribute | $R_{REF}$ (Ω) | $C_{REF}$[1] (pF) | $V_{MEAS}$ (V) | $V_{REF}$ (V) |
|---|---|---|---|---|---|
| LVCMOS, 1.2V | LVCMOS12 | 1M | 0 | 0.6 | 0 |
| LVCMOS/LVDCI/HSLVDCI, 1.5V | LVCMOS15, LVDCI_15, HSLVDCI_15 | 1M | 0 | 0.75 | 0 |
| LVCMOS/LVDCI/HSLVDCI, 1.8V | LVCMOS18, LVDCI_15, HSLVDCI_18 | 1M | 0 | 0.9 | 0 |
| LVCMOS, 2.5V | LVCMOS25 | 1M | 0 | 1.25 | 0 |
| LVCMOS, 3.3V | LVCMOS33 | 1M | 0 | 1.65 | 0 |
| LVTTL, 3.3V | LVTTL | 1M | 0 | 1.65 | 0 |
| PCI33, 3.3V | PCI33_3 | 25 | 10 | 1.65 | 0 |
| HSTL (High-Speed Transceiver Logic), Class I, 1.2V | HSTL_I_12 | 50 | 0 | $V_{REF}$ | 0.6 |
| HSTL, Class I, 1.5V | HSTL_I | 50 | 0 | $V_{REF}$ | 0.75 |
| HSTL, Class II, 1.5V | HSTL_II | 25 | 0 | $V_{REF}$ | 0.75 |
| HSTL, Class I, 1.8V | HSTL_I_18 | 50 | 0 | $V_{REF}$ | 0.9 |
| HSTL, Class II, 1.8V | HSTL_II_18 | 25 | 0 | $V_{REF}$ | 0.9 |
| HSUL (High-Speed Unterminated Logic), 1.2V | HSUL_12 | 50 | 0 | $V_{REF}$ | 0.6 |
| SSTL12, 1.2V | SSTL12 | 50 | 0 | $V_{REF}$ | 0.6 |
| SSTL135/SSTL135_R, 1.35V | SSTL135, SSTL135_R | 50 | 0 | $V_{REF}$ | 0.675 |
| SSTL15/SSTL15_R, 1.5V | SSTL15, SSTL15_R | 50 | 0 | $V_{REF}$ | 0.75 |
| SSTL (Stub Series Terminated Logic), Class I & Class II, 1.8V | SSTL18_I, SSTL18_II | 50 | 0 | $V_{REF}$ | 0.9 |
| DIFF_MOBILE_DDR, 1.8V | DIFF_MOBILE_DDR | 50 | 0 | $V_{REF}$ | 0.9 |
| DIFF_HSTL, Class I, 1.2V | DIFF_HSTL_I_12 | 50 | 0 | $V_{REF}$ | 0.6 |
| DIFF_HSTL, Class I & II, 1.5V | DIFF_HSTL_I, DIFF_HSTL_II | 50 | 0 | $V_{REF}$ | 0.75 |
| DIFF_HSTL, Class I & II, 1.8V | DIFF_HSTL_I_18, DIFF_HSTL_II_18 | 50 | 0 | $V_{REF}$ | 0.9 |
| DIFF_HSUL_12, 1.2V | DIFF_HSUL_12 | 50 | 0 | $V_{REF}$ | 0.6 |
| DIFF_SSTL12, 1.2V | DIFF_SSTL12 | 50 | 0 | $V_{REF}$ | 0.6 |
| DIFF_SSTL135/DIFF_SSTL135_R, 1.35V | DIFF_SSTL135, DIFF_SSTL135_R | 50 | 0 | $V_{REF}$ | 0.675 |
| DIFF_SSTL15/DIFF_SSTL15_R, 1.5V | DIFF_SSTL15, DIFF_SSTL15_R | 50 | 0 | $V_{REF}$ | 0.75 |
| DIFF_SSTL18, Class I & II, 1.8V | DIFF_SSTL18_I, DIFF_SSTL18_II | 50 | 0 | $V_{REF}$ | 0.9 |
| LVDS (Low-Voltage Differential Signaling), 1.8V | LVDS | 100 | 0 | 0[2] | 0 |
| LVDS, 2.5V | LVDS_25 | 100 | 0 | 0[2] | 0 |
| BLVDS (Bus LVDS), 2.5V | BLVDS_25 | 100 | 0 | 0[2] | 0 |
| Mini LVDS, 2.5V | MINI_LVDS_25 | 100 | 0 | 0[2] | 0 |
| PPDS_25 | PPDS_25 | 100 | 0 | 0[2] | 0 |

*Table 55:* **Output Delay Measurement Methodology *(Cont'd)***

| Description | I/O Standard Attribute | $R_{REF}$ (Ω) | $C_{REF}$[1] (pF) | $V_{MEAS}$ (V) | $V_{REF}$ (V) |
|---|---|---|---|---|---|
| RSDS_25 | RSDS_25 | 100 | 0 | 0[2] | 0 |
| TMDS_33 | TMDS_33 | 50 | 0 | 0[2] | 3.3 |

**Notes:**

1. $C_{REF}$ is the capacitance of the probe, nominally 0 pF.
2. The value given is the differential output voltage.

## Input/Output Logic Switching Characteristics

*Table 56:* **ILOGIC Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1C/-1I/-1LI | -1Q | |
| **Setup/Hold** | | | | | | |
| $T_{ICE1CK}$/ $T_{ICKCE1}$ | CE1 pin setup/hold with respect to CLK | 0.48/0.02 | 0.54/0.02 | 0.76/0.02 | 0.76/0.02 | ns |
| $T_{ISRCK}$/ $T_{ICKSR}$ | SR pin setup/hold with respect to CLK | 0.60/0.01 | 0.70/0.01 | 1.13/0.01 | 1.13/0.01 | ns |
| $T_{IDOCK}$/ $T_{IOCKD}$ | D pin setup/hold with respect to CLK without Delay | 0.01/0.27 | 0.01/0.29 | 0.01/0.33 | 0.01/0.33 | ns |
| $T_{IDOCKD}$/ $T_{IOCKDD}$ | DDLY pin setup/hold with respect to CLK (using IDELAY) | 0.02/0.27 | 0.02/0.29 | 0.02/0.33 | 0.02/0.33 | ns |
| **Combinatorial** | | | | | | |
| $T_{IDI}$ | D pin to O pin propagation delay, no Delay | 0.11 | 0.11 | 0.13 | 0.13 | ns |
| $T_{IDID}$ | DDLY pin to O pin propagation delay (using IDELAY) | 0.11 | 0.12 | 0.14 | 0.14 | ns |
| **Sequential Delays** | | | | | | |
| $T_{IDLO}$ | D pin to Q1 pin using flip-flop as a latch without Delay | 0.41 | 0.44 | 0.51 | 0.51 | ns |
| $T_{IDLOD}$ | DDLY pin to Q1 pin using flip-flop as a latch (using IDELAY) | 0.41 | 0.44 | 0.51 | 0.51 | ns |
| $T_{ICKQ}$ | CLK to Q outputs | 0.53 | 0.57 | 0.66 | 0.66 | ns |
| $T_{RQ_ILOGIC}$ | SR pin to OQ/TQ out | 0.96 | 1.08 | 1.32 | 1.32 | ns |
| $T_{GSRQ_ILOGIC}$ | Global set/reset to Q outputs | 7.60 | 7.60 | 10.51 | 10.51 | ns |
| **Set/Reset** | | | | | | |
| $T_{RPW_ILOGIC}$ | Minimum pulse width, SR inputs | 0.61 | 0.72 | 0.72 | 0.72 | ns, Min |

*Table 57:* **OLOGIC Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1C/-1I/-1LI | -1Q | |
| **Setup/Hold** | | | | | | |
| $T_{ODCK}$/ $T_{OCKD}$ | D1/D2 pins setup/hold with respect to CLK | 0.67/–0.11 | 0.71/–0.11 | 0.84/–0.11 | 0.84/–0.06 | ns |
| $T_{OOCECK}$/ $T_{OCKOCE}$ | OCE pin setup/hold with respect to CLK | 0.32/0.58 | 0.34/0.58 | 0.51/0.58 | 0.51/0.58 | ns |
| $T_{OSRCK}$/ $T_{OCKSR}$ | SR pin setup/hold with respect to CLK | 0.37/0.21 | 0.44/0.21 | 0.80/0.21 | 0.80/0.21 | ns |
| $T_{OTCK}$/ $T_{OCKT}$ | T1/T2 pins setup/hold with respect to CLK | 0.69/–0.14 | 0.73/–0.14 | 0.89/–0.14 | 0.89/–0.11 | ns |

*Table 57:* **OLOGIC Switching Characteristics *(Cont'd)***

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1C/-1I/-1LI | -1Q | |
| $T_{OTCECK}$/ $T_{OCKTCE}$ | TCE pin setup/hold with respect to CLK | 0.32/0.01 | 0.34/0.01 | 0.51/0.01 | 0.51/0.01 | ns |
| **Combinatorial** | | | | | | |
| $T_{ODQ}$ | D1 to OQ out or T1 to TQ out | 0.83 | 0.96 | 1.16 | 1.16 | ns |
| **Sequential Delays** | | | | | | |
| $T_{OCKQ}$ | CLK to OQ/TQ out | 0.47 | 0.49 | 0.56 | 0.56 | ns |
| $T_{RQ_OLOGIC}$ | SR pin to OQ/TQ out | 0.72 | 0.80 | 0.95 | 0.95 | ns |
| $T_{GSRQ_OLOGIC}$ | Global set/reset to Q outputs | 7.60 | 7.60 | 10.51 | 10.51 | ns |
| **Set/Reset** | | | | | | |
| $T_{RPW_OLOGIC}$ | Minimum pulse width, SR inputs | 0.64 | 0.74 | 0.74 | 0.74 | ns, Min |

## Input Serializer/Deserializer Switching Characteristics

*Table 58:* **ISERDES Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1C/-1I/-1LI | -1Q | |
| **Setup/Hold for Control Lines** | | | | | | |
| $T_{ISCCK_BITSLIP}$/ $T_{ISCKC_BITSLIP}$ | BITSLIP pin setup/hold with respect to CLKDIV | 0.01/0.14 | 0.02/0.15 | 0.02/0.17 | 0.02/0.17 | ns |
| $T_{ISCCK_CE}$ / $T_{ISCKC_CE}$(2) | CE pin setup/hold with respect to CLK (for CE1) | 0.45/–0.01 | 0.50/–0.01 | 0.72/–0.01 | 0.72/–0.01 | ns |
| $T_{ISCCK_CE2}$ / $T_{ISCKC_CE2}$(2) | CE pin setup/hold with respect to CLKDIV (for CE2) | –0.10/0.33 | –0.10/0.36 | –0.10/0.40 | –0.10/0.40 | ns |
| **Setup/Hold for Data Lines** | | | | | | |
| $T_{ISDCK_D}$ /$T_{ISCKD_D}$ | D pin setup/hold with respect to CLK | –0.02/0.12 | –0.02/0.14 | –0.02/0.17 | –0.02/0.17 | ns |
| $T_{ISDCK_DDLY}$/ $T_{ISCKD_DDLY}$ | DDLY pin setup/hold with respect to CLK (using IDELAY)(1) | –0.02/0.12 | –0.02/0.14 | –0.02/0.17 | –0.02/0.17 | ns |
| $T_{ISDCK_D_DDR}$/ $T_{ISCKD_D_DDR}$ | D pin setup/hold with respect to CLK at DDR mode | –0.02/0.12 | –0.02/0.14 | –0.02/0.17 | –0.02/0.17 | ns |
| $T_{ISDCK_DDLY_DDR}$/ $T_{ISCKD_DDLY_DDR}$ | D pin setup/hold with respect to CLK at DDR mode (using IDELAY)(1) | 0.12/0.12 | 0.14/0.14 | 0.17/0.17 | 0.17/0.17 | ns |
| **Sequential Delays** | | | | | | |
| $T_{ISCKO_Q}$ | CLKDIV to out at Q pin | 0.53 | 0.54 | 0.66 | 0.66 | ns |
| **Propagation Delays** | | | | | | |
| $T_{ISDO_DO}$ | D input to DO output pin | 0.11 | 0.11 | 0.13 | 0.13 | ns |

**Notes:**

1. Recorded at 0 tap value.
2. $T_{ISCCK_CE2}$ and $T_{ISCKC_CE2}$ are reported as $T_{ISCCK_CE}$/$T_{ISCKC_CE}$ in the timing report.

## Output Serializer/Deserializer Switching Characteristics

*Table 59:* **OSERDES Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1C/-1I/-1LI | -1Q | |
| **Setup/Hold** | | | | | | |
| $T_{OSDCK_D}$/ $T_{OSCKD_D}$ | D input setup/hold with respect to CLKDIV | 0.42/0.03 | 0.45/0.03 | 0.63/0.03 | 0.63/0.08 | ns |
| $T_{OSDCK_T}$/ $T_{OSCKD_T}$(1) | T input setup/hold with respect to CLK | 0.69/–0.13 | 0.73/–0.13 | 0.88/–0.13 | 0.88/–0.13 | ns |
| $T_{OSDCK_T2}$/ $T_{OSCKD_T2}$(1) | T input setup/hold with respect to CLKDIV | 0.31/–0.13 | 0.34/–0.13 | 0.39/–0.13 | 0.39/–0.13 | ns |
| $T_{OSCCK_OCE}$/ $T_{OSCKC_OCE}$ | OCE input setup/hold with respect to CLK | 0.32/0.58 | 0.34/0.58 | 0.51/0.58 | 0.51/0.58 | ns |
| $T_{OSCCK_S}$ | SR (reset) input setup with respect to CLKDIV | 0.47 | 0.52 | 0.85 | 0.85 | ns |
| $T_{OSCCK_TCE}$/ $T_{OSCKC_TCE}$ | TCE input setup/hold with respect to CLK | 0.32/0.01 | 0.34/0.01 | 0.51/0.01 | 0.51/0.10 | ns |
| **Sequential Delays** | | | | | | |
| $T_{OSCKO_OQ}$ | Clock to out from CLK to OQ | 0.40 | 0.42 | 0.48 | 0.48 | ns |
| $T_{OSCKO_TQ}$ | Clock to out from CLK to TQ | 0.47 | 0.49 | 0.56 | 0.56 | ns |
| **Combinatorial** | | | | | | |
| $T_{OSDO_TTQ}$ | T input to TQ out | 0.83 | 0.92 | 1.11 | 1.11 | ns |

**Notes:**

1. $T_{OSDCK_T2}$ and $T_{OSCKD_T2}$ are reported as $T_{OSDCK_T}$/$T_{OSCKD_T}$ in the timing report.

## Input/Output Delay Switching Characteristics

*Table 60:* **Input Delay Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1C/-1I/-1LI | -1Q | |
| **IDELAYCTRL** | | | | | | |
| $T_{DLYCCO_RDY}$ | Reset to ready for IDELAYCTRL | 3.67 | 3.67 | 3.67 | 3.67 | µs |
| $F_{IDELAYCTRL_REF}$ | Attribute REFCLK frequency = 200.0(1) | 200 | 200 | 200 | 200 | MHz |
| | Attribute REFCLK frequency = 300.0(1) | 300 | 300 | N/A | N/A | MHz |
| | Attribute REFCLK frequency = 400.0(1) | 400 | 400 | N/A | N/A | MHz |
| IDELAYCTRL_ REF_PRECISION | REFCLK precision | ±10 | ±10 | ±10 | ±10 | MHz |
| $T_{IDELAYCTRL_RPW}$ | Minimum reset pulse width | 59.28 | 59.28 | 59.28 | 59.28 | ns |
| **IDELAY** | | | | | | |
| $T_{IDELAYRESOLUTION}$ | IDELAY chain delay resolution | 1/(32 x 2 x $F_{REF}$) | | | | µs |

*Table 60:* **Input Delay Switching Characteristics *(Cont'd)***

| Symbol | Description | | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | -3 | -2 | -1C/-1I/-1LI | -1Q | |
| $T_{IDELAYPAT_JIT}$ and $T_{ODELAYPAT_JIT}$ | Pattern dependent period jitter in delay chain for clock pattern.(2) | | 0 | 0 | 0 | 0 | ps per tap |
| | Pattern dependent period jitter in delay chain for random data pattern (PRBS 23)(3) | REFCLK 200 MHz | ±5 | ±5 | ±5 | ±5 | ps per tap |
| | | REFCLK 300 MHz | ±3.33 | ±3.33 | ±3.33 | N/A | ps per tap |
| | | REFCLK 400 MHz | ±2.50 | ±2.50 | N/A | N/A | ps per tap |
| | Pattern dependent period jitter in delay chain for random data pattern (PRBS 23)(4) | REFCLK 200 MHz | ±9.0 | ±9.0 | ±9.0 | ±9.0 | ps per tap |
| | | REFCLK 300 MHz | ±6.0 | ±6.0 | ±6.0 | N/A | ps per tap |
| | | REFCLK 400 MHz | ±4.5 | ±4.5 | N/A | N/A | ps per tap |
| $T_{IDELAY_CLK_MAX}$ | Maximum frequency of CLK input to IDELAY | | 680.00 | 680.00 | 600.00 | 600.00 | MHz |
| $T_{IDCCK_CE}$ / $T_{IDCKC_CE}$ | CE pin setup/hold with respect to C for IDELAY | | 0.12/0.11 | 0.16/0.13 | 0.21/0.16 | 0.21/0.16 | ns |
| $T_{IDCCK_INC}$/ $T_{IDCKC_INC}$ | INC pin setup/hold with respect to C for IDELAY | | 0.12/0.16 | 0.14/0.18 | 0.16/0.22 | 0.16/0.23 | ns |
| $T_{IDCCK_RST}$/ $T_{IDCKC_RST}$ | RST pin setup/hold with respect to C for IDELAY | | 0.15/0.09 | 0.16/0.11 | 0.18/0.14 | 0.18/0.14 | ns |
| $T_{IDDO_IDATAIN}$ | Propagation delay through IDELAY | | Note 5 | Note 5 | Note 5 | Note 5 | ps |

**Notes:**

1. Average tap delay at 200 MHz = 78 ps, at 300 MHz = 52 ps, and at 400 MHz = 39 ps.
2. When HIGH_PERFORMANCE mode is set to TRUE or FALSE.
3. When HIGH_PERFORMANCE mode is set to TRUE.
4. When HIGH_PERFORMANCE mode is set to FALSE.
5. Delay depends on IDELAY tap setting. See the timing report for actual values.

*Table 61:* **IO_FIFO Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1C/-1I/-1LI | -1Q | |
| **IO_FIFO Clock to Out Delays** | | | | | | |
| $T_{OFFCKO_DO}$ | RDCLK to Q outputs | 0.55 | 0.60 | 0.68 | 0.68 | ns |
| $T_{CKO_FLAGS}$ | Clock to IO_FIFO flags | 0.55 | 0.61 | 0.77 | 0.77 | ns |
| **Setup/Hold** | | | | | | |
| $T_{CCK_D}$/$T_{CKC_D}$ | D inputs to WRCLK | 0.47/0.02 | 0.51/0.02 | 0.58/0.02 | 0.58/0.18 | ns |
| $T_{IFFCCK_WREN}$ / $T_{IFFCKC_WREN}$ | WREN to WRCLK | 0.42/–0.01 | 0.47/–0.01 | 0.53/–0.01 | 0.53/–0.01 | ns |
| $T_{OFFCCK_RDEN}$/ $T_{OFFCKC_RDEN}$ | RDEN to RDCLK | 0.53/0.02 | 0.58/0.02 | 0.66/0.02 | 0.66/0.02 | ns |
| **Minimum Pulse Width** | | | | | | |
| $T_{PWH_IO_FIFO}$ | RESET, RDCLK, WRCLK | 1.62 | 2.15 | 2.15 | 2.15 | ns |
| $T_{PWL_IO_FIFO}$ | RESET, RDCLK, WRCLK | 1.62 | 2.15 | 2.15 | 2.15 | ns |
| **Maximum Frequency** | | | | | | |
| $F_{MAX}$ | RDCLK and WRCLK | 266.67 | 200.00 | 200.00 | 200.00 | MHz |

## CLB Switching Characteristics

*Table 62:* **CLB Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1C/-1I/-1LI | -1Q | |
| **Combinatorial Delays** | | | | | | |
| $T_{ILO}$ | An – Dn LUT address to A | 0.10 | 0.11 | 0.13 | 0.13 | ns, Max |
| $T_{ILO_2}$ | An – Dn LUT address to AMUX/CMUX | 0.27 | 0.30 | 0.36 | 0.36 | ns, Max |
| $T_{ILO_3}$ | An – Dn LUT address to BMUX_A | 0.42 | 0.46 | 0.55 | 0.55 | ns, Max |
| $T_{ITO}$ | An – Dn inputs to A – D Q outputs | 0.94 | 1.05 | 1.27 | 1.27 | ns, Max |
| $T_{AXA}$ | AX inputs to AMUX output | 0.62 | 0.69 | 0.84 | 0.84 | ns, Max |
| $T_{AXB}$ | AX inputs to BMUX output | 0.58 | 0.66 | 0.83 | 0.83 | ns, Max |
| $T_{AXC}$ | AX inputs to CMUX output | 0.60 | 0.68 | 0.82 | 0.82 | ns, Max |
| $T_{AXD}$ | AX inputs to DMUX output | 0.68 | 0.75 | 0.90 | 0.90 | ns, Max |
| $T_{BXB}$ | BX inputs to BMUX output | 0.51 | 0.57 | 0.69 | 0.69 | ns, Max |
| $T_{BXD}$ | BX inputs to DMUX output | 0.62 | 0.69 | 0.82 | 0.82 | ns, Max |
| $T_{CXC}$ | CX inputs to CMUX output | 0.42 | 0.48 | 0.58 | 0.58 | ns, Max |
| $T_{CXD}$ | CX inputs to DMUX output | 0.53 | 0.59 | 0.71 | 0.71 | ns, Max |
| $T_{DXD}$ | DX inputs to DMUX output | 0.52 | 0.58 | 0.70 | 0.70 | ns, Max |
| **Sequential Delays** | | | | | | |
| $T_{CKO}$ | Clock to AQ – DQ outputs | 0.40 | 0.44 | 0.53 | 0.53 | ns, Max |
| $T_{SHCKO}$ | Clock to AMUX – DMUX outputs | 0.47 | 0.53 | 0.66 | 0.66 | ns, Max |
| **Setup and Hold Times of CLB Flip-Flops Before/After Clock CLK** | | | | | | |
| $T_{AS}/T_{AH}$ | $A_N$ – $D_N$ input to CLK on A – D flip-flops | 0.07/0.12 | 0.09/0.14 | 0.11/0.18 | 0.11/0.28 | ns, Min |
| $T_{DICK}/T_{CKDI}$ | $A_X$ – $D_X$ input to CLK on A – D flip-flops | 0.06/0.19 | 0.07/0.21 | 0.09/0.26 | 0.09/0.35 | ns, Min |
| | $A_X$ – $D_X$ input through MUXs and/or carry logic to CLK on A – D flip-flops | 0.59/0.08 | 0.66/0.09 | 0.81/0.11 | 0.81/0.20 | ns, Min |
| $T_{CECK_CLB}/T_{CKCE_CLB}$ | CE input to CLK on A – D flip-flops | 0.15/0.00 | 0.17/0.00 | 0.21/0.01 | 0.21/0.13 | ns, Min |
| $T_{SRCK}/T_{CKSR}$ | SR input to CLK on A – D flip-flops | 0.38/0.03 | 0.43/0.04 | 0.53/0.05 | 0.53/0.18 | ns, Min |
| **Set/Reset** | | | | | | |
| $T_{SRMIN}$ | SR input minimum pulse width | 0.52 | 0.78 | 1.04 | 1.04 | ns, Min |
| $T_{RQ}$ | Delay from SR input to AQ – DQ flip-flops | 0.53 | 0.59 | 0.71 | 0.71 | ns, Max |
| $T_{CEO}$ | Delay from CE input to AQ – DQ flip-flops | 0.52 | 0.58 | 0.70 | 0.70 | ns, Max |
| $F_{TOG}$ | Toggle frequency (for export control) | 1412 | 1286 | 1098 | 1098 | MHz |

## CLB Distributed RAM Switching Characteristics (SLICEM Only)

*Table 63:* **CLB Distributed RAM Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1C/-1I/-1LI | -1Q | |
| **Sequential Delays** | | | | | | |
| $T_{SHCKO}$[(1)] | Clock to A – B outputs | 0.98 | 1.09 | 1.32 | 1.32 | ns, Max |
| $T_{SHCKO_1}$ | Clock to AMUX – BMUX outputs | 1.37 | 1.53 | 1.86 | 1.86 | ns, Max |

*Table 63:* **CLB Distributed RAM Switching Characteristics *(Cont'd)***

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1C/-1I/-1LI | -1Q | |
| **Setup and Hold Times Before/After Clock CLK** | | | | | | |
| $T_{DS_LRAM}$/ $T_{DH_LRAM}$ | A – D inputs to CLK | 0.54/0.28 | 0.60/0.30 | 0.72/0.35 | 0.72/0.37 | ns, Min |
| $T_{AS_LRAM}$/ $T_{AH_LRAM}$ | Address An inputs to clock | 0.27/0.55 | 0.30/0.60 | 0.37/0.70 | 0.37/0.71 | ns, Min |
| | Address An inputs through MUXs and/or carry logic to clock | 0.69/0.18 | 0.77/0.21 | 0.94/0.26 | 0.94/0.35 | ns, Min |
| $T_{WS_LRAM}$/ $T_{WH_LRAM}$ | WE input to clock | 0.38/0.10 | 0.43/0.12 | 0.53/0.17 | 0.53/0.17 | ns, Min |
| $T_{CECK_LRAM}$/ $T_{CKCE_LRAM}$ | CE input to CLK | 0.39/0.10 | 0.44/0.11 | 0.53/0.17 | 0.53/0.17 | ns, Min |
| **Clock CLK** | | | | | | |
| $T_{MPW_LRAM}$ | Minimum pulse width | 1.05 | 1.13 | 1.25 | 1.25 | ns, Min |
| $T_{MCP}$ | Minimum clock period | 2.10 | 2.26 | 2.50 | 2.50 | ns, Min |

**Notes:**

1. $T_{SHCKO}$ also represents the CLK to XMUX output. Refer to the timing report for the CLK to XMUX path.

## CLB Shift Register Switching Characteristics (SLICEM Only)

*Table 64:* **CLB Shift Register Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1C/-1I/-1LI | -1Q | |
| **Sequential Delays** | | | | | | |
| $T_{REG}$ | Clock to A – D outputs | 1.19 | 1.33 | 1.61 | 1.61 | ns, Max |
| $T_{REG_MUX}$ | Clock to AMUX – DMUX output | 1.58 | 1.77 | 2.15 | 2.15 | ns, Max |
| $T_{REG_M31}$ | Clock to DMUX output via M31 output | 1.12 | 1.23 | 1.46 | 1.46 | ns, Max |
| **Setup and Hold Times Before/After Clock CLK** | | | | | | |
| $T_{WS_SHFREG}$/ $T_{WH_SHFREG}$ | WE input | 0.37/0.10 | 0.41/0.12 | 0.51/0.17 | 0.51/0.17 | ns, Min |
| $T_{CECK_SHFREG}$/ $T_{CKCE_SHFREG}$ | CE input to CLK | 0.37/0.10 | 0.42/0.11 | 0.52/0.17 | 0.52/0.17 | ns, Min |
| $T_{DS_SHFREG}$/ $T_{DH_SHFREG}$ | A – D inputs to CLK | 0.33/0.34 | 0.37/0.37 | 0.44/0.43 | 0.44/0.44 | ns, Min |
| **Clock CLK** | | | | | | |
| $T_{MPW_SHFREG}$ | Minimum pulse width | 0.77 | 0.86 | 0.98 | 0.98 | ns, Min |

## Block RAM and FIFO Switching Characteristics

*Table 65:* **Block RAM and FIFO Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1C/-1I/-1LI | -1Q | |
| **Block RAM and FIFO Clock to Out Delays** | | | | | | |
| $T_{RCKO_DO}$ and $T_{RCKO_DO_REG}$[1] | Clock CLK to DOUT output (without output register)[2][3] | 1.85 | 2.13 | 2.46 | 2.46 | ns, Max |
| | Clock CLK to DOUT output (with output register)[4][5] | 0.64 | 0.74 | 0.89 | 0.89 | ns, Max |
| $T_{RCKO_DO_ECC}$ and $T_{RCKO_DO_ECC_REG}$ | Clock CLK to DOUT output with ECC (without output register)[2][3] | 2.77 | 3.04 | 3.84 | 3.84 | ns, Max |
| | Clock CLK to DOUT output with ECC (with output register)[4][5] | 0.73 | 0.81 | 0.94 | 0.94 | ns, Max |
| $T_{RCKO_DO_CASCOUT}$ and $T_{RCKO_DO_CASCOUT_REG}$ | Clock CLK to DOUT output with cascade (without output register)[2] | 2.61 | 2.88 | 3.30 | 3.30 | ns, Max |
| | Clock CLK to DOUT output with cascade (with output register)[4] | 1.16 | 1.28 | 1.46 | 1.46 | ns, Max |
| $T_{RCKO_FLAGS}$ | Clock CLK to FIFO flags outputs[6] | 0.76 | 0.87 | 1.05 | 1.05 | ns, Max |
| $T_{RCKO_POINTERS}$ | Clock CLK to FIFO pointers outputs[7] | 0.94 | 1.02 | 1.15 | 1.15 | ns, Max |
| $T_{RCKO_PARITY_ECC}$ | Clock CLK to ECCPARITY in ECC encode only mode | 0.78 | 0.85 | 0.94 | 0.94 | ns, Max |
| $T_{RCKO_SDBIT_ECC}$ and $T_{RCKO_SDBIT_ECC_REG}$ | Clock CLK to BITERR (without output register) | 2.56 | 2.81 | 3.55 | 3.55 | ns, Max |
| | Clock CLK to BITERR (with output register) | 0.68 | 0.76 | 0.89 | 0.89 | ns, Max |
| $T_{RCKO_RDADDR_ECC}$ and $T_{RCKO_RDADDR_ECC_REG}$ | Clock CLK to RDADDR output with ECC (without output register) | 0.75 | 0.88 | 1.07 | 1.07 | ns, Max |
| | Clock CLK to RDADDR output with ECC (with output register) | 0.84 | 0.93 | 1.08 | 1.08 | ns, Max |
| **Setup and Hold Times Before/After Clock CLK** | | | | | | |
| $T_{RCCK_ADDRA}$/ $T_{RCKC_ADDRA}$ | ADDR inputs[8] | 0.45/0.31 | 0.49/0.33 | 0.57/0.36 | 0.57/0.52 | ns, Min |
| $T_{RDCK_DI_WF_NC}$/ $T_{RCKD_DI_WF_NC}$ | Data input setup/hold time when block RAM is configured in WRITE_FIRST or NO_CHANGE mode[9] | 0.58/0.60 | 0.65/0.63 | 0.74/0.67 | 0.74/0.67 | ns, Min |
| $T_{RDCK_DI_RF}$/ $T_{RCKD_DI_RF}$ | Data input setup/hold time when block RAM is configured in READ_FIRST mode[9] | 0.20/0.29 | 0.22/0.34 | 0.25/0.41 | 0.25/0.50 | ns, Min |
| $T_{RDCK_DI_ECC}$/ $T_{RCKD_DI_ECC}$ | DIN inputs with block RAM ECC in standard mode[9] | 0.50/0.43 | 0.55/0.46 | 0.63/0.50 | 0.63/0.50 | ns, Min |
| | DIN inputs with block RAM ECC encode only[9] | 0.93/0.43 | 1.02/0.46 | 1.17/0.50 | 1.17/0.50 | ns, Min |
| | DIN inputs with FIFO ECC in standard mode[9] | 1.04/0.56 | 1.15/0.59 | 1.32/0.64 | 1.32/0.64 | ns, Min |
| $T_{RDCK_DI_ECCW}$/ $T_{RCKD_DI_ECCW}$ | DIN inputs with block RAM ECC encode only[9] | 0.93/0.43 | 1.02/0.46 | 1.17/0.50 | 1.17/0.50 | ns, Min |
| $T_{RDCK_DI_ECC_FIFO}$/ $T_{RCKD_DI_ECC_FIFO}$ | DIN inputs with FIFO ECC in standard mode[9] | 1.04/0.56 | 1.15/0.59 | 1.32/0.64 | 1.32/0.64 | ns, Min |
| $T_{RCCK_INJECTBITERR}$/ $T_{RCKC_INJECTBITERR}$ | Inject single/double bit error in ECC mode | 0.58/0.35 | 0.64/0.37 | 0.74/0.40 | 0.74/0.52 | ns, Min |

*Table 65:* **Block RAM and FIFO Switching Characteristics *(Cont'd)***

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1C/-1I/-1LI | -1Q | |
| $T_{RCCK_EN}$/ $T_{RCKC_EN}$ | Block RAM enable (EN) input | 0.35/0.20 | 0.39/0.21 | 0.45/0.23 | 0.45/0.41 | ns, Min |
| $T_{RCCK_REGCE}$/ $T_{RCKC_REGCE}$ | CE input of output register | 0.24/0.15 | 0.29/0.15 | 0.36/0.16 | 0.36/0.39 | ns, Min |
| $T_{RCCK_RSTREG}$/ $T_{RCKC_RSTREG}$ | Synchronous RSTREG input | 0.29/0.07 | 0.32/0.07 | 0.35/0.07 | 0.35/0.17 | ns, Min |
| $T_{RCCK_RSTRAM}$/ $T_{RCKC_RSTRAM}$ | Synchronous RSTRAM input | 0.32/0.42 | 0.34/0.43 | 0.36/0.46 | 0.36/0.57 | ns, Min |
| $T_{RCCK_WEA}$/ $T_{RCKC_WEA}$ | Write enable (WE) input (block RAM only) | 0.44/0.18 | 0.48/0.19 | 0.54/0.20 | 0.54/0.42 | ns, Min |
| $T_{RCCK_WREN}$/ $T_{RCKC_WREN}$ | WREN FIFO inputs | 0.46/0.30 | 0.46/0.35 | 0.47/0.43 | 0.47/0.43 | ns, Min |
| $T_{RCCK_RDEN}$/ $T_{RCKC_RDEN}$ | RDEN FIFO inputs | 0.42/0.30 | 0.43/0.35 | 0.43/0.43 | 0.43/0.62 | ns, Min |
| **Reset Delays** | | | | | | |
| $T_{RCO_FLAGS}$ | Reset RST to FIFO flags/pointers(10) | 0.90 | 0.98 | 1.10 | 1.10 | ns, Max |
| $T_{RREC_RST}$/ $T_{RREM_RST}$ | FIFO reset recovery and removal timing(11) | 1.87/–0.81 | 2.07/–0.81 | 2.37/–0.81 | 2.37/–0.58 | ns, Max |
| **Maximum Frequency** | | | | | | |
| $F_{MAX_BRAM_WF_NC}$ | Block RAM (write first and no change modes) When not in SDP RF mode. | 509.68 | 460.83 | 388.20 | 388.20 | MHz |
| $F_{MAX_BRAM_RF_PERFORMANCE}$ | Block RAM (read first, performance mode) When in SDP RF mode but no address overlap between port A and port B. | 509.68 | 460.83 | 388.20 | 388.20 | MHz |
| $F_{MAX_BRAM_RF_DELAYED_WRITE}$ | Block RAM (read first, delayed write mode) When in SDP RF mode and there is possibility of overlap between port A and port B addresses. | 447.63 | 404.53 | 339.67 | 339.67 | MHz |
| $F_{MAX_CAS_WF_NC}$ | Block RAM cascade (write first, no change mode) When cascade but not in RF mode. | 467.07 | 418.59 | 345.78 | 345.78 | MHz |
| $F_{MAX_CAS_RF_PERFORMANCE}$ | Block RAM cascade (read first, performance mode) When in cascade with RF mode and no possibility of address overlap/one port is disabled. | 467.07 | 418.59 | 345.78 | 345.78 | MHz |
| $F_{MAX_CAS_RF_DELAYED_WRITE}$ | When in cascade RF mode and there is a possibility of address overlap between port A and port B. | 405.35 | 362.19 | 297.35 | 297.35 | MHz |

*Table 65:* **Block RAM and FIFO Switching Characteristics *(Cont'd)***

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1C/-1I/-1LI | -1Q | |
| $F_{MAX_FIFO}$ | FIFO in all modes without ECC | 509.68 | 460.83 | 388.20 | 388.20 | MHz |
| $F_{MAX_ECC}$ | Block RAM and FIFO in ECC configuration | 410.34 | 365.10 | 297.53 | 297.53 | MHz |

**Notes:**

1. The timing report shows all of these parameters as $T_{RCKO_DO}$.
2. $T_{RCKO_DOR}$ includes $T_{RCKO_DOW}$, $T_{RCKO_DOPR}$, and $T_{RCKO_DOPW}$ as well as the B port equivalent timing parameters.
3. These parameters also apply to synchronous FIFO with DO_REG = 0.
4. $T_{RCKO_DO}$ includes $T_{RCKO_DOP}$ as well as the B port equivalent timing parameters.
5. These parameters also apply to multirate (asynchronous) and synchronous FIFO with DO_REG = 1.
6. $T_{RCKO_FLAGS}$ includes the following parameters: $T_{RCKO_AEMPTY}$, $T_{RCKO_AFULL}$, $T_{RCKO_EMPTY}$, $T_{RCKO_FULL}$, $T_{RCKO_RDERR}$, and $T_{RCKO_WRERR}$.
7. $T_{RCKO_POINTERS}$ includes both $T_{RCKO_RDCOUNT}$ and $T_{RCKO_WRCOUNT}$.
8. The ADDR setup and hold must be met when EN is asserted (even when WE is deasserted). Otherwise, block RAM data corruption is possible.
9. These parameters include both A and B inputs as well as the parity inputs of A and B.
10. $T_{RCO_FLAGS}$ includes the following flags: AEMPTY, AFULL, EMPTY, FULL, RDERR, WRERR, RDCOUNT, and WRCOUNT.
11. RDEN and WREN must be held Low prior to and during reset. The FIFO reset must be asserted for at least five positive clock edges of the slowest clock (WRCLK or RDCLK).

## DSP48E1 Switching Characteristics

*Table 66:* **DSP48E1 Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1C/-1I/-1LI | -1Q | |
| **Setup and Hold Times of Data/Control Pins to the Input Register Clock** | | | | | | |
| $T_{DSPDCK_A_AREG}$/ $T_{DSPCKD_A_AREG}$ | A input to A register CLK | 0.26/0.12 | 0.30/0.13 | 0.37/0.14 | 0.37/0.28 | ns |
| $T_{DSPDCK_B_BREG}$/$T_{DSPCKD_B_BREG}$ | B input to B register CLK | 0.33/0.15 | 0.38/0.16 | 0.45/0.18 | 0.45/0.25 | ns |
| $T_{DSPDCK_C_CREG}$/$T_{DSPCKD_C_CREG}$ | C input to C register CLK | 0.17/0.17 | 0.20/0.19 | 0.24/0.21 | 0.24/0.26 | ns |
| $T_{DSPDCK_D_DREG}$/$T_{DSPCKD_D_DREG}$ | D input to D register CLK | 0.25/0.25 | 0.32/0.27 | 0.42/0.27 | 0.42/0.42 | ns |
| $T_{DSPDCK_ACIN_AREG}$/ $T_{DSPCKD_ACIN_AREG}$ | ACIN input to A register CLK | 0.23/0.12 | 0.27/0.13 | 0.32/0.14 | 0.32/0.17 | ns |
| $T_{DSPDCK_BCIN_BREG}$/ $T_{DSPCKD_BCIN_BREG}$ | BCIN input to B register CLK | 0.25/0.15 | 0.29/0.16 | 0.36/0.18 | 0.36/0.18 | ns |
| **Setup and Hold Times of Data Pins to the Pipeline Register Clock** | | | | | | |
| $T_{DSPDCK_\{A, B\}_MREG_MULT}$/ $T_{DSPCKD_\{A, B\}_MREG_MULT}$ | {A, B} input to M register CLK using multiplier | 2.40/–0.01 | 2.76/–0.01 | 3.29/–0.01 | 3.29/–0.01 | ns |
| $T_{DSPDCK_\{A, D\}_ADREG}$/ $T_{DSPCKD_\{A, D\}_ADREG}$ | {A, D} input to AD register CLK | 1.29/–0.02 | 1.48/–0.02 | 1.76/–0.02 | 1.76/–0.02 | ns |
| **Setup and Hold Times of Data/Control Pins to the Output Register Clock** | | | | | | |
| $T_{DSPDCK_\{A, B\}_PREG_MULT}$/ $T_{DSPCKD_\{A, B\}_PREG_MULT}$ | {A, B} input to P register CLK using multiplier | 4.02/–0.28 | 4.60/–0.28 | 5.48/–0.28 | 5.48/–0.28 | ns |
| $T_{DSPDCK_D_PREG_MULT}$/ $T_{DSPCKD_D_PREG_MULT}$ | D input to P register CLK using multiplier | 3.93/–0.73 | 4.50/–0.73 | 5.35/–0.73 | 5.35/–0.73 | ns |
| $T_{DSPDCK_\{A, B\}_PREG}$/ $T_{DSPCKD_\{A, B\}_PREG}$ | A or B input to P register CLK not using multiplier | 1.73/–0.28 | 1.98/–0.28 | 2.35/–0.28 | 2.35/–0.28 | ns |
| $T_{DSPDCK_C_PREG}$/ $T_{DSPCKD_C_PREG}$ | C input to P register CLK not using multiplier | 1.54/–0.26 | 1.76/–0.26 | 2.10/–0.26 | 2.10/–0.26 | ns |
| $T_{DSPDCK_PCIN_PREG}$/ $T_{DSPCKD_PCIN_PREG}$ | PCIN input to P register CLK | 1.32/–0.15 | 1.51/–0.15 | 1.80/–0.15 | 1.80/–0.15 | ns |
| **Setup and Hold Times of the CE Pins** | | | | | | |
| $T_{DSPDCK_\{CEA;CEB\}_\{AREG;BREG\}}$/ $T_{DSPCKD_\{CEA;CEB\}_\{AREG;BREG\}}$ | {CEA; CEB} input to {A; B} register CLK | 0.35/0.06 | 0.42/0.08 | 0.52/0.11 | 0.52/0.11 | ns |
| $T_{DSPDCK_CEC_CREG}$/ $T_{DSPCKD_CEC_CREG}$ | CEC input to C register CLK | 0.28/0.10 | 0.34/0.11 | 0.42/0.13 | 0.42/0.13 | ns |
| $T_{DSPDCK_CED_DREG}$/ $T_{DSPCKD_CED_DREG}$ | CED input to D register CLK | 0.36/–0.03 | 0.43/–0.03 | 0.52/–0.03 | 0.52/–0.03 | ns |
| $T_{DSPDCK_CEM_MREG}$/ $T_{DSPCKD_CEM_MREG}$ | CEM input to M register CLK | 0.17/0.18 | 0.21/0.20 | 0.27/0.23 | 0.27/0.23 | ns |
| $T_{DSPDCK_CEP_PREG}$/ $T_{DSPCKD_CEP_PREG}$ | CEP input to P register CLK | 0.36/0.01 | 0.43/0.01 | 0.53/0.01 | 0.53/0.01 | ns |
| **Setup and Hold Times of the RST Pins** | | | | | | |
| $T_{DSPDCK_\{RSTA; RSTB\}_\{AREG; BREG\}}$/ $T_{DSPCKD_\{RSTA; RSTB\}_\{AREG; BREG\}}$ | {RSTA, RSTB} input to {A, B} register CLK | 0.41/0.11 | 0.46/0.13 | 0.55/0.15 | 0.55/0.24 | ns |
| $T_{DSPDCK_RSTC_CREG}$/ $T_{DSPCKD_RSTC_CREG}$ | RSTC input to C register CLK | 0.07/0.10 | 0.08/0.11 | 0.09/0.12 | 0.09/0.25 | ns |
| $T_{DSPDCK_RSTD_DREG}$/ $T_{DSPCKD_RSTD_DREG}$ | RSTD input to D register CLK | 0.44/0.07 | 0.50/0.08 | 0.59/0.09 | 0.59/0.09 | ns |
| $T_{DSPDCK_RSTM_MREG}$/ $T_{DSPCKD_RSTM_MREG}$ | RSTM input to M register CLK | 0.21/0.22 | 0.23/0.24 | 0.27/0.28 | 0.27/0.28 | ns |

*Table 66:* **DSP48E1 Switching Characteristics *(Cont'd)***

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1C/-1I/-1LI | -1Q | |
| $T_{DSPDCK_RSTP_PREG}$/ $T_{DSPCKD_RSTP_PREG}$ | RSTP input to P register CLK | 0.27/0.01 | 0.30/0.01 | 0.35/0.01 | 0.35/0.03 | ns |
| **Combinatorial Delays from Input Pins to Output Pins** | | | | | | |
| $T_{DSPDO_A_CARRYOUT_MULT}$ | A input to CARRYOUT output using multiplier | 3.79 | 4.35 | 5.18 | 5.18 | ns |
| $T_{DSPDO_D_P_MULT}$ | D input to P output using multiplier | 3.72 | 4.26 | 5.07 | 5.07 | ns |
| $T_{DSPDO_A_P}$ | A input to P output not using multiplier | 1.53 | 1.75 | 2.08 | 2.08 | ns |
| $T_{DSPDO_C_P}$ | C input to P output | 1.33 | 1.53 | 1.82 | 1.82 | ns |
| **Combinatorial Delays from Input Pins to Cascading Output Pins** | | | | | | |
| $T_{DSPDO_\{A; B\}_\{ACOUT; BCOUT\}}$ | {A, B} input to {ACOUT, BCOUT} output | 0.55 | 0.63 | 0.74 | 0.74 | ns |
| $T_{DSPDO_\{A, B\}_CARRYCASCOUT_MULT}$ | {A, B} input to CARRYCASCOUT output using multiplier | 4.06 | 4.65 | 5.54 | 5.54 | ns |
| $T_{DSPDO_D_CARRYCASCOUT_MULT}$ | D input to CARRYCASCOUT output using multiplier | 3.97 | 4.54 | 5.40 | 5.40 | ns |
| $T_{DSPDO_\{A, B\}_CARRYCASCOUT}$ | {A, B} input to CARRYCASCOUT output not using multiplier | 1.77 | 2.03 | 2.41 | 2.41 | ns |
| $T_{DSPDO_C_CARRYCASCOUT}$ | C input to CARRYCASCOUT output | 1.58 | 1.81 | 2.15 | 2.15 | ns |
| **Combinatorial Delays from Cascading Input Pins to All Output Pins** | | | | | | |
| $T_{DSPDO_ACIN_P_MULT}$ | ACIN input to P output using multiplier | 3.65 | 4.19 | 5.00 | 5.00 | ns |
| $T_{DSPDO_ACIN_P}$ | ACIN input to P output not using multiplier | 1.37 | 1.57 | 1.88 | 1.88 | ns |
| $T_{DSPDO_ACIN_ACOUT}$ | ACIN input to ACOUT output | 0.38 | 0.44 | 0.53 | 0.53 | ns |
| $T_{DSPDO_ACIN_CARRYCASCOUT_MULT}$ | ACIN input to CARRYCASCOUT output using multiplier | 3.90 | 4.47 | 5.33 | 5.33 | ns |
| $T_{DSPDO_ACIN_CARRYCASCOUT}$ | ACIN input to CARRYCASCOUT output not using multiplier | 1.61 | 1.85 | 2.21 | 2.21 | ns |
| $T_{DSPDO_PCIN_P}$ | PCIN input to P output | 1.11 | 1.28 | 1.52 | 1.52 | ns |
| $T_{DSPDO_PCIN_CARRYCASCOUT}$ | PCIN input to CARRYCASCOUT output | 1.36 | 1.56 | 1.85 | 1.85 | ns |
| **Clock to Outs from Output Register Clock to Output Pins** | | | | | | |
| $T_{DSPCKO_P_PREG}$ | CLK PREG to P output | 0.33 | 0.37 | 0.44 | 0.44 | ns |
| $T_{DSPCKO_CARRYCASCOUT_PREG}$ | CLK PREG to CARRYCASCOUT output | 0.52 | 0.59 | 0.69 | 0.69 | ns |
| **Clock to Outs from Pipeline Register Clock to Output Pins** | | | | | | |
| $T_{DSPCKO_P_MREG}$ | CLK MREG to P output | 1.68 | 1.93 | 2.31 | 2.31 | ns |
| $T_{DSPCKO_CARRYCASCOUT_MREG}$ | CLK MREG to CARRYCASCOUT output | 1.92 | 2.21 | 2.64 | 2.64 | ns |
| $T_{DSPCKO_P_ADREG_MULT}$ | CLK ADREG to P output using multiplier | 2.72 | 3.10 | 3.69 | 3.69 | ns |
| $T_{DSPCKO_CARRYCASCOUT_ADREG_MULT}$ | CLK ADREG to CARRYCASCOUT output using multiplier | 2.96 | 3.38 | 4.02 | 4.02 | ns |

*Table 66:* **DSP48E1 Switching Characteristics *(Cont'd)***

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1C/-1I/-1LI | -1Q | |
| **Clock to Outs from Input Register Clock to Output Pins** | | | | | | |
| $T_{DSPCKO_P_AREG_MULT}$ | CLK AREG to P output using multiplier | 3.94 | 4.51 | 5.37 | 5.37 | ns |
| $T_{DSPCKO_P_BREG}$ | CLK BREG to P output not using multiplier | 1.64 | 1.87 | 2.22 | 2.22 | ns |
| $T_{DSPCKO_P_CREG}$ | CLK CREG to P output not using multiplier | 1.69 | 1.93 | 2.30 | 2.30 | ns |
| $T_{DSPCKO_P_DREG_MULT}$ | CLK DREG to P output using multiplier | 3.91 | 4.48 | 5.32 | 5.32 | ns |
| **Clock to Outs from Input Register Clock to Cascading Output Pins** | | | | | | |
| $T_{DSPCKO_\{ACOUT; BCOUT\}_\{AREG; BREG\}}$ | CLK (ACOUT, BCOUT) to {A,B} register output | 0.64 | 0.73 | 0.87 | 0.87 | ns |
| $T_{DSPCKO_CARRYCASCOUT_\{AREG, BREG\}_MULT}$ | CLK (AREG, BREG) to CARRYCASCOUT output using multiplier | 4.19 | 4.79 | 5.70 | 5.70 | ns |
| $T_{DSPCKO_CARRYCASCOUT_BREG}$ | CLK BREG to CARRYCASCOUT output not using multiplier | 1.88 | 2.15 | 2.55 | 2.55 | ns |
| $T_{DSPCKO_CARRYCASCOUT_DREG_MULT}$ | CLK DREG to CARRYCASCOUT output using multiplier | 4.16 | 4.76 | 5.65 | 5.65 | ns |
| $T_{DSPCKO_CARRYCASCOUT_CREG}$ | CLK CREG to CARRYCASCOUT output | 1.94 | 2.21 | 2.63 | 2.63 | ns |
| **Maximum Frequency** | | | | | | |
| $F_{MAX}$ | With all registers used | 628.93 | 550.66 | 464.25 | 464.25 | MHz |
| $F_{MAX_PATDET}$ | With pattern detector | 531.63 | 465.77 | 392.93 | 392.93 | MHz |
| $F_{MAX_MULT_NOMREG}$ | Two register multiply without MREG | 349.28 | 305.62 | 257.47 | 257.47 | MHz |
| $F_{MAX_MULT_NOMREG_PATDET}$ | Two register multiply without MREG with pattern detect | 317.26 | 277.62 | 233.92 | 233.92 | MHz |
| $F_{MAX_PREADD_MULT_NOADREG}$ | Without ADREG | 397.30 | 346.26 | 290.44 | 290.44 | MHz |
| $F_{MAX_PREADD_MULT_NOADREG_PATDET}$ | Without ADREG with pattern detect | 397.30 | 346.26 | 290.44 | 290.44 | MHz |
| $F_{MAX_NOPIPELINEREG}$ | Without pipeline registers (MREG, ADREG) | 260.01 | 227.01 | 190.69 | 190.69 | MHz |
| $F_{MAX_NOPIPELINEREG_PATDET}$ | Without pipeline registers (MREG, ADREG) with pattern detect | 241.72 | 211.15 | 177.43 | 177.43 | MHz |

## Clock Buffers and Networks

*Table 67:* **Global Clock Switching Characteristics (Including BUFGCTRL)**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1C/-1I/-1LI | -1Q | |
| $T_{BCCCK_CE}/T_{BCCKC_CE}$(1) | CE pins setup/hold | 0.13/0.39 | 0.14/0.41 | 0.18/0.42 | 0.18/0.84 | ns |
| $T_{BCCCK_S}/T_{BCCKC_S}$(1) | S pins setup/hold | 0.13/0.39 | 0.14/0.41 | 0.18/0.42 | 0.18/0.84 | ns |
| $T_{BCCKO_O}$(2) | BUFGCTRL delay from I0/I1 to O | 0.08 | 0.09 | 0.11 | 0.11 | ns |
| **Maximum Frequency** | | | | | | |
| $F_{MAX_BUFG}$ | Global clock tree (BUFG) | 628.00 | 628.00 | 464.00 | 464.00 | MHz |

**Notes:**

1. $T_{BCCCK_CE}$ and $T_{BCCKC_CE}$ must be satisfied to assure glitch-free operation of the global clock when switching between clocks. These parameters do not apply to the BUFGMUX primitive that assures glitch-free operation. The other global clock setup and hold times are optional; only needing to be satisfied if device operation requires simulation matches on a cycle-for-cycle basis when switching between clocks.
2. $T_{BGCKO_O}$ (BUFG delay from I0 to O) values are the same as $T_{BCCKO_O}$ values.

*Table 68:* **Input/Output Clock Switching Characteristics (BUFIO)**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1C/-1I/-1LI | -1Q | |
| $T_{BIOCKO_O}$ | Clock to out delay from I to O | 1.16 | 1.32 | 1.61 | 1.61 | ns |
| **Maximum Frequency** | | | | | | |
| $F_{MAX_BUFIO}$ | I/O clock tree (BUFIO) | 680.00 | 680.00 | 600.00 | 600.00 | MHz |

*Table 69:* **Regional Clock Buffer Switching Characteristics (BUFR)**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1C/-1I/-1LI | -1Q | |
| $T_{BRCKO_O}$ | Clock to out delay from I to O | 0.64 | 0.80 | 1.04 | 1.04 | ns |
| $T_{BRCKO_O_BYP}$ | Clock to out delay from I to O with Divide Bypass attribute set | 0.35 | 0.41 | 0.54 | 0.54 | ns |
| $T_{BRDO_O}$ | Propagation delay from CLR to O | 0.85 | 0.89 | 1.14 | 1.14 | ns |
| **Maximum Frequency** | | | | | | |
| $F_{MAX_BUFR}$(1) | Regional clock tree (BUFR) | 420.00 | 375.00 | 315.00 | 315.00 | MHz |

**Notes:**

1. The maximum input frequency to the BUFR and BUFMR is the BUFIO $F_{MAX}$ frequency.

*Table 70:* **Horizontal Clock Buffer Switching Characteristics (BUFH)**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1C/-1I/-1LI | -1Q | |
| $T_{BHCKO_O}$ | BUFH delay from I to O | 0.11 | 0.11 | 0.14 | 0.14 | ns |
| $T_{BHCCK_CE}/T_{BHCKC_CE}$ | CE pin setup and hold | 0.20/0.13 | 0.23/0.16 | 0.29/0.21 | 0.29/0.43 | ns |
| **Maximum Frequency** | | | | | | |
| $F_{MAX_BUFH}$ | Horizontal clock buffer (BUFH) | 628.00 | 628.00 | 464.00 | 464.00 | MHz |

*Table 71:* **Duty-Cycle Distortion and Clock-Tree Skew**

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | -3 | -2 | -1C/-1I/-1LI | -1Q | |
| $T_{DCD_CLK}$ | Global clock tree duty-cycle distortion(1) | All | 0.20 | 0.20 | 0.20 | 0.20 | ns |
| $T_{CKSKEW}$ | Global clock tree skew(2) | XC7Z007S | N/A | 0.27 | 0.27 | N/A | ns |
| | | XC7Z012S | N/A | 0.39 | 0.42 | N/A | ns |
| | | XC7Z014S | N/A | 0.38 | 0.42 | N/A | ns |
| | | XC7Z010 | 0.27 | 0.27 | 0.27 | N/A | ns |
| | | XC7Z015 | 0.33 | 0.39 | 0.42 | N/A | ns |
| | | XC7Z020 | 0.33 | 0.38 | 0.42 | N/A | ns |
| | | XA7Z010 | N/A | N/A | 0.27 | 0.27 | ns |
| | | XA7Z020 | N/A | N/A | 0.42 | 0.42 | ns |
| | | XQ7Z020 | N/A | 0.38 | 0.42 | 0.42 | ns |
| $T_{DCD_BUFIO}$ | I/O clock tree duty-cycle distortion | All | 0.14 | 0.14 | 0.14 | 0.14 | ns |
| $T_{BUFIOSKEW}$ | I/O clock tree skew across one clock region | All | 0.03 | 0.03 | 0.03 | 0.03 | ns |
| $T_{DCD_BUFR}$ | Regional clock tree duty-cycle distortion | All | 0.18 | 0.18 | 0.18 | 0.18 | ns |

**Notes:**

1. These parameters represent the worst-case duty-cycle distortion observable at the pins of the device using LVDS output buffers. For cases where other I/O standards are used, IBIS can be used to calculate any additional duty-cycle distortion that might be caused by asymmetrical rise/fall times.
2. The $T_{CKSKEW}$ value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx Timing Analyzer tools to evaluate application specific clock skew.

## MMCM Switching Characteristics

*Table 72:* **MMCM Specification**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1C/-1I/-1LI | -1Q | |
| $MMCM_F_{INMAX}$ | Maximum input clock frequency | 800.00 | 800.00 | 800.00 | 800.00 | MHz |
| $MMCM_F_{INMIN}$ | Minimum input clock frequency | 10.00 | 10.00 | 10.00 | 10.00 | MHz |
| $MMCM_F_{INJITTER}$ | Maximum input clock period jitter | < 20% of clock input period or 1 ns Max | | | | |
| $MMCM_F_{INDUTY}$ | Allowable input duty cycle: 10—49 MHz | 25 | 25 | 25 | 25 | % |
| | Allowable input duty cycle: 50—199 MHz | 30 | 30 | 30 | 30 | % |
| | Allowable input duty cycle: 200—399 MHz | 35 | 35 | 35 | 35 | % |
| | Allowable input duty cycle: 400—499 MHz | 40 | 40 | 40 | 40 | % |
| | Allowable input duty cycle: >500 MHz | 45 | 45 | 45 | 45 | % |
| $MMCM_F_{MIN_PSCLK}$ | Minimum dynamic phase-shift clock frequency | 0.01 | 0.01 | 0.01 | 0.01 | MHz |
| $MMCM_F_{MAX_PSCLK}$ | Maximum dynamic phase-shift clock frequency | 550.00 | 500.00 | 450.00 | 450.00 | MHz |
| $MMCM_F_{VCOMIN}$ | Minimum MMCM VCO frequency | 600.00 | 600.00 | 600.00 | 600.00 | MHz |
| $MMCM_F_{VCOMAX}$ | Maximum MMCM VCO frequency | 1600.00 | 1440.00 | 1200.00 | 1200.00 | MHz |
| $MMCM_F_{BANDWIDTH}$ | Low MMCM bandwidth at typical(1) | 1.00 | 1.00 | 1.00 | 1.00 | MHz |
| | High MMCM bandwidth at typical(1) | 4.00 | 4.00 | 4.00 | 4.00 | MHz |
| $MMCM_T_{STATPHAOFFSET}$ | Static phase offset of the MMCM outputs(2) | 0.12 | 0.12 | 0.12 | 0.12 | ns |
| $MMCM_T_{OUTJITTER}$ | MMCM output jitter | Note 3 | | | | |
| $MMCM_T_{OUTDUTY}$ | MMCM output clock duty-cycle precision(4) | 0.20 | 0.20 | 0.20 | 0.20 | ns |

*Table 72:* **MMCM Specification *(Cont'd)***

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1C/-1I/-1LI | -1Q | |
| MMCM_$T_{LOCKMAX}$ | MMCM maximum lock time | 100.00 | 100.00 | 100.00 | 100.00 | µs |
| MMCM_$F_{OUTMAX}$ | MMCM maximum output frequency | 800.00 | 800.00 | 800.00 | 800.00 | MHz |
| MMCM_$F_{OUTMIN}$ | MMCM minimum output frequency(5)(6) | 4.69 | 4.69 | 4.69 | 4.69 | MHz |
| MMCM_$T_{EXTFDVAR}$ | External clock feedback variation | < 20% of clock input period or 1 ns Max | | | | |
| MMCM_$RST_{MINPULSE}$ | Minimum reset pulse width | 5.00 | 5.00 | 5.00 | 5.00 | ns |
| MMCM_$F_{PFDMAX}$ | Maximum frequency at the phase frequency detector | 550.00 | 500.00 | 450.00 | 450.00 | MHz |
| MMCM_$F_{PFDMIN}$ | Minimum frequency at the phase frequency detector | 10.00 | 10.00 | 10.00 | 10.00 | MHz |
| MMCM_$T_{FBDELAY}$ | Maximum delay in the feedback path | 3 ns Max or one CLKIN cycle | | | | |
| **MMCM Switching Characteristics Setup and Hold** | | | | | | |
| $T_{MMCMDCK_PSEN}$/ $T_{MMCMCKD_PSEN}$ | Setup and hold of phase-shift enable | 1.04/0.00 | 1.04/0.00 | 1.04/0.00 | 1.04/0.00 | ns |
| $T_{MMCMDCK_PSINCDEC}$/ $T_{MMCMCKD_PSINCDEC}$ | Setup and hold of phase-shift increment/decrement | 1.04/0.00 | 1.04/0.00 | 1.04/0.00 | 1.04/0.00 | ns |
| $T_{MMCMCKO_PSDONE}$ | Phase shift clock-to-out of PSDONE | 0.59 | 0.68 | 0.81 | 0.81 | ns |
| **Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK** | | | | | | |
| $T_{MMCMDCK_DADDR}$/ $T_{MMCMCKD_DADDR}$ | DADDR setup/hold | 1.25/0.15 | 1.40/0.15 | 1.63/0.15 | 1.63/0.15 | ns, Min |
| $T_{MMCMDCK_DI}$/ $T_{MMCMCKD_DI}$ | DI setup/hold | 1.25/0.15 | 1.40/0.15 | 1.63/0.15 | 1.63/0.15 | ns, Min |
| $T_{MMCMDCK_DEN}$/ $T_{MMCMCKD_DEN}$ | DEN setup/hold | 1.76/0.00 | 1.97/0.00 | 2.29/0.00 | 2.29/0.00 | ns, Min |
| $T_{MMCMDCK_DWE}$/ $T_{MMCMCKD_DWE}$ | DWE setup/hold | 1.25/0.15 | 1.40/0.15 | 1.63/0.15 | 1.63/0.15 | ns, Min |
| $T_{MMCMCKO_DRDY}$ | CLK to out of DRDY | 0.65 | 0.72 | 0.99 | 0.99 | ns, Max |
| $F_{DCK}$ | DCLK frequency | 200.00 | 200.00 | 200.00 | 200.00 | MHz, Max |

**Notes:**

1. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any MMCM outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard. See http://www.xilinx.com/products/intellectual-property/clocking_wizard.htm.
4. Includes global clock buffer.
5. Calculated as $F_{VCO}/128$ assuming output duty cycle is 50%.
6. When CLKOUT4_CASCADE = TRUE, MMCM_$F_{OUTMIN}$ is 0.036 MHz.

## PLL Switching Characteristics

*Table 73:* **PLL Specification**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1C/-1I/-1LI | -1Q | |
| PLL_$F_{INMAX}$ | Maximum input clock frequency | 800.00 | 800.00 | 800.00 | 800.00 | MHz |
| PLL_$F_{INMIN}$ | Minimum input clock frequency | 19.00 | 19.00 | 19.00 | 19.00 | MHz |
| PLL_$F_{INJITTER}$ | Maximum input clock period jitter | < 20% of clock input period or 1 ns Max | | | | |
| PLL_$F_{INDUTY}$ | Allowable input duty cycle: 19—49 MHz | 25 | 25 | 25 | 25 | % |
| | Allowable input duty cycle: 50—199 MHz | 30 | 30 | 30 | 30 | % |
| | Allowable input duty cycle: 200—399 MHz | 35 | 35 | 35 | 35 | % |
| | Allowable input duty cycle: 400—499 MHz | 40 | 40 | 40 | 40 | % |
| | Allowable input duty cycle: >500 MHz | 45 | 45 | 45 | 45 | % |
| PLL_$F_{VCOMIN}$ | Minimum PLL VCO frequency | 800.00 | 800.00 | 800.00 | 800.00 | MHz |
| PLL_$F_{VCOMAX}$ | Maximum PLL VCO frequency | 2133.00 | 1866.00 | 1600.00 | 1600.00 | MHz |
| PLL_$F_{BANDWIDTH}$ | Low PLL bandwidth at typical(1) | 1.00 | 1.00 | 1.00 | 1.00 | MHz |
| | High PLL bandwidth at typical(1) | 4.00 | 4.00 | 4.00 | 4.00 | MHz |
| PLL_$T_{STATPHAOFFSET}$ | Static phase offset of the PLL outputs(2) | 0.12 | 0.12 | 0.12 | 0.12 | ns |
| PLL_$T_{OUTJITTER}$ | PLL output jitter | Note 3 | | | | |
| PLL_$T_{OUTDUTY}$ | PLL output clock duty-cycle precision(4) | 0.20 | 0.20 | 0.20 | 0.20 | ns |
| PLL_$T_{LOCKMAX}$ | PLL maximum lock time | 100.00 | 100.00 | 100.00 | 100.00 | µs |
| PLL_$F_{OUTMAX}$ | PLL maximum output frequency | 800.00 | 800.00 | 800.00 | 800.00 | MHz |
| PLL_$F_{OUTMIN}$ | PLL minimum output frequency(5) | 6.25 | 6.25 | 6.25 | 6.25 | MHz |
| PLL_$T_{EXTFDVAR}$ | External clock feedback variation | < 20% of clock input period or 1 ns Max | | | | |
| PLL_$RST_{MINPULSE}$ | Minimum reset pulse width | 5.00 | 5.00 | 5.00 | 5.00 | ns |
| PLL_$F_{PFDMAX}$ | Maximum frequency at the phase frequency detector | 550.00 | 500.00 | 450.00 | 450.00 | MHz |
| PLL_$F_{PFDMIN}$ | Minimum frequency at the phase frequency detector | 19.00 | 19.00 | 19.00 | 19.00 | MHz |
| PLL_$T_{FBDELAY}$ | Maximum delay in the feedback path | 3 ns Max or one CLKIN cycle | | | | |
| **Dynamic Reconfiguration Port (DRP) for PLL Before and After DCLK** | | | | | | |
| $T_{PLLCCK_DADDR}/T_{PLLCKC_DADDR}$ | Setup and hold of D address | 1.25/0.15 | 1.40/0.15 | 1.63/0.15 | 1.63/0.15 | ns, Min |
| $T_{PLLCCK_DI}/T_{PLLCKC_DI}$ | Setup and hold of D input | 1.25/0.15 | 1.40/0.15 | 1.63/0.15 | 1.63/0.15 | ns, Min |
| $T_{PLLCCK_DEN}/T_{PLLCKC_DEN}$ | Setup and hold of D enable | 1.76/0.00 | 1.97/0.00 | 2.29/0.00 | 2.29/0.00 | ns, Min |
| $T_{PLLCCK_DWE}/T_{PLLCKC_DWE}$ | Setup and hold of D write enable | 1.25/0.15 | 1.40/0.15 | 1.63/0.15 | 1.63/0.15 | ns, Min |
| $T_{PLLCKO_DRDY}$ | CLK to out of DRDY | 0.65 | 0.72 | 0.99 | 0.99 | ns, Max |
| $F_{DCK}$ | DCLK frequency | 200.00 | 200.00 | 200.00 | 200.00 | MHz, Max |

**Notes:**

1. The PLL does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any PLL outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard. See http://www.xilinx.com/products/intellectual-property/clocking_wizard.htm.
4. Includes global clock buffer.
5. Calculated as $F_{VCO}/128$ assuming output duty cycle is 50%.

## Device Pin-to-Pin Output Parameter Guidelines

*Table 74:* **Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Near Clock Region)(1)**

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | -3 | -2 | -1C/-1I/-1LI | -1Q | |
| SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flops, Fast Slew Rate, *without* MMCM/PLL. | | | | | | | |
| $T_{ICKOF}$ | Clock-capable clock input and OUTFF at pins/banks closest to the BUFGs *without* MMCM/PLL (near clock region)(2) | XC7Z007S | N/A | 5.68 | 6.65 | N/A | ns |
| | | XC7Z012S | N/A | 5.96 | 6.90 | N/A | ns |
| | | XC7Z014S | N/A | 6.05 | 7.08 | N/A | ns |
| | | XC7Z010 | 5.08 | 5.68 | 6.65 | N/A | ns |
| | | XC7Z015 | 5.34 | 5.96 | 6.90 | N/A | ns |
| | | XC7Z020 | 5.42 | 6.05 | 7.08 | N/A | ns |
| | | XA7Z010 | N/A | N/A | 6.65 | 6.65 | ns |
| | | XA7Z020 | N/A | N/A | 7.08 | 7.08 | ns |
| | | XQ7Z020 | N/A | 6.05 | 7.08 | 7.08 | ns |

**Notes:**

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Refer to the *Die Level Bank Numbering Overview* section of *Zynq-7000 SoC Packaging and Pinout Specification* (UG865).

*Table 75:* **Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Far Clock Region)(1)**

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | -3 | -2 | -1C/-1I/-1LI | -1Q | |
| SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flops, Fast Slew Rate, *without* MMCM/PLL. | | | | | | | |
| $T_{ICKOFFAR}$ | Clock-capable clock input and OUTFF at pins/banks farthest from the BUFGs *without* MMCM/PLL (far clock region)(2) | XC7Z007S | N/A | 5.68 | 6.65 | N/A | ns |
| | | XC7Z012S | N/A | 6.25 | 7.21 | N/A | ns |
| | | XC7Z014S | N/A | 6.34 | 7.40 | N/A | ns |
| | | XC7Z010 | 5.08 | 5.68 | 6.65 | N/A | ns |
| | | XC7Z015 | 5.60 | 6.25 | 7.21 | N/A | ns |
| | | XC7Z020 | 5.69 | 6.34 | 7.40 | N/A | ns |
| | | XA7Z010 | N/A | N/A | 6.65 | 6.65 | ns |
| | | XA7Z020 | N/A | N/A | 7.40 | 7.40 | ns |
| | | XQ7Z020 | N/A | 6.34 | 7.40 | 7.40 | ns |

**Notes:**

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Refer to the *Die Level Bank Numbering Overview* section of *Zynq-7000 SoC Packaging and Pinout Specification* (UG865).

*Table 76:* **Clock-Capable Clock Input to Output Delay With MMCM**

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | -3 | -2 | -1C/-1I/-1LI | -1Q | |
| SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flops, Fast Slew Rate, *with* MMCM. | | | | | | | |
| $T_{ICKOFMMCMCC}$ | Clock-capable clock input and OUTFF *with* MMCM | XC7Z007S | N/A | 1.03 | 1.03 | N/A | ns |
| | | XC7Z012S | N/A | 1.04 | 1.06 | N/A | ns |
| | | XC7Z014S | N/A | 1.04 | 1.05 | N/A | ns |
| | | XC7Z010 | 1.04 | 1.03 | 1.03 | N/A | ns |
| | | XC7Z015 | 1.05 | 1.04 | 1.06 | N/A | ns |
| | | XC7Z020 | 1.05 | 1.04 | 1.05 | N/A | ns |
| | | XA7Z010 | N/A | N/A | 1.03 | 1.03 | ns |
| | | XA7Z020 | N/A | N/A | 1.05 | 1.05 | ns |
| | | XQ7Z020 | N/A | 1.04 | 1.05 | 1.05 | ns |

**Notes:**

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

*Table 77:* **Clock-Capable Clock Input to Output Delay With PLL**

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | -3 | -2 | -1C/-1I/-1LI | -1Q | |
| SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flops, Fast Slew Rate, *with* PLL. | | | | | | | |
| $T_{ICKOFPLLCC}$ | Clock-capable clock input and OUTFF *with* PLL | XC7Z007S | N/A | 0.82 | 0.82 | N/A | ns |
| | | XC7Z012S | N/A | 0.82 | 0.82 | N/A | ns |
| | | XC7Z014S | N/A | 0.82 | 0.82 | N/A | ns |
| | | XC7Z010 | 0.82 | 0.82 | 0.82 | N/A | ns |
| | | XC7Z015 | 0.82 | 0.82 | 0.82 | N/A | ns |
| | | XC7Z020 | 0.82 | 0.82 | 0.82 | N/A | ns |
| | | XA7Z010 | N/A | N/A | 0.82 | 0.82 | ns |
| | | XA7Z020 | N/A | N/A | 0.82 | 0.82 | ns |
| | | XQ7Z020 | N/A | 0.82 | 0.82 | 0.82 | ns |

**Notes:**

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. PLL output jitter is already included in the timing calculation.

*Table 78:* **Pin-to-Pin, Clock-to-Out using BUFIO**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1C/-1I/-1LI | -1Q | |
| SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, with BUFIO. | | | | | | |
| $T_{ICKOFCS}$ | Clock to out of I/O clock | 5.14 | 5.76 | 6.81 | 6.81 | ns |

## Device Pin-to-Pin Input Parameter Guidelines

*Table 79:* **Global Clock Input Setup and Hold Without MMCM/PLL with ZHOLD_DELAY on HR I/O Banks**

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | -3 | -2 | -1C/-1I/-1LI | -1Q | |
| Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard.(1) | | | | | | | |
| $T_{PSFD}$/ $T_{PHFD}$ | Full delay (legacy delay or default delay) global clock input and IFF(2) without MMCM/PLL with ZHOLD_DELAY on HR I/O banks | XC7Z007S | N/A | 2.13/–0.17 | 2.44/–0.17 | N/A | ns |
| | | XC7Z012S | N/A | 2.55/–0.18 | 3.03/–0.18 | N/A | ns |
| | | XC7Z014S | N/A | 2.74/–0.25 | 3.18/–0.25 | N/A | ns |
| | | XC7Z010 | 2.00/–0.17 | 2.13/–0.17 | 2.44/–0.17 | N/A | ns |
| | | XC7Z015 | 2.38/–0.18 | 2.55/–0.18 | 3.03/–0.18 | N/A | ns |
| | | XC7Z020 | 2.55/–0.25 | 2.74/–0.25 | 3.18/–0.25 | N/A | ns |
| | | XA7Z010 | N/A | N/A | 2.44/–0.17 | 2.44/–0.17 | ns |
| | | XA7Z020 | N/A | N/A | 3.18/–0.25 | 3.18/–0.25 | ns |
| | | XQ7Z020 | N/A | 2.74/–0.25 | 3.18/–0.25 | 3.18/–0.25 | ns |

**Notes:**

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input flip-flop or latch.

*Table 80:* **Clock-Capable Clock Input Setup and Hold With MMCM**

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | -3 | -2 | -1C/-1I/-1LI | -1Q | |
| Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard.(1) | | | | | | | |
| $T_{PSMMCMCC}$/ $T_{PHMMCMCC}$ | No delay clock-capable clock input and IFF(2) with MMCM | XC7Z007S | N/A | 2.68/–0.62 | 3.22/–0.62 | N/A | ns |
| | | XC7Z012S | N/A | 2.80/–0.62 | 3.34/–0.62 | N/A | ns |
| | | XC7Z014S | N/A | 2.82/–0.62 | 3.38/–0.62 | N/A | ns |
| | | XC7Z010 | 2.36/–0.62 | 2.68/–0.62 | 3.22/–0.62 | N/A | ns |
| | | XC7Z015 | 2.47/–0.62 | 2.80/–0.62 | 3.34/–0.62 | N/A | ns |
| | | XC7Z020 | 2.48/–0.62 | 2.82/–0.62 | 3.38/–0.62 | N/A | ns |
| | | XA7Z010 | N/A | N/A | 3.22/–0.62 | 3.22/–0.62 | ns |
| | | XA7Z020 | N/A | N/A | 3.38/–0.62 | 3.38/–0.62 | ns |
| | | XQ7Z020 | N/A | 2.82/–0.62 | 3.38/–0.62 | 3.38/–0.62 | ns |

**Notes:**

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input flip-flop or latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

*Table 81:* **Clock-Capable Clock Input Setup and Hold With PLL**

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | -3 | -2 | -1C/-1I/-1LI | -1Q | |
| Input Setup and Hold Time Relative to Clock-Capable Clock Input Signal for SSTL15 Standard.(1) | | | | | | | |
| $T_{PSPLLCC}$/ $T_{PHPLLCC}$ | No delay clock-capable clock input and IFF(2) with PLL | XC7Z007S | N/A | 3.03/–0.19 | 3.64/–0.19 | N/A | ns |
| | | XC7Z012S | N/A | 3.15/–0.20 | 3.76/–0.20 | N/A | ns |
| | | XC7Z014S | N/A | 3.17/–0.20 | 3.80/–0.20 | N/A | ns |
| | | XC7Z010 | 2.67/–0.19 | 3.03/–0.19 | 3.64/–0.19 | N/A | ns |
| | | XC7Z015 | 2.78/–0.20 | 3.15/–0.20 | 3.76/–0.20 | N/A | ns |
| | | XC7Z020 | 2.79/–0.20 | 3.17/–0.20 | 3.80/–0.20 | N/A | ns |
| | | XA7Z010 | N/A | N/A | 3.64/–0.19 | 3.64/–0.19 | ns |
| | | XA7Z020 | N/A | N/A | 3.80/–0.20 | 3.80/–0.20 | ns |
| | | XQ7Z020 | N/A | 3.17/–0.20 | 3.80/–0.20 | 3.80/–0.20 | ns |

**Notes:**

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input flip-flop or latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

*Table 82:* **Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin Using BUFIO**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1C/-1I/-1LI | -1Q | |
| Input Setup and Hold Time Relative to a Forwarded Clock Input Pin Using BUFIO for SSTL15 Standard. | | | | | | |
| $T_{PSCS}$/$T_{PHCS}$ | Setup and hold of I/O clock | –0.38/1.39 | –0.38/1.55 | –0.38/1.86 | –0.38/1.86 | ns |

*Table 83:* **Sample Window**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1C/-1I/-1LI | -1Q | |
| $T_{SAMP}$ | Sampling error at receiver pins(1) | 0.59 | 0.64 | 0.70 | 0.70 | ns |
| $T_{SAMP_BUFIO}$ | Sampling error at receiver pins using BUFIO(2) | 0.35 | 0.40 | 0.46 | 0.46 | ns |

**Notes:**

1. This parameter indicates the total sampling error of the PL DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include:
   - CLK0 MMCM jitter
   - MMCM accuracy (phase offset)
   - MMCM phase shift resolution

   These measurements do not include package or clock tree skew.
2. This parameter indicates the total sampling error of the PL DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO clock network and IDELAY to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

## Additional Package Parameter Guidelines

The parameters in this section provide the necessary values for calculating timing budgets for PL clock transmitter and receiver data-valid windows.

*Table 84:* **Package Skew**

| Symbol | Description | Device | Package | Value | Units |
|---|---|---|---|---|---|
| $T_{PKGSKEW}$ | Package skew(1) | XC7Z007S | CLG225 | 101 | ps |
| | | | CLG400 | 155 | ps |
| | | XC7Z012S | CLG485 | 182 | ps |
| | | XC7Z014S | CLG400 | 166 | ps |
| | | | CLG484 | 248 | ps |
| | | XC7Z010 | CLG225 | 101 | ps |
| | | | CLG400 | 155 | ps |
| | | XC7Z015 | CLG485 | 182 | ps |
| | | XC7Z020 | CLG400 | 166 | ps |
| | | | CLG484 | 248 | ps |
| | | XA7Z010 | CLG225 | 101 | ps |
| | | | CLG400 | 155 | ps |
| | | XA7Z020 | CLG400 | 166 | ps |
| | | | CLG484 | 248 | ps |
| | | XQ7Z020 | CL400 | 166 | ps |
| | | | CL484 | 248 | ps |

**Notes:**

1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from die pad to ball.
2. Package delay information is available for these device/package combinations. This information can be used to deskew the package.

# GTP Transceiver Specifications (Only available in the XC7Z012S and XC7Z015)

## GTP Transceiver DC Input and Output Levels

Table 85 summarizes the DC output specifications of the GTP transceivers in the XC7Z012S and XC7Z015. Consult the *7 Series FPGAs GTP Transceiver User Guide* (UG482) for further details.

*Table 85:* **GTP Transceiver DC Specifications**

| Symbol | DC Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $DV_{PPOUT}$ | Differential peak-to-peak output voltage(1) | Transmitter output swing is set to maximum setting | 1000 | – | – | mV |
| $V_{CMOUTDC}$ | DC common mode output voltage | Equation based | $V_{MGTAVTT} - DV_{PPOUT}/4$ | | | mV |
| $R_{OUT}$ | Differential output resistance | | – | 100 | – | Ω |
| $V_{CMOUTAC}$ | Common mode output voltage: AC coupled | | 1/2 $V_{MGTAVTT}$ | | | mV |
| $T_{OSKEW}$ | Transmitter output pair (TXP and TXN) intra-pair skew | | – | – | 12 | ps |
| $DV_{PPIN}$ | Differential peak-to-peak input voltage | External AC coupled | 150 | – | 2000 | mV |
| $V_{IN}$ | Single-ended input voltage(2) | DC coupled $V_{MGTAVTT}$ = 1.2V | –200 | – | $V_{MGTAVTT}$ | mV |
| $V_{CMIN}$ | Common mode input voltage | DC coupled $V_{MGTAVTT}$ = 1.2V | – | 2/3 $V_{MGTAVTT}$ | – | mV |
| $R_{IN}$ | Differential input resistance | | – | 100 | – | Ω |
| $C_{EXT}$ | Recommended external AC coupling capacitor(3) | | – | 100 | – | nF |

**Notes:**

1. The output swing and preemphasis levels are programmable using the attributes discussed in the *7 Series FPGAs GTP Transceiver User Guide* (UG482) and can result in values lower than reported in this table.
2. Voltage measured at the pin referenced to GND.
3. Other values can be used as appropriate to conform to specific protocols and standards.

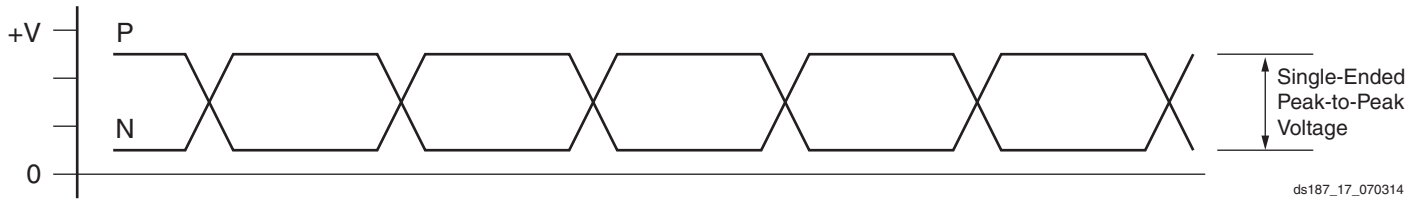


*Figure 20:* **Single-Ended Peak-to-Peak Voltage**

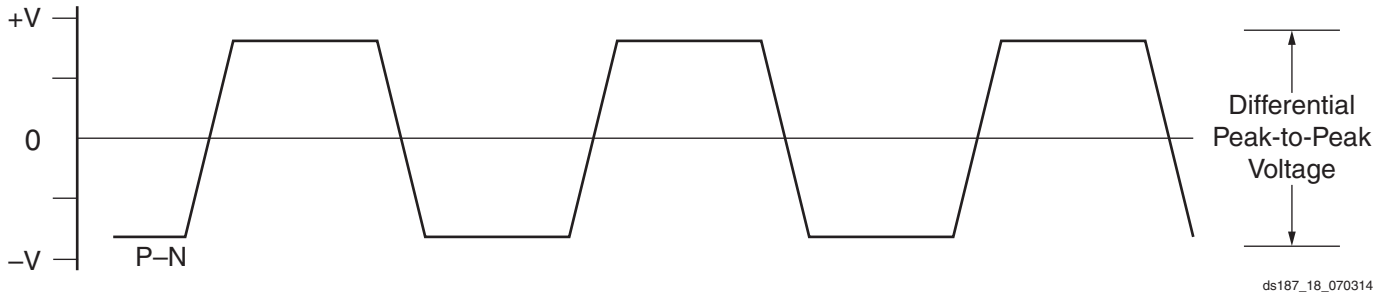


*Figure 21:* **Differential Peak-to-Peak Voltage**

***Note:*** In Figure 21, differential peak-to-peak voltage = single-ended peak-to-peak voltage x 2.

Table 86 summarizes the DC specifications of the clock input of the GTP transceiver. Consult the *7 Series FPGAs GTP Transceiver User Guide* (UG482) for further details.

*Table 86:* **GTP Transceiver Clock DC Input Level Specification**

| Symbol | DC Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $V_{IDIFF}$ | Differential peak-to-peak input voltage | 350 | – | 2000 | mV |
| $R_{IN}$ | Differential input resistance | – | 100 | – | Ω |
| $C_{EXT}$ | Required external AC coupling capacitor | – | 100 | – | nF |

## GTP Transceiver Switching Characteristics

Consult the *7 Series FPGAs GTP Transceiver User Guide* (UG482) for further information.

*Table 87:* **GTP Transceiver Performance**

| Symbol | Description | Output Divider | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | -3 | -2 | -1C/-1I/-1LI | -1Q | |
| $F_{GTPMAX}$ | Maximum GTP transceiver data rate | | 6.25 | 6.25 | 3.75 | N/A | Gb/s |
| $F_{GTPMIN}$ | Minimum GTP transceiver data rate | | 0.500 | 0.500 | 0.500 | N/A | Gb/s |
| $F_{GTPRANGE}$ | PLL line rate range | 1 | 3.2–6.25 | 3.2–6.25 | 3.2–3.75 | N/A | Gb/s |
| | | 2 | 1.6–3.3 | 1.6–3.3 | 1.6–3.2 | N/A | Gb/s |
| | | 4 | 0.8–1.65 | 0.8–1.65 | 0.8–1.6 | N/A | Gb/s |
| | | 8 | 0.5–0.825 | 0.5–0.825 | 0.5–0.8 | N/A | Gb/s |
| $F_{GTPPLLRANGE}$ | GTP transceiver PLL frequency range | | 1.6–3.3 | 1.6–3.3 | 1.6–3.3 | N/A | GHz |

*Table 88:* **GTP Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1C/-1I/-1LI | -1Q | |
| $F_{GTPDRPCLK}$ | GTPDRPCLK maximum frequency | 175 | 175 | 156 | N/A | MHz |

*Table 89:* **GTP Transceiver Reference Clock Switching Characteristics**

| Symbol | Description | Conditions | All Speed Grades | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $F_{GCLK}$ | Reference clock frequency range | | 60 | – | 660 | MHz |
| $T_{RCLK}$ | Reference clock rise time | 20% – 80% | – | 200 | – | ps |
| $T_{FCLK}$ | Reference clock fall time | 80% – 20% | – | 200 | – | ps |
| $T_{DCREF}$ | Reference clock duty cycle | Transceiver PLL only | 40 | – | 60 | % |

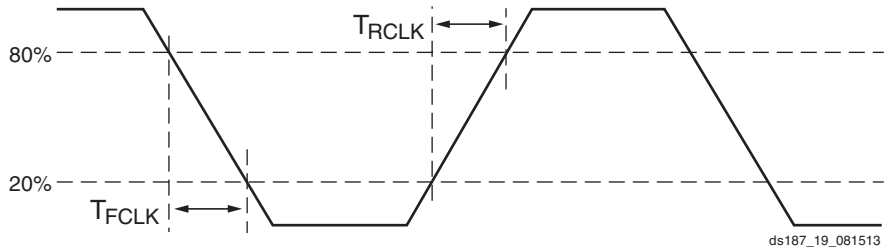


*Figure 22:* **Reference Clock Timing Parameters**

*Table 90:* **GTP Transceiver PLL/Lock Time Adaptation**

| Symbol | Description | Conditions | All Speed Grades | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $T_{LOCK}$ | Initial PLL lock | | – | – | 1 | ms |
| $T_{DLOCK}$ | Clock recovery phase acquisition and adaptation time. | After the PLL is locked to the reference clock, this is the time it takes to lock the clock data recovery (CDR) to the data present at the input. | – | 50,000 | $2.3 \times 10^6$ | UI |

*Table 91:* **GTP Transceiver User Clock Switching Characteristics(1)**

| Symbol | Description | Conditions | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | -3 | -2 | -1C/-1I/-1LI | -1Q | |
| $F_{TXOUT}$ | TXOUTCLK maximum frequency | | 390.625 | 390.625 | 234.375 | N/A | MHz |
| $F_{RXOUT}$ | RXOUTCLK maximum frequency | | 390.625 | 390.625 | 234.375 | N/A | MHz |
| $F_{TXIN}$ | TXUSRCLK maximum frequency | 16-bit data path | 390.625 | 390.625 | 234.375 | N/A | MHz |
| $F_{RXIN}$ | RXUSRCLK maximum frequency | 16-bit data path | 390.625 | 390.625 | 234.375 | N/A | MHz |
| $F_{TXIN2}$ | TXUSRCLK2 maximum frequency | 16-bit data path | 390.625 | 390.625 | 234.375 | N/A | MHz |
| $F_{RXIN2}$ | RXUSRCLK2 maximum frequency | 16-bit data path | 390.625 | 390.625 | 234.375 | N/A | MHz |

**Notes:**

1. Clocking must be implemented as described in the *7 Series FPGAs GTP Transceiver User Guide* (UG482).

*Table 92:* **GTP Transceiver Transmitter Switching Characteristics**

| Symbol | Description | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $F_{GTPTX}$ | Serial data rate range | | 0.500 | – | $F_{GTPMAX}$ | Gb/s |
| $T_{RTX}$ | TX rise time | 20%–80% | – | 50 | – | ps |
| $T_{FTX}$ | TX fall time | 80%–20% | – | 50 | – | ps |
| $T_{LLSKEW}$ | TX lane-to-lane skew(1) | | – | – | 500 | ps |
| $V_{TXOOBVDPP}$ | Electrical idle amplitude | | – | – | 20 | mV |
| $T_{TXOOBTRANSITION}$ | Electrical idle transition time | | – | – | 140 | ns |
| $TJ_{6.25}$ | Total Jitter(2)(3) | 6.25 Gb/s | – | – | 0.30 | UI |
| $DJ_{6.25}$ | Deterministic Jitter(2)(3) | | – | – | 0.15 | UI |
| $TJ_{5.0}$ | Total Jitter(2)(3) | 5.0 Gb/s | – | – | 0.30 | UI |
| $DJ_{5.0}$ | Deterministic Jitter(2)(3) | | – | – | 0.15 | UI |
| $TJ_{4.25}$ | Total Jitter(2)(3) | 4.25 Gb/s | – | – | 0.30 | UI |
| $DJ_{4.25}$ | Deterministic Jitter(2)(3) | | – | – | 0.15 | UI |
| $TJ_{3.75}$ | Total Jitter(2)(3) | 3.75 Gb/s | – | – | 0.30 | UI |
| $DJ_{3.75}$ | Deterministic Jitter(2)(3) | | – | – | 0.15 | UI |
| $TJ_{3.2}$ | Total Jitter(2)(3) | 3.20 Gb/s(4) | – | – | 0.2 | UI |
| $DJ_{3.2}$ | Deterministic Jitter(2)(3) | | – | – | 0.1 | UI |
| $TJ_{3.2L}$ | Total Jitter(2)(3) | 3.20 Gb/s(5) | – | – | 0.32 | UI |
| $DJ_{3.2L}$ | Deterministic Jitter(2)(3) | | – | – | 0.16 | UI |
| $TJ_{2.5}$ | Total Jitter(2)(3) | 2.5 Gb/s(6) | – | – | 0.20 | UI |
| $DJ_{2.5}$ | Deterministic Jitter(2)(3) | | – | – | 0.08 | UI |
| $TJ_{1.25}$ | Total Jitter(2)(3) | 1.25 Gb/s(7) | – | – | 0.15 | UI |
| $DJ_{1.25}$ | Deterministic Jitter(2)(3) | | – | – | 0.06 | UI |
| $TJ_{500}$ | Total Jitter(2)(3) | 500 Mb/s | – | – | 0.1 | UI |
| $DJ_{500}$ | Deterministic Jitter(2)(3) | | – | – | 0.03 | UI |

**Notes:**

1. Using same REFCLK input with TX phase alignment enabled for up to four consecutive transmitters (one fully populated GTP Quad).
2. Using PLL[0/1]_FBDIV = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
3. All jitter values are based on a bit-error ratio of $1e^{-12}$.
4. PLL frequency at 3.2 GHz and TXOUT_DIV = 2.
5. PLL frequency at 1.6 GHz and TXOUT_DIV = 1.
6. PLL frequency at 2.5 GHz and TXOUT_DIV = 2.
7. PLL frequency at 2.5 GHz and TXOUT_DIV = 4.

*Table 93:* **GTP Transceiver Receiver Switching Characteristics**

| Symbol | Description | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $F_{GTPRX}$ | Serial data rate | RX oversampler not enabled | 0.500 | – | $F_{GTPMAX}$ | Gb/s |
| $T_{RXELECIDLE}$ | Time for RXELECIDLE to respond to loss or restoration of data | | – | 10 | – | ns |
| $RX_{OOBVDPP}$ | OOB detect threshold peak-to-peak | | 60 | – | 150 | mV |
| $RX_{SST}$ | Receiver spread-spectrum tracking(1) | Modulated @ 33 KHz | –5000 | – | 5000 | ppm |
| $RX_{RL}$ | Run length (CID) | | – | – | 512 | UI |
| $RX_{PPMTOL}$ | Data/REFCLK PPM offset tolerance | | –1250 | – | 1250 | ppm |
| **SJ Jitter Tolerance(2)** | | | | | | |
| $JT_SJ_{6.25}$ | Sinusoidal Jitter(3) | 6.25 Gb/s | 0.44 | – | – | UI |
| $JT_SJ_{5.0}$ | Sinusoidal Jitter(3) | 5.0 Gb/s | 0.44 | – | – | UI |
| $JT_SJ_{4.25}$ | Sinusoidal Jitter(3) | 4.25 Gb/s | 0.44 | – | – | UI |
| $JT_SJ_{3.75}$ | Sinusoidal Jitter(3) | 3.75 Gb/s | 0.44 | – | – | UI |
| $JT_SJ_{3.2}$ | Sinusoidal Jitter(3) | 3.2 Gb/s(4) | 0.45 | – | – | UI |
| $JT_SJ_{3.2L}$ | Sinusoidal Jitter(3) | 3.2 Gb/s(5) | 0.45 | – | – | UI |
| $JT_SJ_{2.5}$ | Sinusoidal Jitter(3) | 2.5 Gb/s(6) | 0.5 | – | – | UI |
| $JT_SJ_{1.25}$ | Sinusoidal Jitter(3) | 1.25 Gb/s(7) | 0.5 | – | – | UI |
| $JT_SJ_{500}$ | Sinusoidal Jitter(3) | 500 Mb/s | 0.4 | – | – | UI |
| **SJ Jitter Tolerance with Stressed Eye(2)** | | | | | | |
| $JT_TJSE_{3.2}$ | Total Jitter with Stressed Eye(8) | 3.2 Gb/s | 0.70 | – | – | UI |
| $JT_TJSE_{6.25}$ | | 6.25 Gb/s | 0.70 | – | – | UI |
| $JT_SJSE_{3.2}$ | Sinusoidal Jitter with Stressed Eye(8) | 3.2 Gb/s | 0.1 | – | – | UI |
| $JT_SJSE_{6.25}$ | | 6.25 Gb/s | 0.1 | – | – | UI |

**Notes:**

1. Using RXOUT_DIV = 1, 2, and 4.
2. All jitter values are based on a bit error ratio of $1e^{-12}$.
3. The frequency of the injected sinusoidal jitter is 10 MHz.
4. PLL frequency at 3.2 GHz and RXOUT_DIV = 2.
5. PLL frequency at 1.6 GHz and RXOUT_DIV = 1.
6. PLL frequency at 2.5 GHz and RXOUT_DIV = 2.
7. PLL frequency at 2.5 GHz and RXOUT_DIV = 4.
8. Composite jitter.

## GTP Transceiver Protocol Jitter Characteristics

For Table 94 through Table 98, the *7 Series FPGAs GTP Transceiver User Guide* (UG482) contains recommended settings for optimal usage of protocol specific characteristics.

*Table 94:* **Gigabit Ethernet Protocol Characteristics**

| Description | Line Rate (Mb/s) | Min | Max | Units |
|---|---|---|---|---|
| **Gigabit Ethernet Transmitter Jitter Generation** | | | | |
| Total transmitter jitter (T_TJ) | 1250 | – | 0.24 | UI |
| **Gigabit Ethernet Receiver High Frequency Jitter Tolerance** | | | | |
| Total receiver jitter tolerance | 1250 | 0.749 | – | UI |

*Table 95:* **XAUI Protocol Characteristics**

| Description | Line Rate (Mb/s) | Min | Max | Units |
|---|---|---|---|---|
| **XAUI Transmitter Jitter Generation** | | | | |
| Total transmitter jitter (T_TJ) | 3125 | – | 0.35 | UI |
| **XAUI Receiver High Frequency Jitter Tolerance** | | | | |
| Total receiver jitter tolerance | 3125 | 0.65 | – | UI |

*Table 96:* **PCI Express Protocol Characteristics(1)**

| Standard | Description | Line Rate (Mb/s) | Min | Max | Units |
|---|---|---|---|---|---|
| **PCI Express Transmitter Jitter Generation** | | | | | |
| PCI Express Gen 1 | Total transmitter jitter | 2500 | – | 0.25 | UI |
| PCI Express Gen 2 | Total transmitter jitter | 5000 | – | 0.25 | UI |
| **PCI Express Receiver High Frequency Jitter Tolerance** | | | | | |
| PCI Express Gen 1 | Total receiver jitter tolerance | 2500 | 0.65 | – | UI |
| PCI Express Gen 2(2) | Receiver inherent timing error | 5000 | 0.40 | – | UI |
| | Receiver inherent deterministic timing error | | 0.30 | – | UI |

**Notes:**

1. Tested per card electromechanical (CEM) methodology.
2. Using common REFCLK.

*Table 97:* **CEI-6G Protocol Characteristics**

| Description | Line Rate (Mb/s) | Interface | Min | Max | Units |
|---|---|---|---|---|---|
| **CEI-6G Transmitter Jitter Generation** | | | | | |
| Total transmitter jitter(1) | 4976–6375 | CEI-6G-SR | – | 0.3 | UI |
| **CEI-6G Receiver High Frequency Jitter Tolerance** | | | | | |
| Total receiver jitter tolerance(1) | 4976–6375 | CEI-6G-SR | 0.6 | – | UI |

**Notes:**

1. Tested at most commonly used line rate of 6250 Mb/s using 390.625 MHz reference clock.

*Table 98:* **CPRI Protocol Characteristics**

| Description | Line Rate (Mb/s) | Min | Max | Units |
|---|---|---|---|---|
| **CPRI Transmitter Jitter Generation** | | | | |
| Total transmitter jitter | 614.4 | – | 0.35 | UI |
| | 1228.8 | – | 0.35 | UI |
| | 2457.6 | – | 0.35 | UI |
| | 3072.0 | – | 0.35 | UI |
| | 4915.2 | – | 0.3 | UI |
| | 6144.0 | – | 0.3 | UI |
| **CPRI Receiver Frequency Jitter Tolerance** | | | | |
| Total receiver jitter tolerance | 614.4 | 0.65 | – | UI |
| | 1228.8 | 0.65 | – | UI |
| | 2457.6 | 0.65 | – | UI |
| | 3072.0 | 0.65 | – | UI |
| | 4915.2(1) | 0.60 | – | UI |
| | 6144.0(1) | 0.60 | – | UI |

**Notes:**

1. Tested to CEI-6G-SR.

## Integrated Interface Block for PCI Express Designs Switching Characteristics (XC7Z012S and XC7Z015 Only)

This block is only available in the XC7Z012S and XC7Z015. More information and documentation on solutions for PCI Express designs can be found at: www.xilinx.com/technology/protocols/pciexpress.htm.

*Table 99:* **Maximum Performance for PCI Express Designs (XC7Z012S and XC7Z015 only)**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1C/-1I/-1LI | -1Q | |
| $F_{PIPECLK}$ | Pipe clock maximum frequency | 250.00 | 250.00 | 250.00 | N/A | MHz |
| $F_{USERCLK}$ | User clock maximum frequency | 250.00 | 250.00 | 250.00 | N/A | MHz |
| $F_{USERCLK2}$ | User clock 2 maximum frequency | 250.00 | 250.00 | 250.00 | N/A | MHz |
| $F_{DRPCLK}$ | DRP clock maximum frequency | 250.00 | 250.00 | 250.00 | N/A | MHz |

**Notes:**

1. Refer to the *7 Series FPGAs Integrated Block for PCI Express Product Guide* (PG054) for specific supported core configurations.

## XADC Specifications

*Table 100:* **XADC Specifications**

| Parameter | Symbol | Comments/Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{CCADC}$ = 1.8V ± 5%, $V_{REFP}$ = 1.25V, $V_{REFN}$ = 0V, ADCCLK = 26 MHz, –55°C ≤ $T_j$ ≤ 125°C, Typical values at $T_j$=+40°C | | | | | | |
| **ADC Accuracy**(1) | | | | | | |
| Resolution | | | 12 | – | – | Bits |
| Integral Nonlinearity(2) | INL | –40°C ≤ $T_j$ ≤ 100°C | – | – | ±2 | LSBs |
| | | –55°C ≤ $T_j$ < –40°C; 100°C < $T_j$ ≤ 125°C | – | – | ±3 | LSBs |
| Differential Nonlinearity | DNL | No missing codes, guaranteed monotonic | – | – | ±1 | LSBs |
| Offset Error | Unipolar | –40°C ≤ $T_j$ ≤ 100°C | – | – | ±8 | LSBs |
| | | –55°C ≤ $T_j$ < –40°C; 100°C < $T_j$ ≤ 125°C | | | ±12 | LSBs |
| | Bipolar | –55°C ≤ $T_j$ ≤ 125°C | – | – | ±4 | LSBs |
| Gain Error | | | – | – | ±0.5 | % |
| Offset Matching | | | – | – | 4 | LSBs |
| Gain Matching | | | – | – | 0.3 | % |
| Sample Rate | | | – | – | 1 | MS/s |
| Signal to Noise Ratio(2) | SNR | $F_{SAMPLE}$ = 500KS/s, $F_{IN}$ = 20KHz | 60 | – | – | dB |
| RMS Code Noise | | External 1.25V reference | – | – | 2 | LSBs |
| | | On-chip reference | – | 3 | – | LSBs |
| Total Harmonic Distortion(2) | THD | $F_{SAMPLE}$ = 500KS/s, $F_{IN}$ = 20KHz | 70 | – | – | dB |
| **Analog Inputs**(3) | | | | | | |
| ADC Input Ranges | | Unipolar operation | 0 | – | 1 | V |
| | | Bipolar operation | –0.5 | – | +0.5 | V |
| | | Unipolar common mode range (FS input) | 0 | – | +0.5 | V |
| | | Bipolar common mode range (FS input) | +0.5 | – | +0.6 | V |
| Maximum External Channel Input Ranges | | Adjacent analog channels set within these ranges should not corrupt measurements on adjacent channels | –0.1 | – | $V_{CCADC}$ | V |
| Auxiliary Channel Full Resolution Bandwidth | FRBW | | 250 | – | – | KHz |
| **On-Chip Sensors** | | | | | | |
| Temperature Sensor Error | | –40°C ≤ $T_j$ ≤ 100°C | – | – | ±4 | °C |
| | | –55°C ≤ $T_j$ < –40°C; 100°C < $T_j$ ≤ 125°C | – | – | ±6 | °C |
| Supply Sensor Error | | –40°C ≤ $T_j$ ≤ 100°C | – | – | ±1 | % |
| | | –55°C ≤ $T_j$ < –40°C; 100°C < $T_j$ ≤ 125°C | – | – | ±2 | % |
| **Conversion Rate**(4) | | | | | | |
| Conversion Time - Continuous | $t_{CONV}$ | Number of ADCCLK cycles | 26 | – | 32 | Cycles |
| Conversion Time - Event | $t_{CONV}$ | Number of CLK cycles | – | – | 21 | Cycles |
| DRP Clock Frequency | DCLK | DRP clock frequency | 8 | – | 250 | MHz |
| ADC Clock Frequency | ADCCLK | Derived from DCLK | 1 | – | 26 | MHz |
| DCLK Duty Cycle | | | 40 | – | 60 | % |

*Table 100:* **XADC Specifications *(Cont'd)***

| Parameter | Symbol | Comments/Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **XADC Reference**(5) | | | | | | |
| External Reference | $V_{REFP}$ | Externally supplied reference voltage | 1.20 | 1.25 | 1.30 | V |
| On-Chip Reference | | Ground $V_{REFP}$ pin to AGND, $-40°C \le T_j \le 100°C$ | 1.2375 | 1.25 | 1.2625 | V |
| | | Ground $V_{REFP}$ pin to AGND, $-55°C \le T_j < -40°C$; $100°C < T_j \le 125°C$ | 1.225 | 1.25 | 1.275 | V |

**Notes:**

1. Offset and gain errors are removed by enabling the XADC automatic gain calibration feature. The values are specified for when this feature is enabled.
2. Only specified for bitstream option XADCEnhancedLinearity = ON.
3. See the ADC chapter in the *7 Series FPGAs and Zynq-7000 SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide* (UG480) for a detailed description.
4. See the Timing chapter in the *7 Series FPGAs and Zynq-7000 SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide* (UG480) for a detailed description.
5. Any variation in the reference voltage from the nominal $V_{REFP}$ = 1.25V and $V_{REFN}$ = 0V will result in a deviation from the ideal transfer function. This also impacts the accuracy of the internal sensor measurements (i.e., temperature and power supply). However, for external ratiometric type applications allowing reference to vary by ±4% is permitted.

## Configuration Switching Characteristics

*Table 101:* **Configuration Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1C/-1I/-1LI | -1Q | |
| **Power-up Timing Characteristics** | | | | | | |
| $T_{PL}$(1) | Program latency | 5.00 | 5.00 | 5.00 | 5.00 | ms, Max |
| $T_{POR}$ | Power-on reset (50 ms ramp rate time) | 10/50 | 10/50 | 10/50 | 10/50 | ms, Min/Max |
| | Power-on reset (1 ms ramp rate time) with the power-on reset override function disabled; (`devcfg.CTRL.PCFG_POR_CNT_4K = 0`).(2) | 10/35 | 10/35 | 10/35 | 10/35 | ms, Min/Max |
| | Power-on reset (1 ms ramp rate time) with the power-on reset override function enabled; (`devcfg.CTRL.PCFG_POR_CNT_4K = 1`).(2) | 2/8 | 2/8 | 2/8 | 2/8 | ms, Min/Max |
| $T_{PROGRAM}$ | Program pulse width | 250.00 | 250.00 | 250.00 | 250.00 | ns, Min |
| **Boundary-Scan Port Timing Specifications** | | | | | | |
| $T_{TAPTCK}/T_{TCKTAP}$ | TMS and TDI setup/hold | 3.00/2.00 | 3.00/2.00 | 3.00/2.00 | 3.00/2.00 | ns, Min |
| $T_{TCKTDO}$ | TCK falling edge to TDO output | 7.00 | 7.00 | 7.00 | 7.00 | ns, Max |
| $F_{TCK}$ | TCK frequency | 66.00 | 66.00 | 66.00 | 66.00 | MHz, Max |
| **Internal Configuration Access Port** | | | | | | |
| $F_{ICAPCK}$ | Internal configuration access port (ICAPE2) | 100.00 | 100.00 | 100.00 | 100.00 | MHz, Max |
| **Device DNA Access Port** | | | | | | |
| $F_{DNACK}$ | DNA access port (DNA_PORT) | 100.00 | 100.00 | 100.00 | 100.00 | MHz, Max |

**Notes:**

1. To support longer delays in configuration, use the design solutions described in the *7 Series FPGA Configuration User Guide* (UG470).
2. For non-secure boot only. Measurement is made when the PS is already powered and stable, before power cycling the PL.

## eFUSE Programming Conditions

Table 102 lists the programming conditions specifically for eFUSE. For more information, see the *7 Series FPGA Configuration User Guide* (UG470).

*Table 102:* **eFUSE Programming Conditions(1)**

| Symbol | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $I_{PLFS}$ | PL $V_{CCAUX}$ supply current | – | – | 115 | mA |
| $I_{PSFS}$ | PS $V_{CCPAUX}$ supply current | – | – | 115 | mA |
| $t_j$ | Temperature range | 15 | – | 125 | °C |

**Notes:**

1. The Zynq-7000 device must not be configured during eFUSE programming.

## Revision History

The following table shows the revision history for this document:

| Date | Version | Description of Revisions |
|---|---|---|
| 05/07/2012 | 1.0 | Initial Xilinx release. |
| 06/27/2012 | 1.1 | Updated the descriptions, changed $V_{IN}$, Note 3, Note 4, and added $V_{PREF}$ , $V_{PIN}$, and Note 5 in Table 1. In Table 2, updated descriptions and notes. Updated Table 3 and added $R_{IN_TERM}$. Removed $I_{CCMIOQ}$ from Table 5. Removed $I_{CCMIOQ}$ and updated XC7Z020 in Table 6. Updated LVCMOS12, SSTL135, and SSTL15 in Table 10. Updated Table 18.<br>In PS Performance Characteristics section, added timing diagrams and revised many tables.<br>Updated Table 50 and removed notes 2 and 3. Added Note 2 and Note 3 to Table 51. Changed Table 53 by adding $T_{IOIBUFDISABLE}$. Removed many of the combinatorial delay specifications and $T_{CINCK}/T_{CKCIN}$ from Table 62.<br>In Table 100 updated Offset Error and Matching descriptions and Gain Error and Matching descriptions, and added Note 2 to Integral Nonlinearity. |
| 09/12/2012 | 1.2 | Changed Note 3 and added Note 5 in Table 1. Updated $T_j$ in Table 2, also revised Note 4 and Note 9. Updated specifications including $R_{IN_TERM}$ in Table 3. Added Table 4. Updated the XC7Z020 specifications in Table 6. Updated standards in Table 8. Updated specifications in Table 12.<br>Updated the AC Switching Characteristics section for the ISE tools 14.2 speed specifications throughout the document.<br>In PS Performance Characteristics section introduction, revised tables, updated Figure 4, and added Figure 5. Updated parameters in Figure 6 through Figure 13. Updated values in Table 17. Added Note 2 to Table 23. Added Note 3 to Table 36. Updated descriptions and revised $F_{MSPICLK}$ in Table 41.<br>Updated Note 3 in Table 51. Changed $F_{PFDMAX}$ conditions in Table 72 and Table 73. Updated devices and added values to Table 84. |
| 02/11/2013 | 1.3 | Updated the AC Switching Characteristics based upon ISE tools 14.4 and Vivado tools 2012.4, both at v1.05 for the -3, -2, and -1 speed specifications throughout the document. Updated Table 15 and Table 16 to the product status of production for the XC7Z020 devices with -2 and -1 speed specifications.<br>Updated description in Introduction. Revised $V_{PIN}$ in Table 1. Revised $V_{PIN}$ and $I_{IN}$ and added Note 2 to Table 2. Clarified PS specifications, added $C_{PIN}$, and removed Note 3 on $I_{RPD}$ in Table 3. Added values to Table 5. Updated Power Supply Requirements section. Revised descriptions in Table 7. Revised Note 1, removed LVTTL, notes 2 and 3, and added SSTL135 to Table 8. Added Table 9. Removed HSTL_I_12 and SSTL_12 from Table 10. Removed DIFF_SSTL12 from Table 12. Revise in $V_{CCO}$ min/max in Table 13.<br>Many changes to the PS Switching Characteristics section including adding tables, figures, notes with test conditions where applicable. In Table 17, updated the 6:2:1 clock ratio frequencies. Updated minimum value for $T_{ULPIDCK}$ in Table 35. Added a 2:1 memory controller section to Table 51.<br>Updated Note 1 in Table 69. Updated Note 1 and Note 2 in Table 84.Updated the rows on offset error and matching and gain error and matching and the maximum external channel input ranges in Table 100. Added Internal Configuration Access Port section to Table 101. |

| Date | Version | Description of Revisions |
|---|---|---|
| 02/14/2013 | 1.4 | Corrected $T_{QSPICKD2}$ minimum equation in Table 34. Updated timing parameter names in Figure 4 and Figure 5 to match those in the accompanying table. |
| 02/19/2013 | 1.4.1 | Corrected version history. |
| 03/19/2013 | 1.5 | Updated Table 15 and Table 16 to the product status of production for the XC7Z010 devices with -2 and -1 speed specifications.<br>Updated Figure 4 by adding OUT0. Added Note 2 to Table 33. Added Table 38 and Figure 9. |
| 04/24/2013 | 1.6 | All the devices listed in this data sheet are production released. Updated the AC Switching Characteristics based upon ISE tools 14.5 and Vivado tools 2013.1, both at v1.06 for the -3, -2, and -1 speed specifications throughout the document. Updated Table 15 and Table 16 for production release of the XC7Z010 and XC7Z020 in the -3 speed designations.<br>Removed the *PS Power-on Reset* section. Updated the PS—PL Power Sequencing section.<br>In Table 1, revised $V_{IN}$ (I/O input voltage) to match values in Table 4, and combined Note 4 with old Note 5 and then added new Note 6. Revised $V_{IN}$ description and added Note 8 in Table 2. Updated first 3 rows in Table 4. Revised PCI33_3 voltage minimum in Table 10 to match values in Table 1 and Table 4. Added Note 1 to Table 13. Clarified the load conditions in Table 34 by adding new data. Clarified title of Table 51. Throughout the data sheet (Table 62, Table 63, Table 64, and Table 79) removed the obvious note “A Zero “0” Hold Time listing indicates no hold time or a negative hold time.” |
| 07/08/2013 | 1.7 | Added Note 5 to Table 2. Revised the frequency of CPU clock performance (6:2:1) in Table 17. Updated $F_{DDR3L_MAX}$ values in Table 18. Moved and added $F_{AXI_MAX}$ to Table 19. Updated the minimum $T_{DQVALID}$ values in Table 25 and Table 26. In Table 37, corrected the $F_{SDSCLK}$ maximum value. In Table 38, corrected $F_{SDSCLK}$ and fixed the $F_{SDIDCLK}$ typographical unit error. Values in Table 78 and Table 82 were reported incorrectly and have been updated to match speed specifications. |
| 09/12/2013 | 1.8 | Added the XC7Z015 throughout the document. The XC7Z015 is the only device in this data sheet that includes GTP transceivers. Added the GTP transceivers specifications to Table 1, Table 2, and Table 7, and the PL Power-On/Off Power Supply Sequencing, PS—PL Power Sequencing, GTP Transceiver Specifications (Only available in the XC7Z012S and XC7Z015), Integrated Interface Block for PCI Express Designs Switching Characteristics (XC7Z012S and XC7Z015 Only) and sections. Added USRCCLK Output section and clarified values for $T_{POR}$ in Table 101. Added $I_{PSFS}$ to Table 102. Updated Notice of Disclaimer. |
| 11/26/2013 | 1.9 | Added specifications for the XQ7Z020 with the -1Q speed specification/temperature range. Added specifications for the XA7Z010 and XA7Z020 with the -1Q speed specification/temperature range. Removed Note 1 and Note 2 from Table 6. Added Table 14. Updated Table 100 specifications. In Table 101, removed the USRCCLK Output section, added $T_{PL}$, $T_{PROGRAM}$, Note 1, and the Device DNA Access Port section, and updated the $T_{POR}$ description. |
| 01/20/2014 | 1.10 | Update Note 7 in Table 2. Added Note 2 to Table 4. Updated speed files in data sheet and Table 14. Updated Table 15 and Table 16 for production release of the XA7Z010 and XA7Z020 in the -1I and -1Q speed designations. Added I/O standards to Table 52 and improved all of the $T_{IOTP}$ speed specifications. |
| 02/25/2014 | 1.11 | Production release of the XC7Z015 for all speed specifications and temperature ranges, including finalizing information in Table 15 and Table 16. Added XC7Z015 data to Table 5, Table 6, and Table 71. Added Table 27. |
| 07/14/2014 | 1.12 | In Table 4, updated Note 2 per the customer notice *7 Series FPGA and Zynq-7000 AP SoC I/O Undershoot Voltage Data Sheet Update* (XCN14014). Added heading LVDS DC Specifications (LVDS_25). Fixed units for $T_{DQSS}$ in Table 27. Updated heading Input/Output Delay Switching Characteristics. Updated $F_{IDELAYCTRL_REF}$, $T_{IDELAYPAT_JIT}$ and $T_{ODELAYPAT_JIT}$, and Note 1 in Table 60. Removed note from Table 62. Updated description of $T_{ICKOF}$ and added Note 2 to Table 74. Updated description of $T_{ICKOFFAR}$ and added Note 2 to Table 75. Revised $DV_{PPOUT}$ and $V_{IN}$, and added Note 2 to Table 85. Revised labels in Figure 20 and Figure 21 and added a note after Figure 21. Added Note 1 to Table 99. |
| 10/09/2014 | 1.13 | Added -1LI speed grade throughout. Updated Introduction. Removed 3.3V as descriptor of HR I/O banks throughout. In PL Power-On/Off Power Supply Sequencing, added sentence about there being no recommended sequence for supplies not shown. In PS—PL Power Sequencing, removed list of PL power supplies. In Table 20, removed typical value and added maximum value for $T_{RFPSCLK}$. Added note about measurement being taken from $V_{REF}$ to $V_{REF}$ in Table 25 to Table 32. Added I/O Standard Adjustment Measurement Methodology. |

| Date | Version | Description of Revisions |
|---|---|---|
| 11/19/2014 | 1.14 | Added $V_{CCBRAM}$ to Introduction. Replaced -1L speed grade with -1LI and removed 1.0V row for $V_{CCINT}$ and $V_{CCBRAM}$ in Table 2. Updated the AC Switching Characteristics based upon Vivado 2014.4. Updated Vivado software version in Table 14. In Table 15, moved -1LI speed grade for XC7Z010, XC7Z015, and XC7Z020 devices from Advance to Production. In Table 16, added Vivado 2013.1 software version to -2E, -2I, -1C, and -1I speed grades of XC7Z010 and XC7Z020 devices, added Vivado 2014.4 software version to -1LI speed grade for all commercial devices, and removed table note. Added Selecting the Correct Speed Grade and Voltage in the Vivado Tools. Added Note 1 to Table 49. In Table 51, moved LPDDR2 row to end of 2:1 Memory Controllers section. |
| 02/23/2015 | 1.15 | Updated descriptions of $V_{CCPINT}$ in Table 1 and Table 2. Added Note 6 to Table 11. In Table 13, changed maximum $V_{ICM}$ value from 1.425V to 1.500V. Updated Table 22 title. Added Figure 1 and Table 23. In Table 34, updated minimum $T_{QSPIDCK2}$ and $T_{QSPICKD2}$ to 6 ns and 12.5 ns, respectively, and removed note 5. In Table 65, added $T_{RDCK_DI_ECCW}$/$T_{RCKD_DI_ECCW}$ and $T_{RDCK_DI_ECC_FIFO}$/ $T_{RCKD_DI_ECC_FIFO}$, updated $T_{RCCK_EN}$/$T_{RCKC_EN}$ symbols, and updated Note 1. In Table 66, updated $T_{DSPDCK_\{A, B\}_MREG_MULT}$/$T_{DSPCKD_\{A, B\}_MREG_MULT}$ and $T_{DSPDCK_\{A, D\}_ADREG}$/ $T_{DSPCKD_\{A, D\}_ADREG}$ symbols, and replaced B input with A input for $T_{DSPDO_A_P}$. Removed minimum sample rate specification from Table 100. |
| 09/22/2015 | 1.16 | Updated data sheet per the customer notice XCN15034: *Zynq-7000 AP SoC Requirement for the PS Power-Off Sequence*. Assigned quiescent supply currents to -1LI speed grade XQ7Z020 device in Table 5. Updated PS Power-On/Off Power Supply Sequencing. Removed N/A from -1LI speed gradeXQ7Z020 device production software cell in Table 16. Added $F_{SMC_REF_CLK}$ to Table 33. |
| 11/24/2015 | 1.17 | Updated the AC Switching Characteristics based upon Vivado 2015.4. In Table 15, added -1LI speed grade to Production column for XQ7Z020. In Table 16, added Vivado 2015.4 software version to -1LI speed grade column for XQ7Z020. In Figure 4 and Figure 5, added extra clock pulse on QSPI_SCLK_OUT. |
| 07/26/2016 | 1.18 | Updated first sentence in PS Power-On/Off Power Supply Sequencing. Added $T_{PSPOR}$ to Note 1 in Table 22. In Table 54, changed $V_{MEAS}$ for LVCMOS (3.3V), LVTTL (3.3V), and PCI33 (3.3V) to 1.65V. |
| 10/03/2016 | 1.19 | Added XC7Z007S, XC7Z012S, and XC7Z014S throughout. Updated the AC Switching Characteristics based upon Vivado 2016.3. |
| 06/15/2017 | 1.20 | Added 1.35V to Note 7 in Table 2. Updated to Vivado 2016.3 in first paragraph of AC Switching Characteristics. In Table 60, changed $T_{IDELAYRESOLUTION}$ units from ps to µs. |
| 07/02/2018 | 1.20.1 | Editorial updates only. No technical content updates. |

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| Certifications | ISO9001 |
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| Country / Region | Hongkong, China |
| Total Employees | 100 - 200 People |
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