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XC9572XV High-performance CPLD

DS052 (v3.0) June 25, 2007

Product Specification

Note: This product is being discontinued. You cannot order parts after May 14, 2008. Xilinx recommends replacing XC9572XV devices with equivalent XC9572XL devices in all designs as soon as possible. Recommended replacements are pin compatible, however require a V_{CC} change to 3.3V, and a recompile of the design file. In addition, there is no 1.8V I/O support. See **XCN07010** for details regarding this discontinuation, including device replacement recomendations for the XC9572XV CPLD.

Features

- 72 macrocells with 1,600 usable gates
- Available in small footprint packages
  - 44-pin VQFP (34 user I/O pins)
  - 100-pin TQFP (72-user I/O pins)
- Optimized for high-performance 2.5V systems
  - Low power operation
  - Multi-voltage operation
- Advanced system features
  - In-system programmable
  - Superior pin-locking and routability with Fast CONNECT™ II switch matrix
  - Extra wide 54-input Function Blocks
  - Up to 90 product-terms per macrocell with individual product-term allocation
  - Local clock inversion with three global and one product-term clocks
  - Individual output enable per output pin
  - Input hysteresis on all user and boundary-scan pin inputs
  - Bus-hold ciruitry on all user pin inputs
  - Full IEEE Standard 1149.1 boundary-scan (JTAG)
- Fast concurrent programming
- Slew rate control on individual outputs
- Enhanced data security features
- Excellent quality and reliability
  - 20 year data retention
  - ESD protection exceeding 2,000V

Description

The XC9572XV is a 2.5V CPLD targeted for high-performance, low-voltage applications in leading-edge communications and computing systems. It is comprised of four 54V18 Function Blocks, providing 1,600 usable gates with propagation delays of 5 ns.

Power Estimation

Power dissipation in CPLDs can vary substantially depending on the system frequency, design application and output loading. To help reduce power dissipation, each macrocell in a XC9500XV device may be configured for low-power mode (from the default high-performance mode). In addition, unused product-terms and macrocells are automatically deactivated by the software to further conserve power.

For a general estimate of I_{CC}, the following equation may be used:

$$P_{TOTAL} = P_{INT} + P_{IO} = I_{CCINT} \times V_{CCINT} + P_{IO}$$

Separating internal and I/O power here is convenient because XC9500XV CPLDs also separate the corresponding power pins. P_{IO} is a strong function of the load capacitance driven, so it is handled by I = CVf. I_{CCINT} is another situation that reflects the actual design considered and the internal switching speeds. An estimation expression for I_{CCINT} (taken from simulation) is:

$$I_{CCINT}(mA) = MC_{HS}(0.122 \times PT_{HS} + 0.238) + MC_{LP}(0.042 \times PT_{LP} + 0.171) + 0.04(MC_{HS} + MC_{LP}) \times f_{MAX} \times MC_{TOG}$$

where:

MC_{HS} = # macrocells used in high speed mode

MC_{LP} = #macrocells used in low power mode

PT_{HS} = average p-terms used per high speed macrocell

PT_{LP} = average p-terms used over low power macrocell

f_{MAX} = max clocking frequency in the device

MC_{TOG} = % macrocells toggling on each clock (12% is frequently a good estimate

This calculation was derived from laboratory measurements of an XC9500XV part filled with 16-bit counters and allowing a single output (the LSB) to be enabled. The actual I_{CC} value varies with the design application and should be verified during normal system operation. Figure 1 shows the above estimation in a graphical form. For a more detailed discussion of power consumption in this device, see Xilinx application note **XAPP361, "Planning for High Speed XC9500XV Designs."**

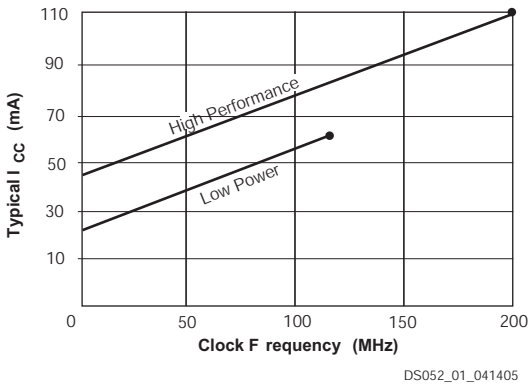

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Figure 1: **Typical ICC vs. Frequency for XC9572XV**

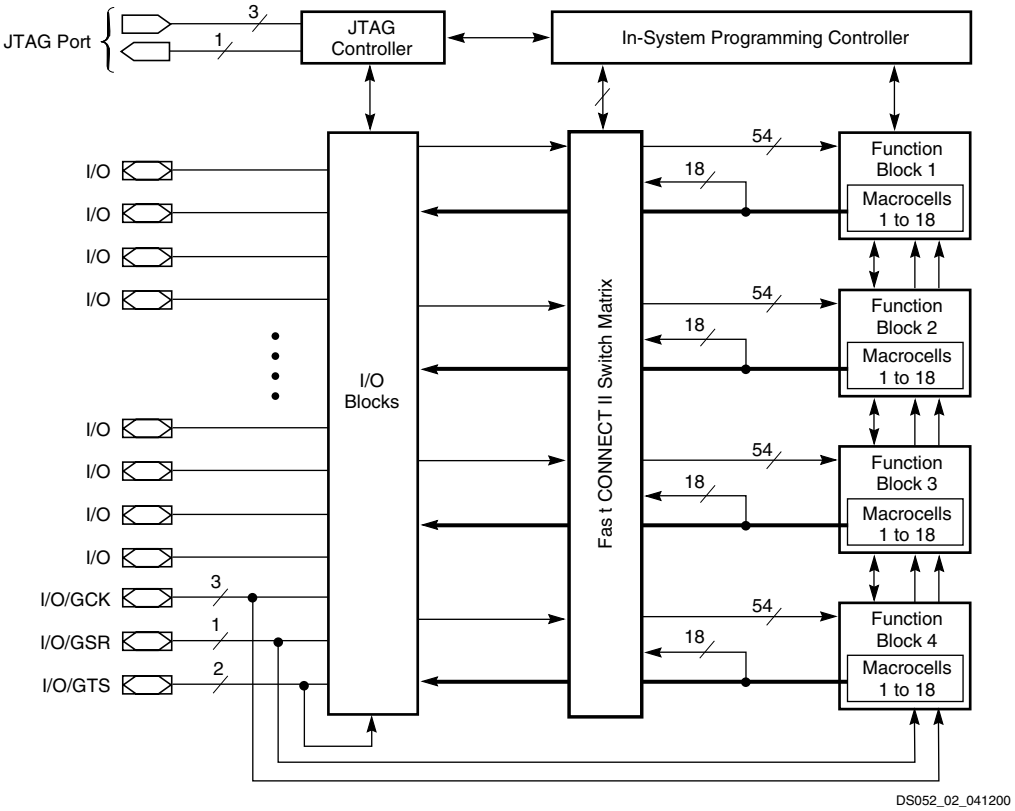

Figure 2: XC9572XV Architecture (Function Block outputs (indicated by the bold line) drive the I/O Blocks directly)

Supported I/O Standards

Table 1: **IOSTANDARD Options**

IOSTANDARD	V_{CCIO}
LVTTL	3.3V
LVCMOS2	2.5V
X25TO18	1.8V

The XC9572XV CPLD features both LVCMOS and LVTTL I/O implementations. See Table 1 for I/O standard voltages.

The LVTTL I/O standard is a general purpose EIA/JEDEC standard for 3.3V applications that use an LVTTL input buffer and Push-Pull output buffer. The LVCMOS2 standard is used in 2.5V applications.

XC9500XV CPLDs are also 1.8V I/O compatible. The X25TO18 setting is provided for generating 1.8V compatible outputs from a CPLD normally operating in a 2.5V environment. The default I/O Standard for pads without IOSTANDARD attributes is LVTTL for XC9500XV devices.

Absolute Maximum Ratings

Symbol	Description	Value	Units
V_{CC}	Supply voltage relative to GND	–0.5 to 2.7	V
V_{CCIO}	Supply voltage for output drivers	–0.5 to 3.6	V
V_{IN}	Input voltage relative to GND(1)	–0.5 to 3.6	V
V_{TS}	Voltage applied to 3-state output(1)	–0.5 to 3.6	V
T_{STG}	Storage temperature (ambient)	–65 to +150	^oC
T_J	Junction temperature	+150	^oC

Notes:

1. Maximum DC undershoot below GND must be limited to either 0.5V or 10 mA, whichever is easier to achieve. During transitions, the device pins may undershoot to –2.0V or overshoot to +3.6V, provided this over- or undershoot lasts less than 10 ns and with the forcing current being limited to 200 mA.
2. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.
3. For solder specifications, see **Xilinx Packaging** .

Recommended Operation Conditions

Symbol	Parameter		Min	Max	Units
V_{CCINT}	Supply voltage for internal logic and input buffers	Commercial T_A = 0^oC to $+70^oC$	2.37	2.62	V
		Industrial T_A = $–40^oC$ to $+85^oC$	2.37	2.62	
V_{CCIO}	Supply voltage for output drivers for 3.3V operation		3.0	3.6	V
	Supply voltage for output drivers for 2.5V operation		2.37	2.62	V
	Supply voltage for output drivers for 1.8V operation		1.71	1.89	V
V_{IL}	Low-level input voltage		0	0.8	V
V_{IH}	High-level input voltage		1.7	3.6	V
V_O	Output voltage		0	V_{CCIO}	V

Quality and Reliability Characteristics

Symbol	Parameter	Min	Max	Units
T_{DR}	Data retention	20	-	Years
N_{PE}	Program/Erase cycles (endurance)	1,000	-	Cycles
V_{ESD}	Electrostatic Discharge (ESD)	2,000	-	Volts

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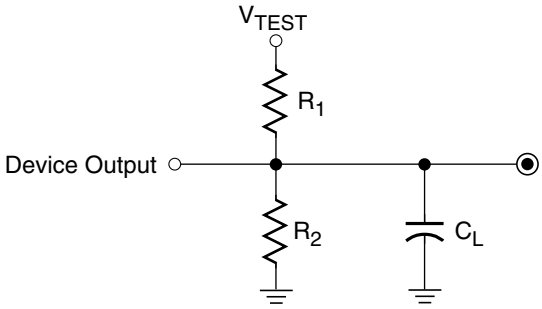
DC Characteristics (Over Recommended Operating Conditions)

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{OH}	Output high voltage for 3.3V outputs	I_{OH} = –4.0 mA	2.4	-	V
	Output high voltage for 2.5V outputs	I_{OH} = –1.0 mA	2.0	-	V
	Output high voltage for 1.8V outputs	I_{OH} = –100 µA	90% V_{CCIO}	-	V
V_{OL}	Output low voltage for 3.3V outputs	I_{OL} = 8.0 mA	-	0.4	V
	Output low voltage for 2.5V outputs	I_{OL} = 1.0 mA	-	0.4	V
	Output low voltage for 1.8V outputs	I_{OL} = 100 µA	-	0.4	V
I_{IL}	Input leakage current	V_{CC} = 2.62V V_{CCIO} = 3.6V V_{IN} = GND or 3.6V	-	±10	µA
I_{IH}	Input high-Z leakage current	V_{CC} = 2.62V V_{CCIO} = 3.6V V_{IN} = GND or 3.6V	-	±10	µA
		V_{CC} min < V_{IN} < 3.6V	-	±150	µA
C_{IN}	I/O capacitance	V_{IN} = GND f = 1.0 MHz	-	10	pF
I_{CC}	Operating Supply Current (low power mode, active)	V_I = GND, No load f = 1.0 MHz	14		mA

AC Characteristics

Symbol	Parameter	XC9572XV-5		XC9572XV-7		Units
		Min	Max	Min	Max	
T_{PD}	I/O to output valid	-	5.0	-	7.5	ns
T_{SU}	I/O setup time before GCK	3.5	-	4.8	-	ns
T_H	I/O hold time after GCK	0	-	0	-	ns
T_{CO}	GCK to output valid	-	3.5	-	4.5	ns
f_{SYSTEM}	Multiple FB internal operating frequency	-	222.2	-	125.0	MHz
T_{PSU}	I/O setup time before p-term clock input	1.0	-	1.6	-	ns
T_{PH}	I/O hold time after p-term clock input	2.5	-	3.2	-	ns
T_{PCO}	P-term clock output valid	-	6.0	-	7.7	ns
T_{OE}	GTS to output valid	-	4.0	-	5.0	ns
T_{OD}	GTS to output disable	-	4.0	-	5.0	ns
T_{POE}	Product term OE to output enabled	-	7.0	-	9.5	ns
T_{POD}	Product term OE to output disabled	-	7.0	-	9.5	ns
T_{AO}	GSR to output valid	-	10.0	-	12.0	ns
T_{PAO}	P-term S/R to output valid	-	10.7	-	12.6	ns
T_{WLH}	GCK pulse width (High or Low)	2.2	-	4.0	-	ns
T_{PLH}	P-term clock pulse width (High or Low)	5.0	-	6.5	-	ns
T_{APRPW}	Asynchronous preset/reset pulse width (High or Low)	5.0	-	6.5	-	ns

Internal Timing Parameters



Output Type	V_{CCIO}	V_{TEST}	R_1	R_2	C_L
	3.3V	3.3V	320Ω	360Ω	35 pF
	2.5V	2.5V	250Ω	660Ω	35 pF
	1.8V	1.8V	10KΩ	14KΩ	35 pF

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Figure 3: **AC Load Circuit**

Symbol	Parameter	XC9572XV-5		XC9572XV-7		Units
		Min	Max	Min	Max	
Buffer Delays						
T_{IN}	Input buffer delay	-	2.0	-	2.3	ns
T_{GCK}	GCK buffer delay	-	1.2	-	1.5	ns
T_{GSR}	GSR buffer delay	-	2.0	-	3.1	ns
T_{GTS}	GTS buffer delay	-	4.0	-	5.0	ns
T_{OUT}	Output buffer delay	-	2.1	-	2.5	ns
T_{EN}	Output buffer enable/disable delay	-	0	-	0	ns
Product Term Control Delays						
T_{PTCK}	Product term clock delay	-	1.7	-	2.4	ns
T_{PTSR}	Product term set/reset delay	-	0.7	-	1.4	ns
T_{PTTS}	Product term 3-state delay	-	5.0	-	7.2	ns
Internal Register and Combinatorial Delays						
T_{PDI}	Combinatorial logic propagation delay	-	0.2	-	1.3	ns
T_{SUI}	Register setup time	2.0	-	2.6	-	ns
T_{HI}	Register hold time	1.5	-	2.2	-	ns
T_{ECSU}	Register clock enable setup time	2.0	-	2.6	-	ns
T_{ECHO}	Register clock enable hold time	1.5	-	2.2	-	ns
T_{COI}	Register clock to output valid time	-	0.2	-	0.5	ns
T_{AOI}	Register async. S/R to output delay	-	5.9	-	6.4	ns
T_{RAI}	Register async. S/R recover before clock	5.0		7.5		ns
T_{LOGI}	Internal logic delay	-	0.7	-	1.4	ns
T_{LOGILP}	Internal low power logic delay	-	5.7	-	6.4	ns
Feedback Delays						
T_F	Fast CONNECT II feedback delay	-	1.6	-	3.5	ns
Time Adders						
T_{PTA}	Incremental product term allocator delay	-	0.7	-	0.8	ns
T_{PTA2}	Adjacent macrocell p-term allocator delay	-	0.3	-	0.3	ns
T_{SLEW}	Slew-rate limited delay	-	3.0	-	4.0	ns

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XC9572XV I/O Pins

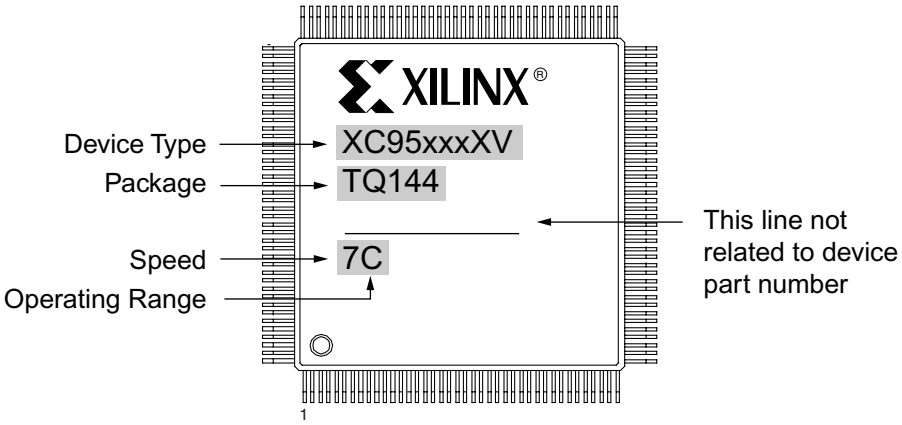
Function Block	Macro-cell	VQ44	TQ100	BScan Order	Function Block	Macro-cell	VQ44	TQ100	BScan Order
1	1	-	16	213	3	1	-	41	105
1	2	39	13	210	3	2	5	32	102
1	3	-	18	207	3	3	-	49	99
1	4	-	20	204	3	4	-	50	96
1	5	40	14	201	3	5	6	35	93
1	6	41	15	198	3	6	-	53	90
1	7	-	25	195	3	7	-	54	87
1	8	42	17	192	3	8	7	37	84
1	9	43(1)	22(1)	189	3	9	8	42	81
1	10	-	28	186	3	10	-	60	78
1	11	44(1)	23(1)	183	3	11	12	52	75
1	12	-	33	180	3	12	-	61	72
1	13	-	36	177	3	13	-	63	69
1	14	1(1)	27(1)	174	3	14	13	55	66
1	15	2	29	171	3	15	14	56	63
1	16	-	39	168	3	16	18	64	60
1	17	3	30	165	3	17	16	58	57
1	18	-	40	162	3	18	-	59	54
2	1	-	87	159	4	1	-	65	51
2	2	29	94	156	4	2	19	67	48
2	3	-	91	153	4	3	-	71	45
2	4	-	93	150	4	4	-	72	42
2	5	30	95	147	4	5	20	68	39
2	6	31	96	144	4	6	-	76	36
2	7	-	3(2)	141	4	7	-	77	33
2	8	32	97	138	4	8	21	70	30
2	9	33(1)	99(1)	135	4	9	-	66	27
2	10	-	1	132	4	10	-	81	24
2	11	34(1)	4(1)	129	4	11	22	74	21
2	12	-	6	126	4	12	-	82	18
2	13	-	8	123	4	13	-	85	15
2	14	36(3)	9(3)	120	4	14	23	78	12
2	15	37	11	117	4	15	27	89	9
2	16	-	10	114	4	16	-	86	6
2	17	38	12	111	4	17	28	90	3
2	18	-	92	108	4	18	-	79	0

Notes:
1. Global control pin.
2. GTS1 for TQ100
3. GTS1 for VQ44

XC9572XV Global, JTAG and Power Pins

Pin Type	VQ44	TQ100
I/O/GCK1	43	22
I/O/GCK2	44	23
I/O/GCK3	1	27
I/O/GTS1	36	3
I/O/GTS2	34	4
I/O/GSR	33	99
TCK	11	48
TDI	9	45
TDO	24	83
TMS	10	47
V_{CCINT} 2.5V	15, 35	5, 57, 98
V_{CCIO} 1.8/2.5V/3.3V	26	26, 38, 51, 88
GND	4, 17, 25	21, 31, 44, 62, 69, 75, 84, 100
No Connects	-	2, 7, 19, 24, 34, 43, 46, 73, 80

Device Part Marking and Ordering Combination Information



Sample package with part marking.

Notes:

1. Due to the small size of chip scale packages, part marking on these packages does not follow the above sample and the complete part number cannot be included in the marking. Part marking on chip scale packages by line:
   - Line 1 = X (Xilinx logo), then truncated part number (no XC), i.e., 95xxxXV.
   - Line 2 = Not related to device part number.
   - Line 3 = Not related to device part number.
   - Line 4 = Package code, speed, operating temperature, three digits not related to device part number. Package code: C1 = CS48.

Device Ordering and Part Marking Number	Speed (pin-to-pin delay)	Pkg. Symbol	No. of Pins	Package Type	Operating Range(1)
XC9572XV-5VQ44C	5 ns	VQ44	44-pin	Quad Flat Pack (VQFP)	C
XC9572XV-5TQ100C	5 ns	TQ100	100-pin	Thin Quad Flat Pack (TQFP)	C
XC9572XV-7VQ44C	7.5 ns	VQ44	44-pin	Quad Flat Pack (VQFP)	C
XC9572XV-7TQ100C	7.5 ns	TQ100	100-pin	Thin Quad Flat Pack (TQFP)	C
XC9572XV-7VQ44I	7.5 ns	VQ44	44-pin	Quad Flat Pack (VQFP)	I
XC9572XV-7TQ100I	7.5 ns	TQ100	100-pin	Thin Quad Flat Pack (TQFP)	I

Notes:

1. C = Commercial: T_A = 0° to +70°C; I = Industrial: T_A = –40° to +85°C
2. Some packages available in Pb-free option. See **Xilinx Packaging** for more information.

Revision History

Date	Revision No.	Description
02/01/00	1.1	Initial Xilinx release. Advance information specification.
01/29/01	2.0	Added -4 performance specification and VQ44 pagkage. Deleted VQ64 package. Updated I_{CC} vs. Frequency Figure 1.
05/15/01	2.1	Updated I_{CC} formula, Recommended Operation Conditions, -4 and -5 AC Characteristics and Internal Timing Parameters
08/27/01	2.2	Changed V_{CCIO} 3.3V from 3.13 to 3.0 (min), 3.46 to 3.60 (max); DC characteristics: I_{IL} - added "low" current, I_{IH} - changed to "Input leakage high current"; Internal Timing: -5 T_{AOI} from 6.5 to 5.9.
05/31/02	2.3	Updated I_{CC} equation on page 1. Updated Component Availability Chart. Changed to Preliminary. Added second test condition and max measurement to I_{IH} DC Characteristics. Added Part Marking Information to Ordering Information. Removed the -4 device.
06/18/03	2.4	Updated T_{SOL} from 260 to 220°C. Updated Device Part Marking.
08/21/03	2.5	Updated Package Device Marking Pin 1 orientation.
04/15/05	2.6	Added T_{APRPW} specification to AC Characteristics. Added IOSTANDARD information.
01/16/06	2.7	Removed PC44 and CS48 packages as per **XCN05020**.
06/25/07	3.0	Notice of discontinuance.

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OUR CERTIFICATE

A long-term cooperative relationship can be built between global customers and us by providing excellent products

Business Type	Trading Company, Distributor/Wholesaler
Main Products	Electronic Integrated Circuit
Certifications	ISO9001
Total Annual Revenue	US$2.5 Million - US$5 Million
Country / Region	Hongkong, China
Total Employees	100 - 200 People
Year Established	2018
Main Markets	North America South Asia Western Europe

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