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Zynq UltraScale+ MPSoC Data Sheet: DC and AC Switching Characteristics

DS925 (v1.17) March 13, 2020

Product Specification

Summary

The Xilinx® Zynq® UltraScale+™ MPSoCs are available in -3, -2, -1 speed grades, with -3E devices having the highest performance. The -2LE and -1LI devices can operate at a V_{CCINT} voltage at 0.85V or 0.72V and are screened for lower maximum static power. When operated at $V_{CCINT} = 0.85V$, using -2LE and -1LI devices, the speed specification for the L devices is the same as the -2I or -1I speed grades. When operated at $V_{CCINT} = 0.72V$, the -2LE and -1LI performance and static and dynamic power is reduced.

DC and AC characteristics are specified in extended (E), industrial (I), automotive (Q), and military (M) temperature ranges. Except the operating temperature range or unless otherwise noted, all the DC and AC electrical parameters are the same for a particular speed grade (that is, the timing characteristics of a -1 speed grade extended device are the same as for a -1 speed grade industrial device). However, only selected speed grades and/or devices are available in each temperature range.

The XQ references in this data sheet are specific to the devices available in XQ Ruggedized packages. See the *Defense-Grade UltraScale Architecture Data Sheet: Overview (DS895)* for further information on XQ Defense-grade part numbers, packages, and ordering information.

All supply voltage and junction temperature specifications are representative of worst-case conditions. The parameters included are common to popular designs and typical applications.

This data sheet, part of an overall set of documentation on the Zynq UltraScale+ MPSoCs, is available on the Xilinx website at www.xilinx.com/documentation.

DC Characteristics

Absolute Maximum Ratings

Table 1: Absolute Maximum Ratings

| Symbol | Description ¹ | Min | Max | Units |
|------------------------------|---|--------|-------|-------|
| Processor System (PS) | | | | |
| $V_{CC_PSINTFP}$ | PS primary logic full-power domain supply voltage | -0.500 | 1.000 | V |
| $V_{CC_PSINTLP}$ | PS primary logic low-power domain supply voltage | -0.500 | 1.000 | V |
| V_{CC_PSAUX} | PS auxiliary supply voltage | -0.500 | 2.000 | V |

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Table 1: Absolute Maximum Ratings (cont'd)

| Symbol | Description ¹ | Min | Max | Units |
|---|---|--------|--------------------------------|-------|
| V _{CC_PSINTFP_DDR} | PS DDR controller and PHY supply voltage | -0.500 | 1.000 | V |
| V _{CC_PSADC} | PS SYSMON ADC supply voltage relative to GND_PSADC | -0.500 | 2.000 | V |
| V _{CC_PSPLL} | PS PLL supply voltage | -0.500 | 1.320 | V |
| V _{PS_MGTRAVCC} | PS-GTR supply voltage | -0.500 | 1.000 | V |
| V _{PS_MGTRAVTT} | PS-GTR termination voltage | -0.500 | 2.000 | V |
| V _{PS_MGTREFCLK} | PS-GTR reference clock input voltage | -0.500 | 1.100 | V |
| V _{PS_MGTRIN} | PS-GTR receiver input voltage | -0.500 | 1.100 | V |
| V _{CCO_PSDDR} | PS DDR I/O supply voltage | -0.500 | 1.650 | V |
| V _{CC_PSDDR_PLL} | PS DDR PLL supply voltage | -0.500 | 2.000 | V |
| V _{CCO_PSIO} | PS I/O supply | -0.500 | 3.630 | V |
| V _{PSIN} ² | PS I/O input voltage | -0.500 | V _{CCO_PSIO} + 0.550 | V |
| | PS DDR I/O input voltage | -0.500 | V _{CCO_PSDDR} + 0.550 | V |
| V _{CC_PSBATT} | PS battery-backed RAM and battery-backed real-time clock (RTC) supply voltage | -0.500 | 2.000 | V |
| Programmable Logic (PL) | | | | |
| V _{CCINT} | Internal supply voltage | -0.500 | 1.000 | V |
| V _{CCINT_IO} ³ | Internal supply voltage for the I/O banks | -0.500 | 1.000 | V |
| V _{CCAUX} | Auxiliary supply voltage | -0.500 | 2.000 | V |
| V _{CCBRAM} | Supply voltage for the block RAM memories | -0.500 | 1.000 | V |
| V _{CCO} | Output drivers supply voltage for HD I/O banks | -0.500 | 3.400 | V |
| | Output drivers supply voltage for HP I/O banks | -0.500 | 2.000 | V |
| V _{CCAUX_IO} ⁴ | Auxiliary supply voltage for the I/O banks | -0.500 | 2.000 | V |
| V _{REF} | Input reference voltage | -0.500 | 2.000 | V |
| V _{IN} ^{2, 5, 6} | I/O input voltage for HD I/O banks | -0.550 | V _{CCO} + 0.550 | V |
| | I/O input voltage for HP I/O banks | -0.550 | V _{CCO} + 0.550 | V |
| I _{DC} | Available output current at the pad | -20 | 20 | mA |
| I _{RMS} | Available RMS output current at the pad | -20 | 20 | mA |
| GTH or GTY Transceiver⁷ | | | | |
| V _{MGTA VCC} | Analog supply voltage for transceiver circuits | -0.500 | 1.000 | V |
| V _{MGTA VTT} | Analog supply voltage for transceiver termination circuits | -0.500 | 1.300 | V |
| V _{MGTVCCAUX} | Auxiliary analog Quad PLL (QPLL) voltage supply for transceivers | -0.500 | 1.900 | V |
| V _{MGTA VREFCLK} | Transceiver reference clock absolute input voltage | -0.500 | 1.300 | V |
| V _{MGTA VTRCAL} | Analog supply voltage for the resistor calibration circuit of the transceiver column | -0.500 | 1.300 | V |
| V _{IN} | Receiver (RXP/RXN) and transmitter (TXP/TXN) absolute input voltage | -0.500 | 1.200 | V |
| I _{DCIN-FLOAT} | DC input current for receiver input pins DC coupled RX termination = floating ⁸ | - | 10 | mA |
| I _{DCIN-MGTA VTT} | DC input current for receiver input pins DC coupled RX termination = V _{MGTA VTT} | - | 10 | mA |
| I _{DCIN-GND} | DC input current for receiver input pins DC coupled RX termination = GND ⁹ | - | 0 | mA |
| I _{DCIN-PROG} | DC input current for receiver input pins DC coupled RX termination = programmable ¹⁰ | - | 0 | mA |

Table 1: Absolute Maximum Ratings (cont'd)

| Symbol | Description ¹ | Min | Max | Units |
|---------------------------------|--|--------|-------|-------|
| I _{DCOUT-FLOAT} | DC output current for transmitter pins DC coupled RX termination = floating | - | 6 | mA |
| I _{DCOUT-MGTAVTT} | DC output current for transmitter pins DC coupled RX termination = V _{MGTAVTT} | - | 6 | mA |
| Video Codec Unit | | | | |
| V _{CCINT_VCU} | Internal supply voltage for the video codec unit | -0.500 | 1.000 | V |
| PL System Monitor | | | | |
| V _{CCADC} | PL System Monitor supply relative to GNDADC | -0.500 | 2.000 | V |
| V _{REFP} | PL System Monitor reference input relative to GNDADC | -0.500 | 2.000 | V |
| Temperature¹¹ | | | | |
| T _{STG} | Storage temperature (ambient) | -65 | 150 | °C |
| T _{SOL} | Maximum dry rework soldering temperature | - | 260 | °C |
| | Maximum reflow soldering temperature for SBVB484, SFVA625, and SFVC784 packages | - | 250 | °C |
| | Maximum reflow soldering temperature for FBVB900, FFVC900, FFVB1156, FFVC1156, FFVB1517, FFVF1517, FFVC1760, FFVD1760, and FFVE1924 packages | - | 245 | °C |
| | Maximum reflow soldering temperature for SFRA484, SFRC784, FFRB900, FFRC900, FFRB1156, FFRC1156, FFRB1517, and FFRC1760 packages | - | 225 | °C |
| T _j | Maximum junction temperature | - | 125 | °C |

Notes:

- Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
- When operating outside of the recommended operating conditions, refer to [Table 6](#), [Table 7](#), and [Table 8](#) for maximum overshoot and undershoot specifications.
- V_{CCINT_IO} must be connected to V_{CCBRAM}.
- V_{CCAUX_IO} must be connected to V_{CCAUX}.
- The lower absolute voltage specification always applies.
- For I/O operation, see the *UltraScale Architecture SelectIO Resources User Guide (UG571)*.
- For more information on supported GTH or GTY transceiver terminations see the *UltraScale Architecture GTH Transceivers User Guide (UG576)* or *UltraScale Architecture GTY Transceivers User Guide (UG578)*.
- AC coupled operation is not supported for RX termination = floating.
- For GTY transceivers, DC coupled operation is not supported for RX termination = GND.
- DC coupled operation is not supported for RX termination = programmable.
- For soldering guidelines and thermal considerations, see the *Zynq UltraScale+ Device Packaging and Pinouts Product Specification User Guide (UG1075)*.

Recommended Operating Conditions

Table 2: Recommended Operating Conditions

| Symbol | Description ^{1,2} | Min | Typ | Max | Units |
|--|--|--------|-------|--------------------------------|-------|
| Processor System | | | | | |
| V _{CC_PSINTFP} ³ | PS full-power domain supply voltage | 0.808 | 0.850 | 0.892 | V |
| | For -1LI and -2LE (V _{CCINT} = 0.72V) devices: PS full-power domain supply voltage | 0.808 | 0.850 | 0.892 | V |
| | For -3E devices: PS full-power domain supply voltage | 0.873 | 0.900 | 0.927 | V |
| V _{CC_PSINTLP} | PS low-power domain supply voltage | 0.808 | 0.850 | 0.892 | V |
| | For -1LI and -2LE (V _{CCINT} = 0.72V) devices: PS low-power domain supply voltage | 0.808 | 0.850 | 0.892 | V |
| | For -3E devices: PS low-power domain supply voltage | 0.873 | 0.900 | 0.927 | V |
| V _{CC_PSAUX} | PS auxiliary supply voltage | 1.710 | 1.800 | 1.890 | V |
| V _{CC_PSINTFP_DDR} ³ | PS DDR controller and PHY supply voltage | 0.808 | 0.850 | 0.892 | V |
| | For -1LI and -2LE (V _{CCINT} = 0.72V) devices: PS DDR controller and PHY supply voltage | 0.808 | 0.850 | 0.892 | V |
| | For -3E devices: PS DDR controller and PHY supply voltage | 0.873 | 0.900 | 0.927 | V |
| V _{CC_PSADC} | PS SYSMON ADC supply voltage relative to GND_PSADC | 1.710 | 1.800 | 1.890 | V |
| V _{CC_PSPLL} | PS PLL supply voltage | 1.164 | 1.200 | 1.236 | V |
| V _{PS_MGTRAVCC} ⁴ | PS-GTR supply voltage | 0.825 | 0.850 | 0.875 | V |
| V _{PS_MGTRAVTT} ⁴ | PS-GTR termination voltage | 1.746 | 1.800 | 1.854 | V |
| V _{CCO_PSDDR} ⁵ | PS DDR I/O supply voltage | 1.06 | - | 1.575 | V |
| V _{CC_PSDDR_PLL} | PS DDR PLL supply voltage | 1.710 | 1.800 | 1.890 | V |
| V _{CCO_PSIO} ⁶ | PS I/O supply | 1.710 | - | 3.465 | V |
| V _{PSIN} | PS I/O input voltage | -0.200 | - | V _{CCO_PSIO} + 0.200 | V |
| | PS DDR I/O input voltage | -0.200 | - | V _{CCO_PSDDR} + 0.200 | V |
| V _{CC_PSBATT} ⁷ | PS battery-backed RAM and battery-backed real-time clock (RTC) supply voltage | 1.200 | - | 1.500 | V |
| Programmable Logic | | | | | |
| V _{CCINT} | PL internal supply voltage | 0.825 | 0.850 | 0.876 | V |
| | For -1LI and -2LE (V _{CCINT} = 0.72V) devices: PL internal supply voltage | 0.698 | 0.720 | 0.742 | V |
| | For -3E devices: PL internal supply voltage | 0.873 | 0.900 | 0.927 | V |
| V _{CCINT_IO} ⁸ | PL internal supply voltage for the I/O banks | 0.825 | 0.850 | 0.876 | V |
| | For -1LI and -2LE (V _{CCINT} = 0.72V) devices: PL internal supply voltage for the I/O banks | 0.825 | 0.850 | 0.876 | V |
| | For -3E devices: PL internal supply voltage for the I/O banks | 0.873 | 0.900 | 0.927 | V |
| V _{CCBRAM} | Block RAM supply voltage | 0.825 | 0.850 | 0.876 | V |
| | For -3E devices: block RAM supply voltage | 0.873 | 0.900 | 0.927 | V |
| V _{CCAUX} | Auxiliary supply voltage | 1.746 | 1.800 | 1.854 | V |
| V _{CCO'} ⁹ | Supply voltage for HD I/O banks | 1.140 | - | 3.400 | V |
| | Supply voltage for HP I/O banks | 0.950 | - | 1.900 | V |
| V _{CCAUX_IO} ¹⁰ | Auxiliary I/O supply voltage | 1.746 | 1.800 | 1.854 | V |
| V _{IN} ¹¹ | I/O input voltage | -0.200 | - | V _{CCO} + 0.200 | V |

Table 2: Recommended Operating Conditions (cont'd)

| Symbol | Description ^{1,2} | Min | Typ | Max | Units |
|-------------------------------|--|-------|-------|-------|-------|
| I_{IN}^{12} | Maximum current through any PL or PS pin in a powered or unpowered bank when forward biasing the clamp diode | - | - | 10 | mA |
| GTH or GTY Transceiver | | | | | |
| $V_{MGTAVCC}^{13}$ | Analog supply voltage for the GTH or GTY transceiver | 0.873 | 0.900 | 0.927 | V |
| $V_{MGTAVTT}^{13}$ | Analog supply voltage for the GTH or GTY transmitter and receiver termination circuits | 1.164 | 1.200 | 1.236 | V |
| $V_{MGTVCCAUX}^{13}$ | Auxiliary analog QPLL voltage supply for the transceivers | 1.746 | 1.800 | 1.854 | V |
| $V_{MGTAVTTRCAL}^{13}$ | Analog supply voltage for the resistor calibration circuit of the GTH or GTY transceiver column | 1.164 | 1.200 | 1.236 | V |
| VCU | | | | | |
| V_{CCINT_VCU} | Internal supply voltage for the VCU | 0.873 | 0.900 | 0.927 | V |
| PL System Monitor | | | | | |
| V_{CCADC} | PL System Monitor supply relative to GNDADC | 1.746 | 1.800 | 1.854 | V |
| V_{REFP} | PL System Monitor externally supplied reference voltage relative to GNDADC | 1.200 | 1.250 | 1.300 | V |
| Temperature | | | | | |
| T_j^{14} | Junction temperature operating range for extended (E) temperature devices ¹⁵ | 0 | - | 100 | °C |
| | Junction temperature operating range for industrial (I) temperature devices | -40 | - | 100 | °C |
| | Junction temperature operating range for automotive (Q) temperature devices | -40 | - | 125 | °C |
| | Junction temperature operating range for military (M) temperature devices | -55 | - | 125 | °C |
| | Junction temperature operating range for eFUSE programming | -40 | - | 125 | °C |

Notes:

- All voltages are relative to GND.
- For the design of the power distribution system consult the *UltraScale Architecture PCB Design User Guide (UG583)*.
- $V_{CC_PSINTFP_DDR}$ must be tied to $V_{CC_PSINTFP}$.
- Each voltage listed requires filtering as described in the *UltraScale Architecture PCB Design User Guide (UG583)*.
- Includes V_{CCO_PSDDR} of 1.2V, 1.35V, 1.5V at $\pm 5\%$ and 1.1V $+0.07V/-0.04V$ depending upon the tolerances required by specific memory standards.
- Applies to all PS I/O supply banks. Includes V_{CCO_PSIO} of 1.8V, 2.5V, and 3.3V at $\pm 5\%$.
- If the battery-backed RAM or RTC is not used, connect V_{CC_PSBATT} to GND or V_{CC_PSAUX} . The V_{CC_PSAUX} maximum of 1.89V is acceptable on an unused V_{CC_PSBATT} .
- V_{CCINT_IO} must be connected to V_{CCBRAM} .
- Includes V_{CCO} of 1.0V (HP I/O only), 1.2V, 1.35V, 1.5V, 1.8V, 2.5V (HD I/O only) at $\pm 5\%$, and 3.3V (HD I/O only) at $+3/-5\%$.
- V_{CCAUX_IO} must be connected to V_{CCAUX} .
- The lower absolute voltage specification always applies.
- A total of 200 mA per bank should not be exceeded.
- Each voltage listed requires filtering as described in the *UltraScale Architecture GTH Transceivers User Guide (UG576)* or the *UltraScale Architecture GTY Transceivers User Guide (UG578)*.
- Xilinx recommends measuring the T_j of a device using the system monitor as described in the *UltraScale Architecture System Monitor User Guide (UG580)*. The SYSMON temperature measurement errors (that are described in [Table 69](#) and [Table 126](#)) must be accounted for in your design. For example, when using the PL system monitor with an external reference of 1.25V, and when SYSMON reports 97°C, there is a measurement error $\pm 3^\circ\text{C}$. A reading of 97°C is considered the maximum adjusted T_j ($100^\circ\text{C} - 3^\circ\text{C} = 97^\circ\text{C}$).
- Devices labeled with the speed/temperature grade of -2LE can operate for a limited time at a junction temperature between 100°C and 110°C. Timing parameters adhere to the same speed file at 110°C as they do below 110°C, regardless of operating voltage (nominal voltage of 0.85V or a low-voltage of 0.72V). Operation up to $T_j = 110^\circ\text{C}$ is limited to 1% of the device lifetime and can occur sequentially or at regular intervals as long as the total time does not exceed 1% of the device lifetime.

Available Speed Grades and Operating Voltages

Table 3 describes the speed grades per device and the V_{CCINT} operating supply voltages for the full-power, low-power, and DDR domains. For more information on selecting devices and speed grades, see the *UltraScale Architecture and Product Data Sheet: Overview (DS890)*.

Table 3: Available Speed Grades and Operating Voltages

| Speed Grade | V_{CCINT} | $V_{CC_PSINTLP}$ | $V_{CC_PSINTFP}$ | $V_{CC_PSINTFP_DDR}$ | Units |
|-------------|-------------|-------------------|-------------------|------------------------|-------|
| -3E | 0.90 | 0.90 | 0.90 | 0.90 | V |
| -2E | 0.85 | 0.85 | 0.85 | 0.85 | V |
| -2I | 0.85 | 0.85 | 0.85 | 0.85 | V |
| -2LE | 0.85 | 0.85 | 0.85 | 0.85 | V |
| -1E | 0.85 | 0.85 | 0.85 | 0.85 | V |
| -1I | 0.85 | 0.85 | 0.85 | 0.85 | V |
| -1Q | 0.85 | 0.85 | 0.85 | 0.85 | V |
| -1M | 0.85 | 0.85 | 0.85 | 0.85 | V |
| -1LI | 0.85 | 0.85 | 0.85 | 0.85 | V |
| -2LE | 0.72 | 0.85 | 0.85 | 0.85 | V |
| -1LI | 0.72 | 0.85 | 0.85 | 0.85 | V |

DC Characteristics Over Recommended Operating Conditions

Table 4: DC Characteristics Over Recommended Operating Conditions

| Symbol | Description | Min | Typ ¹ | Max | Units |
|-----------------------|---|------|------------------|------|---------|
| V_{DRINT} | Data retention V_{CCINT} voltage (below which configuration data might be lost) | 0.68 | - | - | V |
| V_{DRAUX} | Data retention V_{CCAUX} voltage (below which configuration data might be lost) | 1.5 | - | - | V |
| I_{REF} | V_{REF} leakage current per pin | - | - | 15 | μ A |
| I_L | Input or output leakage current per pin (sample-tested) ² | - | - | 15 | μ A |
| C_{IN} ³ | Die input capacitance at the pad (HP I/O) | - | - | 3.1 | pF |
| | Die input capacitance at the pad (HD I/O) | - | - | 4.75 | pF |
| I_{RPU} | Pad pull-up (when selected) at $V_{IN} = 0V$, $V_{CCO} = 3.3V$ | 75 | - | 190 | μ A |
| | Pad pull-up (when selected) at $V_{IN} = 0V$, $V_{CCO} = 2.5V$ | 50 | - | 169 | μ A |
| | Pad pull-up (when selected) at $V_{IN} = 0V$, $V_{CCO} = 1.8V$ | 60 | - | 120 | μ A |
| | Pad pull-up (when selected) at $V_{IN} = 0V$, $V_{CCO} = 1.5V$ | 30 | - | 120 | μ A |
| | Pad pull-up (when selected) at $V_{IN} = 0V$, $V_{CCO} = 1.2V$ | 10 | - | 100 | μ A |
| I_{RPD} | Pad pull-down (when selected) at $V_{IN} = 3.3V$ | 60 | - | 200 | μ A |
| | Pad pull-down (when selected) at $V_{IN} = 1.8V$ | 29 | - | 120 | μ A |
| $I_{CCADCONPL}$ | Analog supply current for the PL SYSMON circuits in the power-up state | - | - | 8 | mA |
| $I_{CCADCONPS}$ | Analog supply current for the PS SYSMON circuits in the power-up state | - | - | 10 | mA |
| $I_{CCADCOFFPL}$ | Analog supply current for the PL SYSMON circuits in the power-down state | - | - | 1.5 | mA |

Table 4: DC Characteristics Over Recommended Operating Conditions (cont'd)

| Symbol | Description | Min | Typ ¹ | Max | Units |
|--|--|-------------------------|-------------------------|-------------------------|-------|
| I _{CCADCOFFPS} | Analog supply current for the PS SYSMON circuits in the power-down state | - | - | 1.8 | mA |
| I _{CC_PSBATT} ^{4,5} | Battery supply current at V _{CC_PSBATT} = 1.50V, RTC enabled | - | - | 3650 | nA |
| | Battery supply current at V _{CC_PSBATT} = 1.50V, RTC disabled | - | - | 650 | nA |
| | Battery supply current at V _{CC_PSBATT} = 1.20V, RTC enabled | - | - | 3150 | nA |
| | Battery supply current at V _{CC_PSBATT} = 1.20V, RTC disabled | - | - | 150 | nA |
| I _{PSFS} ⁶ | PS V _{CC_PSAUX} additional supply current during eFUSE programming | - | - | 115 | mA |
| Calibrated programmable on-die termination (DCI) in HP I/O banks⁷ (measured per JEDEC specification) | | | | | |
| R ⁹ | Thevenin equivalent resistance of programmable input termination to V _{CCO} /2 where ODT = RTT_40 | -10% ⁸ | 40 | +10% ⁸ | Ω |
| | Thevenin equivalent resistance of programmable input termination to V _{CCO} /2 where ODT = RTT_48 | -10% ⁸ | 48 | +10% ⁸ | Ω |
| | Thevenin equivalent resistance of programmable input termination to V _{CCO} /2 where ODT = RTT_60 | -10% ⁸ | 60 | +10% ⁸ | Ω |
| | Programmable input termination to V _{CCO} where ODT = RTT_40 | -10% ⁸ | 40 | +10% ⁸ | Ω |
| | Programmable input termination to V _{CCO} where ODT = RTT_48 | -10% ⁸ | 48 | +10% ⁸ | Ω |
| | Programmable input termination to V _{CCO} where ODT = RTT_60 | -10% ⁸ | 60 | +10% ⁸ | Ω |
| | Programmable input termination to V _{CCO} where ODT = RTT_120 | -10% ⁸ | 120 | +10% ⁸ | Ω |
| | Programmable input termination to V _{CCO} where ODT = RTT_240 | -10% ⁸ | 240 | +10% ⁸ | Ω |
| Uncalibrated programmable on-die termination in HP I/Os banks (measured per JEDEC specification) | | | | | |
| R ⁹ | Thevenin equivalent resistance of programmable input termination to V _{CCO} /2 where ODT = RTT_40 | -50% | 40 | +50% | Ω |
| | Thevenin equivalent resistance of programmable input termination to V _{CCO} /2 where ODT = RTT_48 | -50% | 48 | +50% | Ω |
| | Thevenin equivalent resistance of programmable input termination to V _{CCO} /2 where ODT = RTT_60 | -50% | 60 | +50% | Ω |
| | Programmable input termination to V _{CCO} where ODT = RTT_40 | -50% | 40 | +50% | Ω |
| | Programmable input termination to V _{CCO} where ODT = RTT_48 | -50% | 48 | +50% | Ω |
| | Programmable input termination to V _{CCO} where ODT = RTT_60 | -50% | 60 | +50% | Ω |
| | Programmable input termination to V _{CCO} where ODT = RTT_120 | -50% | 120 | +50% | Ω |
| | Programmable input termination to V _{CCO} where ODT = RTT_240 | -50% | 240 | +50% | Ω |
| Uncalibrated programmable on-die termination in HD I/O banks (measured per JEDEC specification) | | | | | |
| R ⁹ | Thevenin equivalent resistance of programmable input termination to V _{CCO} /2 where ODT = RTT_48 | -50% | 48 | +50% | Ω |
| Internal V _{REF} | 50% V _{CCO} | V _{CCO} × 0.49 | V _{CCO} × 0.50 | V _{CCO} × 0.51 | V |
| | 70% V _{CCO} | V _{CCO} × 0.69 | V _{CCO} × 0.70 | V _{CCO} × 0.71 | V |
| Differential termination | Programmable differential termination (TERM_100) for HP I/O banks | -35% | 100 | +35% | Ω |
| n | Temperature diode ideality factor | - | 1.026 | - | - |

Table 4: DC Characteristics Over Recommended Operating Conditions (cont'd)

| Symbol | Description | Min | Typ ¹ | Max | Units |
|--------|-------------------------------------|-----|------------------|-----|-------|
| r | Temperature diode series resistance | - | 2 | - | Ω |

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. For the HP I/O banks with a V_{CCO} of 1.8V and separated V_{CCO} and V_{CCAUX_IO} power supplies, the I_L maximum current is 70 μA.
3. This measurement represents the die capacitance at the pad, not including the package.
4. Maximum value specified for worst case process at 25°C.
5. I_{CC_PSBATT} is measured when the battery-backed RAM (BBRAM) is enabled.
6. Do not program eFUSE during device configuration (e.g., during configuration, during configuration readback, or when readback CRC is active).
7. VRP resistor tolerance is (240Ω ±1%).
8. If VRP resides at a different bank (DCI cascade), the range increases to ±15%.
9. On-die input termination resistance, for more information see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).

Table 5: PS MIO Pull-up and Pull-down Current

| Symbol | Description | Min | Max | Units |
|--------------------------------|---|-----|-----|-------|
| I _{IRPU} ¹ | Pad pull-up (when selected) at V _{IN} = 0V, V _{CCO_PSIO} = 3.3V | 20 | 80 | μA |
| | Pad pull-up (when selected) at V _{IN} = 0V, V _{CCO_PSIO} = 2.5V | 20 | 80 | μA |
| | Pad pull-up (when selected) at V _{IN} = 0V, V _{CCO_PSIO} = 1.8V | 15 | 65 | μA |
| I _{IRPD} | Pad pull-down (when selected) at V _{IN} = 3.3V | 20 | 80 | μA |
| | Pad pull-down (when selected) at V _{IN} = 2.5V | 20 | 80 | μA |
| | Pad pull-down (when selected) at V _{IN} = 1.8V | 15 | 65 | μA |

Notes:

1. After power-on, the reset values of the MIO pin configuration registers enable and select the PS MIO pull-ups.

V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot

Table 6: V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot for HD I/O Banks

| AC Voltage Overshoot ¹ | % of UI ² at -40°C to 100°C ³ | AC Voltage Undershoot ¹ | % of UI ² at -40°C to 100°C ³ |
|-----------------------------------|---|------------------------------------|---|
| $V_{CCO} + 0.30$ | 100% | -0.30 | 100% |
| $V_{CCO} + 0.35$ | 100% | -0.35 | 90% |
| $V_{CCO} + 0.40$ | 100% | -0.40 | 78% |
| $V_{CCO} + 0.45$ | 100% | -0.45 | 40% |
| $V_{CCO} + 0.50$ | 100% | -0.50 | 24% |
| $V_{CCO} + 0.55$ | 100% | -0.55 | 18.0% |
| $V_{CCO} + 0.60$ | 100% | -0.60 | 13.0% |
| $V_{CCO} + 0.65$ | 100% | -0.65 | 10.8% |
| $V_{CCO} + 0.70$ | 92% | -0.70 | 9.0% |
| $V_{CCO} + 0.75$ | 92% | -0.75 | 7.0% |
| $V_{CCO} + 0.80$ | 92% | -0.80 | 6.0% |
| $V_{CCO} + 0.85$ | 92% | -0.85 | 5.0% |
| $V_{CCO} + 0.90$ | 92% | -0.90 | 4.0% |
| $V_{CCO} + 0.95$ | 92% | -0.95 | 2.5% |

Notes:

1. A total of 200 mA per bank should not be exceeded.
2. For UI smaller than 20 μ s.
3. For the -1Q devices, the upper temperature limit is 125°C. For the -1M devices, the temperature limits are -55°C to 125°C.

Table 7: V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot for HP I/O Banks

| AC Voltage Overshoot ¹ | % of UI ² at -40°C to 100°C ³ | AC Voltage Undershoot ¹ | % of UI ² at -40°C to 100°C ³ |
|-----------------------------------|---|------------------------------------|---|
| $V_{CCO} + 0.30$ | 100% | -0.30 | 100% |
| $V_{CCO} + 0.35$ | 100% | -0.35 | 100% |
| $V_{CCO} + 0.40$ | 92% | -0.40 | 92% |
| $V_{CCO} + 0.45$ | 50% | -0.45 | 50% |
| $V_{CCO} + 0.50$ | 20% | -0.50 | 20% |
| $V_{CCO} + 0.55$ | 10% | -0.55 | 10% |
| $V_{CCO} + 0.60$ | 6% | -0.60 | 6% |
| $V_{CCO} + 0.65$ | 2% | -0.65 | 2% |
| $V_{CCO} + 0.70$ | 2% | -0.70 | 2% |

Notes:

1. A total of 200 mA per bank should not be exceeded.
2. For UI smaller than 20 μ s.
3. For the -1Q devices, the upper temperature limit is 125°C. For the -1M devices, the temperature limits are -55°C to 125°C.

Table 8: V_{PSIN} Maximum Allowed AC Voltage Overshoot and Undershoot for PS I/O Banks

| AC Voltage Overshoot ¹ | % of UI ² at -40°C to 100°C ³ | AC Voltage Undershoot ¹ | % of UI ² at -40°C to 100°C ³ |
|-----------------------------------|---|------------------------------------|---|
| $V_{CCO_PSIO} + 0.30$ | 100% | -0.30 | 100% |
| $V_{CCO_PSIO} + 0.35$ | 100% | -0.35 | 75% |
| $V_{CCO_PSIO} + 0.40$ | 100% | -0.40 | 45% |
| $V_{CCO_PSIO} + 0.45$ | 100% | -0.45 | 40% |
| $V_{CCO_PSIO} + 0.50$ | 75% | -0.50 | 10% |
| $V_{CCO_PSIO} + 0.55$ | 75% | -0.55 | 6% |
| $V_{CCO_PSIO} + 0.60$ | 60% | -0.60 | 2% |
| $V_{CCO_PSIO} + 0.65$ | 30% | -0.65 | 0% |
| $V_{CCO_PSIO} + 0.70$ | 20% | -0.70 | 0% |
| $V_{CCO_PSIO} + 0.75$ | 10% | -0.75 | 0% |
| $V_{CCO_PSIO} + 0.80$ | 10% | -0.80 | 0% |
| $V_{CCO_PSIO} + 0.85$ | 8% | -0.85 | 0% |
| $V_{CCO_PSIO} + 0.90$ | 6% | -0.90 | 0% |
| $V_{CCO_PSIO} + 0.95$ | 6% | -0.95 | 0% |

Notes:

1. A total of 200 mA per bank should not be exceeded.
2. For UI smaller than 20 μ s.
3. For the -1Q devices, the upper temperature limit is 125°C. For the -1M devices, the temperature limits are -55°C to 125°C.

Quiescent Supply Current

Table 9: Typical Quiescent Supply Current

| Symbol | Description ^{1, 2, 3, 4} | Device | Speed Grade and V _{CCINT} Operating Voltages | | | | | Units |
|---------------------|---|--------|---|-------|------|-------|------|-------|
| | | | 0.90V | 0.85V | | 0.72V | | |
| | | | -3 | -2 | -1 | -2 | -1 | |
| I _{CCINTQ} | Quiescent V _{CCINT} supply current | XCZU2 | N/A | 393 | 393 | 344 | 344 | mA |
| | | XCZU3 | N/A | 393 | 393 | 344 | 344 | mA |
| | | XCZU4 | 719 | 684 | 684 | 601 | 601 | mA |
| | | XCZU5 | 719 | 684 | 684 | 601 | 601 | mA |
| | | XCZU6 | 1629 | 1549 | 1549 | 1358 | 1358 | mA |
| | | XCZU7 | 1263 | 1201 | 1201 | 1055 | 1055 | mA |
| | | XCZU9 | 1629 | 1549 | 1549 | 1358 | 1358 | mA |
| | | XCZU11 | 1786 | 1699 | 1699 | 1491 | 1491 | mA |
| | | XCZU15 | 1987 | 1890 | 1890 | 1660 | 1660 | mA |
| | | XCZU17 | 2728 | 2594 | 2594 | 2275 | 2275 | mA |
| | | XCZU19 | 2728 | 2594 | 2594 | 2275 | 2275 | mA |
| | | XAZU2 | N/A | N/A | 393 | N/A | 344 | mA |
| | | XAZU3 | N/A | N/A | 393 | N/A | 344 | mA |
| | | XAZU4 | N/A | N/A | 684 | N/A | 601 | mA |
| | | XAZU5 | N/A | N/A | 684 | N/A | 601 | mA |
| | | XAZU7 | N/A | N/A | 1201 | N/A | N/A | mA |
| | | XAZU11 | N/A | N/A | 1699 | N/A | N/A | mA |
| | | XQZU3 | N/A | 393 | 393 | N/A | 344 | mA |
| | | XQZU5 | N/A | 684 | 684 | N/A | 601 | mA |
| | | XQZU7 | N/A | 1201 | 1201 | N/A | 1055 | mA |
| XQZU9 | N/A | 1549 | 1549 | N/A | 1358 | mA | | |
| XQZU11 | N/A | 1699 | 1699 | N/A | 1491 | mA | | |
| XQZU15 | N/A | 1890 | 1890 | N/A | 1660 | mA | | |
| XQZU19 | N/A | 2594 | 2594 | N/A | 2275 | mA | | |

Table 9: Typical Quiescent Supply Current (cont'd)

| Symbol | Description ^{1, 2, 3, 4} | Device | Speed Grade and V _{CCINT} Operating Voltages | | | | | Units |
|------------------------|--|-------------|---|-------|-----|-------|-----|-------|
| | | | 0.90V | 0.85V | | 0.72V | | |
| | | | -3 | -2 | -1 | -2 | -1 | |
| I _{CCINT_IOQ} | Quiescent V _{CCINT_IO} supply current | XCZU2 | N/A | 44 | 44 | 44 | 44 | mA |
| | | XCZU3 | N/A | 44 | 44 | 44 | 44 | mA |
| | | XCZU4 | 61 | 59 | 59 | 59 | 59 | mA |
| | | XCZU5 | 61 | 59 | 59 | 59 | 59 | mA |
| | | XCZU6 | 61 | 59 | 59 | 59 | 59 | mA |
| | | XCZU7 | 120 | 115 | 115 | 115 | 115 | mA |
| | | XCZU9 | 61 | 59 | 59 | 59 | 59 | mA |
| | | XCZU11 | 120 | 115 | 115 | 115 | 115 | mA |
| | | XCZU15 | 61 | 59 | 59 | 59 | 59 | mA |
| | | XCZU17 | 164 | 158 | 158 | 158 | 158 | mA |
| | | XCZU19 | 164 | 158 | 158 | 158 | 158 | mA |
| | | XAZU2 | N/A | N/A | 44 | N/A | 44 | mA |
| | | XAZU3 | N/A | N/A | 44 | N/A | 44 | mA |
| | | XAZU4 | N/A | N/A | 59 | N/A | 59 | mA |
| | | XAZU5 | N/A | N/A | 59 | N/A | 59 | mA |
| | | XAZU7 | N/A | N/A | 115 | N/A | N/A | mA |
| | | XAZU11 | N/A | N/A | 115 | N/A | N/A | mA |
| | | XQZU3 | N/A | 44 | 44 | N/A | 44 | mA |
| | | XQZU5 | N/A | 59 | 59 | N/A | 59 | mA |
| | | XQZU7 | N/A | 115 | 115 | N/A | 115 | mA |
| XQZU9 | N/A | 59 | 59 | N/A | 59 | mA | | |
| XQZU11 | N/A | 115 | 115 | N/A | 115 | mA | | |
| XQZU15 | N/A | 59 | 59 | N/A | 59 | mA | | |
| XQZU19 | N/A | 158 | 158 | N/A | 158 | mA | | |
| I _{CCOQ} | Quiescent V _{CCO} supply current | All devices | 1 | 1 | 1 | 1 | 1 | mA |

Table 9: Typical Quiescent Supply Current (cont'd)

| Symbol | Description ^{1, 2, 3, 4} | Device | Speed Grade and V _{CCINT} Operating Voltages | | | | | Units |
|---------------------|---|--------|---|-------|-----|-------|-----|-------|
| | | | 0.90V | 0.85V | | 0.72V | | |
| | | | -3 | -2 | -1 | -2 | -1 | |
| I _{CCAUXQ} | Quiescent V _{CCAUX} supply current | XCZU2 | N/A | 55 | 55 | 55 | 55 | mA |
| | | XCZU3 | N/A | 55 | 55 | 55 | 55 | mA |
| | | XCZU4 | 90 | 90 | 90 | 90 | 90 | mA |
| | | XCZU5 | 90 | 90 | 90 | 90 | 90 | mA |
| | | XCZU6 | 227 | 227 | 227 | 227 | 227 | mA |
| | | XCZU7 | 174 | 174 | 174 | 174 | 174 | mA |
| | | XCZU9 | 227 | 227 | 227 | 227 | 227 | mA |
| | | XCZU11 | 255 | 255 | 255 | 255 | 255 | mA |
| | | XCZU15 | 266 | 266 | 266 | 266 | 266 | mA |
| | | XCZU17 | 396 | 396 | 396 | 396 | 396 | mA |
| | | XCZU19 | 396 | 396 | 396 | 396 | 396 | mA |
| | | XAZU2 | N/A | N/A | 55 | N/A | 55 | mA |
| | | XAZU3 | N/A | N/A | 55 | N/A | 55 | mA |
| | | XAZU4 | N/A | N/A | 90 | N/A | 90 | mA |
| | | XAZU5 | N/A | N/A | 90 | N/A | 90 | mA |
| | | XAZU7 | N/A | N/A | 174 | N/A | N/A | mA |
| | | XAZU11 | N/A | N/A | 255 | N/A | N/A | mA |
| | | XQZU3 | N/A | 55 | 55 | N/A | 55 | mA |
| | | XQZU5 | N/A | 90 | 90 | N/A | 90 | mA |
| | | XQZU7 | N/A | 174 | 174 | N/A | 174 | mA |
| XQZU9 | N/A | 227 | 227 | N/A | 227 | mA | | |
| XQZU11 | N/A | 255 | 255 | N/A | 255 | mA | | |
| XQZU15 | N/A | 266 | 266 | N/A | 266 | mA | | |
| XQZU19 | N/A | 396 | 396 | N/A | 396 | mA | | |

Table 9: Typical Quiescent Supply Current (cont'd)

| Symbol | Description ^{1, 2, 3, 4} | Device | Speed Grade and V _{CCINT} Operating Voltages | | | | | Units |
|------------------------|--|--------|---|-------|----|-------|-----|-------|
| | | | 0.90V | 0.85V | | 0.72V | | |
| | | | -3 | -2 | -1 | -2 | -1 | |
| I _{CCAUX_IOQ} | Quiescent V _{CCAUX_IO} supply current | XCZU2 | N/A | 26 | 26 | 26 | 26 | mA |
| | | XCZU3 | N/A | 26 | 26 | 26 | 26 | mA |
| | | XCZU4 | 32 | 32 | 32 | 32 | 32 | mA |
| | | XCZU5 | 32 | 32 | 32 | 32 | 32 | mA |
| | | XCZU6 | 33 | 33 | 33 | 33 | 33 | mA |
| | | XCZU7 | 56 | 56 | 56 | 56 | 56 | mA |
| | | XCZU9 | 33 | 33 | 33 | 33 | 33 | mA |
| | | XCZU11 | 56 | 56 | 56 | 56 | 56 | mA |
| | | XCZU15 | 33 | 33 | 33 | 33 | 33 | mA |
| | | XCZU17 | 74 | 74 | 74 | 74 | 74 | mA |
| | | XCZU19 | 74 | 74 | 74 | 74 | 74 | mA |
| | | XAZU2 | N/A | N/A | 26 | N/A | 26 | mA |
| | | XAZU3 | N/A | N/A | 26 | N/A | 26 | mA |
| | | XAZU4 | N/A | N/A | 32 | N/A | 32 | mA |
| | | XAZU5 | N/A | N/A | 32 | N/A | 32 | mA |
| | | XAZU7 | N/A | N/A | 56 | N/A | N/A | mA |
| | | XAZU11 | N/A | N/A | 56 | N/A | N/A | mA |
| | | XQZU3 | N/A | 26 | 26 | N/A | 26 | mA |
| | | XQZU5 | N/A | 32 | 32 | N/A | 32 | mA |
| | | XQZU7 | N/A | 56 | 56 | N/A | 56 | mA |
| XQZU9 | N/A | 33 | 33 | N/A | 33 | mA | | |
| XQZU11 | N/A | 56 | 56 | N/A | 56 | mA | | |
| XQZU15 | N/A | 33 | 33 | N/A | 33 | mA | | |
| XQZU19 | N/A | 74 | 74 | N/A | 74 | mA | | |

Table 9: Typical Quiescent Supply Current (cont'd)

| Symbol | Description ^{1, 2, 3, 4} | Device | Speed Grade and V _{CCINT} Operating Voltages | | | | | Units |
|----------------------|--|--------|---|-----|-------|-----|-------|-------|
| | | | 0.90V | | 0.85V | | 0.72V | |
| | | | -3 | -2 | -1 | -2 | -1 | |
| I _{CCBRAMQ} | Quiescent V _{CCBRAM} supply current | XCZU2 | N/A | 6 | 6 | 6 | 6 | mA |
| | | XCZU3 | N/A | 6 | 6 | 6 | 6 | mA |
| | | XCZU4 | 9 | 9 | 9 | 9 | 9 | mA |
| | | XCZU5 | 9 | 9 | 9 | 9 | 9 | mA |
| | | XCZU6 | 25 | 24 | 24 | 24 | 24 | mA |
| | | XCZU7 | 16 | 15 | 15 | 15 | 15 | mA |
| | | XCZU9 | 25 | 24 | 24 | 24 | 24 | mA |
| | | XCZU11 | 23 | 22 | 22 | 22 | 22 | mA |
| | | XCZU15 | 29 | 28 | 28 | 28 | 28 | mA |
| | | XCZU17 | 37 | 35 | 35 | 35 | 35 | mA |
| | | XCZU19 | 37 | 35 | 35 | 35 | 35 | mA |
| | | XAZU2 | N/A | N/A | 6 | N/A | 6 | mA |
| | | XAZU3 | N/A | N/A | 6 | N/A | 6 | mA |
| | | XAZU4 | N/A | N/A | 9 | N/A | 9 | mA |
| | | XAZU5 | N/A | N/A | 9 | N/A | 9 | mA |
| | | XAZU7 | N/A | N/A | 15 | N/A | N/A | mA |
| | | XAZU11 | N/A | N/A | 22 | N/A | N/A | mA |
| | | XQZU3 | N/A | 6 | 6 | N/A | 6 | mA |
| | | XQZU5 | N/A | 9 | 9 | N/A | 9 | mA |
| | | XQZU7 | N/A | 15 | 15 | N/A | 15 | mA |
| XQZU9 | N/A | 24 | 24 | N/A | 24 | mA | | |
| XQZU11 | N/A | 22 | 22 | N/A | 22 | mA | | |
| XQZU15 | N/A | 28 | 28 | N/A | 28 | mA | | |
| XQZU19 | N/A | 35 | 35 | N/A | 35 | mA | | |

Notes:

1. Typical values are specified at nominal voltage, 85°C junction temperatures (T_j) with single-ended SelectIO™ resources.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, and all I/O pins are 3-state and floating.
3. Use the Xilinx® Power Estimator (XPE) spreadsheet tool (download at www.xilinx.com/power) to estimate static power consumption for conditions or supplies other than those specified.
4. Typical values depend upon your configuration. To accurately estimate all PS supply currents, use the interactive XPE spreadsheet tool.

Power Supply Sequencing

PS Power-On/Off Power Supply Sequencing

The low-power domain (LPD) must operate before the full-power domain (FPD) can function. The low-power and full-power domains can be powered simultaneously. The PS_POR_B input must be asserted to GND during the power-on sequence (see [Table 37](#)). The FPD (when used) must be powered before PS_POR_B is released.

To achieve minimum current draw and ensure that the I/Os are 3-stated at power-on, the recommended power-on sequence for the low-power domain (LPD) is listed. The recommended power-off sequence is the reverse of the power-on sequence.

1. $V_{CC_PSINTLP}$
2. V_{CC_PSAUX} , V_{CC_PSADC} , and V_{CC_PSPLL} in any order or simultaneously.
3. V_{CCO_PSIO}

To achieve minimum current draw and ensure that the I/Os are 3-stated at power-on, the recommended power-on sequence for the full-power domain (FPD) is listed. The recommended power-off sequence is the reverse of the power-on sequence.

1. $V_{CC_PSINTFP}$ and $V_{CC_PSINTFP_DDR}$ driven from the same supply source.
2. $V_{PS_MGTRAVCC}$ and $V_{CC_PSDDR_PLL}$ in any order or simultaneously.
3. $V_{PS_MGTRAVTT}$ and V_{CCO_PSDDR} in any order or simultaneously.

PL Power-On/Off Power Supply Sequencing

The recommended power-on sequence is V_{CCINT} , $V_{CCINT_IO}/V_{CCBRAM}/V_{CCINT_VCU}$, V_{CCAUX}/V_{CCAUX_IO} , and V_{CCO} to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCINT} and V_{CCINT_IO}/V_{CCBRAM} have the same recommended voltage levels, they can be powered by the same supply and ramped simultaneously. V_{CCINT_IO} must be connected to V_{CCBRAM} . If V_{CCAUX}/V_{CCAUX_IO} and V_{CCO} have the same recommended voltage levels, they can be powered by the same supply and ramped simultaneously. V_{CCAUX} and V_{CCAUX_IO} must be connected together. V_{CCADC} and V_{REF} can be powered at any time and have no power-up sequencing requirements.

The recommended power-on sequence to achieve minimum current draw for the GTH or GTY transceivers is V_{CCINT} , $V_{MGTAVCC}$, $V_{MGTAVTT}$ OR $V_{MGTAVCC}$, V_{CCINT} , $V_{MGTAVTT}$. There is no recommended sequencing for $V_{MGTVCCAUX}$. Both $V_{MGTAVCC}$ and V_{CCINT} can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw. If these recommended sequences are not met, current drawn from $V_{MGTAVTT}$ can be higher than specifications during power-up and power-down.

PS-PL Power Sequencing

The PS and PL power supplies are fully independent. All PS power supplies can be powered before or after any PL power supplies. The PS and PL power regions are isolated to prevent damage.

Power Supply Requirements

Table 10 shows the minimum current, in addition to I_{CCQ} maximum, required by each Zynq UltraScale+ MPSoC for proper power-on and configuration. If these current minimums are met, the device powers on after all supplies have passed through their power-on reset threshold voltages. The device must not be configured until after V_{CCINT} is applied. Once initialized and configured, use the Xilinx Power Estimator (XPE) tools to estimate current drain on these supplies. The XPE spreadsheet tool (download at <http://www.xilinx.com/power>) is also used to estimate power-on current for all supplies.

Table 10: Power-on Current by Device

| I_{CC} Min = | I_{CCINTMIN} | I_{CCINT_IOMIN} + I_{CCBRAMMIN} | I_{CCOMIN} | I_{CCAUXMIN} + I_{CCAUX_IOMIN} | Units |
|-----------------------------|-----------------------------|--|---------------------------|---|--------------|
| I_{CCQ} + | I_{CCINTQ} + | I_{CCBRAMQ} + I_{CCINT_IOQ} + | I_{CCOQ} + | I_{CCAUXQ} + I_{CCAUX_IOQ} + | |
| XCZU2 XAZU2 | 464 | 155 | 50 | 111 | mA |
| XCZU3 XAZU3 XQZU3 | 464 | 155 | 50 | 111 | mA |
| XCZU4 XAZU4 | 770 | 257 | 50 | 386 | mA |
| XCZU5 XAZU5 XQZU5 | 770 | 257 | 50 | 386 | mA |
| XCZU6 | 1800 | 600 | 50 | 650 | mA |
| XCZU7 XAZU7 XQZU7 | 1514 | 505 | 50 | 362 | mA |
| XCZU9 XQZU9 | 1800 | 600 | 50 | 650 | mA |
| XCZU11 XAZU11 XQZU11 | 1961 | 654 | 55 | 709 | mA |
| XCZU15 XQZU15 | 2242 | 748 | 63 | 810 | mA |
| XCZU17 | 3433 | 1145 | 96 | 1240 | mA |
| XCZU19 XQZU19 | 3433 | 1145 | 96 | 1240 | mA |

Table 11: Power Supply Ramp Time

| Symbol | Description | Min | Max | Units |
|-------------------------|---|-----|-----|-------|
| T_{VCCINT} | Ramp time from GND to 95% of V_{CCINT} | 0.2 | 40 | ms |
| T_{VCCINT_IO} | Ramp time from GND to 95% of V_{CCINT_IO} | 0.2 | 40 | ms |
| T_{VCCINT_VCU} | Ramp time from GND to 95% of V_{CCINT_VCU} | 0.2 | 40 | ms |
| T_{VCCO} | Ramp time from GND to 95% of V_{CCO} | 0.2 | 40 | ms |
| T_{VCCAUX} | Ramp time from GND to 95% of V_{CCAUX} | 0.2 | 40 | ms |
| $T_{VCCBRAM}$ | Ramp time from GND to 95% of V_{CCBRAM} | 0.2 | 40 | ms |
| $T_{MGTAVCC}$ | Ramp time from GND to 95% of $V_{MGTAVCC}$ | 0.2 | 40 | ms |
| $T_{MGTAVTT}$ | Ramp time from GND to 95% of $V_{MGTAVTT}$ | 0.2 | 40 | ms |
| $T_{MGTVCCAUX}$ | Ramp time from GND to 95% of $V_{MGTVCCAUX}$ | 0.2 | 40 | ms |
| $T_{VCC_PSINTFP}$ | Ramp time from GND to 95% of $V_{CC_PSINTFP}$ | 0.2 | 40 | ms |
| $T_{VCC_PSINTLP}$ | Ramp time from GND to 95% of $V_{CC_PSINTLP}$ | 0.2 | 40 | ms |
| T_{VCC_PSAUX} | Ramp time from GND to 95% of V_{CC_PSAUX} | 0.2 | 40 | ms |
| $T_{VCC_PSINTFP_DDR}$ | Ramp time from GND to 95% of $V_{CC_PSINTFP_DDR}$ | 0.2 | 40 | ms |
| T_{VCC_PSADC} | Ramp time from GND to 95% of V_{CC_PSADC} | 0.2 | 40 | ms |
| T_{VCC_PSPLL} | Ramp time from GND to 95% of V_{CC_PSPLL} | 0.2 | 40 | ms |
| $T_{PS_MGTRAVCC}$ | Ramp time from GND to 95% of $V_{CC_MGTRAVCC}$ | 0.2 | 40 | ms |
| $T_{PS_MGTRAVTT}$ | Ramp time from GND to 95% of $V_{CC_MGTRAVTT}$ | 0.2 | 40 | ms |
| T_{VCCO_PSDDR} | Ramp time from GND to 95% of V_{CCO_PSDDR} | 0.2 | 40 | ms |
| $T_{VCC_PSDDR_PLL}$ | Ramp time from GND to 95% of $V_{CC_PSDDR_PLL}$ | 0.2 | 40 | ms |
| T_{VCCO_PSIO} | Ramp time from GND to 95% of V_{CCO_PSIO} | 0.2 | 40 | ms |

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

PS I/O Levels

Table 12: PS MIO and CONFIG DC Input and Output Levels

| I/O Standard ¹ | V_{IL} | | V_{IH} | | V_{OL} | V_{OH} | I_{OL} | I_{OH} |
|---------------------------|----------|---------------------|---------------------|------------------------|----------|------------------------|----------|----------|
| | V, Min | V, Max | V, Min | V, Max | V, Max | V, Min | mA | mA |
| LVC MOS33 | -0.300 | 0.800 | 2.000 | V_{CCO_PSIO} | 0.40 | 2.40 | 12 | -12 |
| LVC MOS25 | -0.300 | 0.700 | 1.700 | $V_{CCO_PSIO} + 0.30$ | 0.70 | 1.70 | 12 | -12 |
| LVC MOS18 | -0.300 | 35% V_{CCO_PSIO} | 65% V_{CCO_PSIO} | $V_{CCO_PSIO} + 0.30$ | 0.45 | $V_{CCO_PSIO} - 0.45$ | 12 | -12 |

Notes:

1. Tested according to relevant specifications.

Table 13: PS DDR DC Input and Output Levels

| DDR Standard ¹ | V _{IL} | | V _{IH} | | V _{OL} ² | V _{OH} ² | I _{OL} | I _{OH} |
|---------------------------|-----------------|--------------------------|--------------------------|------------------------|--------------------------------------|--------------------------------------|-----------------|-----------------|
| | V, Min | V, Max | V, Min | V, Max | V, Max | V, Min | mA | mA |
| DDR4 | 0.000 | V _{REF} - 0.100 | V _{REF} + 0.100 | V _{CCO_PSDDR} | 0.8 x V _{CCO_PSDDR} - 0.150 | 0.8 x V _{CCO_PSDDR} + 0.150 | 10 | -0.1 |
| LPDDR4 | 0.000 | V _{REF} - 0.100 | V _{REF} + 0.100 | V _{CCO_PSDDR} | 0.3 x V _{CCO_PSDDR} - 0.150 | 0.3 x V _{CCO_PSDDR} + 0.150 | 0.1 | -10 |
| DDR3 | -0.300 | V _{REF} - 0.100 | V _{REF} + 0.100 | V _{CCO_PSDDR} | 0.5 x V _{CCO_PSDDR} - 0.175 | 0.5 x V _{CCO_PSDDR} + 0.175 | 8 | -8 |
| LPDDR3 | 0.000 | V _{REF} - 0.100 | V _{REF} + 0.100 | V _{CCO_PSDDR} | 0.5 x V _{CCO_PSDDR} - 0.150 | 0.5 x V _{CCO_PSDDR} + 0.150 | 8 | -8 |
| DDR3L | -0.300 | V _{REF} - 0.090 | V _{REF} + 0.090 | V _{CCO_PSDDR} | 0.5 x V _{CCO_PSDDR} - 0.150 | 0.5 x V _{CCO_PSDDR} + 0.150 | 8 | -8 |

Notes:

1. Tested according to relevant specifications.
2. DDR4 V_{OL}/V_{OH} specifications are only applicable for DQ/DQS pins.

PL I/O Levels

Table 14: SelectIO DC Input and Output Levels For HD I/O Banks

| I/O Standard ^{1, 2} | V _{IL} | | V _{IH} | | V _{OL} | V _{OH} | I _{OL} | I _{OH} |
|------------------------------|-----------------|--------------------------|--------------------------|--------------------------|-----------------------------|-----------------------------|-----------------|-----------------|
| | V, Min | V, Max | V, Min | V, Max | V, Max | V, Min | mA | mA |
| HSTL_I | -0.300 | V _{REF} - 0.100 | V _{REF} + 0.100 | V _{CCO} + 0.300 | 0.400 | V _{CCO} - 0.400 | 8.0 | -8.0 |
| HSTL_I_18 | -0.300 | V _{REF} - 0.100 | V _{REF} + 0.100 | V _{CCO} + 0.300 | 0.400 | V _{CCO} - 0.400 | 8.0 | -8.0 |
| HSUL_12 | -0.300 | V _{REF} - 0.130 | V _{REF} + 0.130 | V _{CCO} + 0.300 | 20% V _{CCO} | 80% V _{CCO} | 0.1 | -0.1 |
| LVC MOS12 | -0.300 | 35% V _{CCO} | 65% V _{CCO} | V _{CCO} + 0.300 | 0.400 | V _{CCO} - 0.400 | Note 3 | Note 3 |
| LVC MOS15 | -0.300 | 35% V _{CCO} | 65% V _{CCO} | V _{CCO} + 0.300 | 0.450 | V _{CCO} - 0.450 | Note 4 | Note 4 |
| LVC MOS18 | -0.300 | 35% V _{CCO} | 65% V _{CCO} | V _{CCO} + 0.300 | 0.450 | V _{CCO} - 0.450 | Note 4 | Note 4 |
| LVC MOS25 | -0.300 | 0.700 | 1.700 | V _{CCO} + 0.300 | 0.400 | V _{CCO} - 0.400 | Note 4 | Note 4 |
| LVC MOS33 | -0.300 | 0.800 | 2.000 | 3.400 | 0.400 | V _{CCO} - 0.400 | Note 4 | Note 4 |
| LV TTL | -0.300 | 0.800 | 2.000 | 3.400 | 0.400 | 2.400 | Note 4 | Note 4 |
| SSTL12 | -0.300 | V _{REF} - 0.100 | V _{REF} + 0.100 | V _{CCO} + 0.300 | V _{CCO} /2 - 0.150 | V _{CCO} /2 + 0.150 | 14.25 | -14.25 |
| SSTL135 | -0.300 | V _{REF} - 0.090 | V _{REF} + 0.090 | V _{CCO} + 0.300 | V _{CCO} /2 - 0.150 | V _{CCO} /2 + 0.150 | 8.9 | -8.9 |
| SSTL135_II | -0.300 | V _{REF} - 0.090 | V _{REF} + 0.090 | V _{CCO} + 0.300 | V _{CCO} /2 - 0.150 | V _{CCO} /2 + 0.150 | 13.0 | -13.0 |
| SSTL15 | -0.300 | V _{REF} - 0.100 | V _{REF} + 0.100 | V _{CCO} + 0.300 | V _{CCO} /2 - 0.175 | V _{CCO} /2 + 0.175 | 8.9 | -8.9 |
| SSTL15_II | -0.300 | V _{REF} - 0.100 | V _{REF} + 0.100 | V _{CCO} + 0.300 | V _{CCO} /2 - 0.175 | V _{CCO} /2 + 0.175 | 13.0 | -13.0 |
| SSTL18_I | -0.300 | V _{REF} - 0.125 | V _{REF} + 0.125 | V _{CCO} + 0.300 | V _{CCO} /2 - 0.470 | V _{CCO} /2 + 0.470 | 8.0 | -8.0 |
| SSTL18_II | -0.300 | V _{REF} - 0.125 | V _{REF} + 0.125 | V _{CCO} + 0.300 | V _{CCO} /2 - 0.600 | V _{CCO} /2 + 0.600 | 13.4 | -13.4 |

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).
3. Supported drive strengths of 4, 8, or 12 mA in HD I/O banks.
4. Supported drive strengths of 4, 8, 12, or 16 mA in HD I/O banks.

Table 15: SelectIO DC Input and Output Levels for HP I/O Banks

| I/O Standard ^{1, 2, 3} | V_{IL} | | V_{IH} | | V_{OL} | V_{OH} | I_{OL} | I_{OH} |
|---------------------------------|----------|-------------------|--------------------|-------------------|---------------------|---------------------|----------|----------|
| | V, Min | V, Max | V, Min | V, Max | V, Max | V, Min | mA | mA |
| HSTL_I | -0.300 | $V_{REF} - 0.100$ | $V_{REF} + 0.100$ | $V_{CCO} + 0.300$ | 0.400 | $V_{CCO} - 0.400$ | 5.8 | -5.8 |
| HSTL_I_12 | -0.300 | $V_{REF} - 0.080$ | $V_{REF} + 0.080$ | $V_{CCO} + 0.300$ | 25% V_{CCO} | 75% V_{CCO} | 4.1 | -4.1 |
| HSTL_I_18 | -0.300 | $V_{REF} - 0.100$ | $V_{REF} + 0.100$ | $V_{CCO} + 0.300$ | 0.400 | $V_{CCO} - 0.400$ | 6.2 | -6.2 |
| HSUL_12 | -0.300 | $V_{REF} - 0.130$ | $V_{REF} + 0.130$ | $V_{CCO} + 0.300$ | 20% V_{CCO} | 80% V_{CCO} | 0.1 | -0.1 |
| LVC MOS12 | -0.300 | 35% V_{CCO} | 65% V_{CCO} | $V_{CCO} + 0.300$ | 0.400 | $V_{CCO} - 0.400$ | Note 4 | Note 4 |
| LVC MOS15 | -0.300 | 35% V_{CCO} | 65% V_{CCO} | $V_{CCO} + 0.300$ | 0.450 | $V_{CCO} - 0.450$ | Note 5 | Note 5 |
| LVC MOS18 | -0.300 | 35% V_{CCO} | 65% V_{CCO} | $V_{CCO} + 0.300$ | 0.450 | $V_{CCO} - 0.450$ | Note 5 | Note 5 |
| LVDCI_15 | -0.300 | 35% V_{CCO} | 65% V_{CCO} | $V_{CCO} + 0.300$ | 0.450 | $V_{CCO} - 0.450$ | 7.0 | -7.0 |
| LVDCI_18 | -0.300 | 35% V_{CCO} | 65% V_{CCO} | $V_{CCO} + 0.300$ | 0.450 | $V_{CCO} - 0.450$ | 7.0 | -7.0 |
| SSTL12 | -0.300 | $V_{REF} - 0.100$ | $V_{REF} + 0.100$ | $V_{CCO} + 0.300$ | $V_{CCO}/2 - 0.150$ | $V_{CCO}/2 + 0.150$ | 8.0 | -8.0 |
| SSTL135 | -0.300 | $V_{REF} - 0.090$ | $V_{REF} + 0.090$ | $V_{CCO} + 0.300$ | $V_{CCO}/2 - 0.150$ | $V_{CCO}/2 + 0.150$ | 9.0 | -9.0 |
| SSTL15 | -0.300 | $V_{REF} - 0.100$ | $V_{REF} + 0.100$ | $V_{CCO} + 0.300$ | $V_{CCO}/2 - 0.175$ | $V_{CCO}/2 + 0.175$ | 10.0 | -10.0 |
| SSTL18_I | -0.300 | $V_{REF} - 0.125$ | $V_{REF} + 0.125$ | $V_{CCO} + 0.300$ | $V_{CCO}/2 - 0.470$ | $V_{CCO}/2 + 0.470$ | 7.0 | -7.0 |
| MIPI_DPHY_DCI_LP ⁶ | -0.300 | 0.550 | 0.880 ⁷ | $V_{CCO} + 0.300$ | 0.050 | 1.100 | 0.01 | -0.01 |

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).
3. POD10 and POD12 DC input and output levels are shown in Table 16, Table 21, and Table 22.
4. Supported drive strengths of 2, 4, 6, or 8 mA in HP I/O banks.
5. Supported drive strengths of 2, 4, 6, 8, or 12 mA in HP I/O banks.
6. Low-power option for MIPI_DPHY_DCI.
7. When operating at data rates of 1.5 Gb/s to 2.5 Gb/s, the minimum V_{IH} is 0.790V. These data rates, outlined in Table 72 are supported for XC and XA devices only.

Table 16: DC Input Levels for Single-ended POD10 and POD12 I/O Standards

| I/O Standard ^{1, 2} | V_{IL} | | V_{IH} | |
|------------------------------|----------|-------------------|-------------------|-------------------|
| | V, Min | V, Max | V, Min | V, Max |
| POD10 | -0.300 | $V_{REF} - 0.068$ | $V_{REF} + 0.068$ | $V_{CCO} + 0.300$ |
| POD12 | -0.300 | $V_{REF} - 0.068$ | $V_{REF} + 0.068$ | $V_{CCO} + 0.300$ |

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).

Table 17: Differential SelectIO DC Input and Output Levels

| I/O Standard | V_{ICM} (V) ¹ | | | V_{ID} (V) ² | | | V_{ILHS} ³ | V_{IHHS} ³ | V_{OCM} (V) ⁴ | | | V_{OD} (V) ⁵ | | |
|-----------------------------------|----------------------------|-------|-------|---------------------------|-------|-------|-------------------------|-------------------------|----------------------------|-------|-------|---------------------------|-------|-------|
| | Min | Typ | Max | Min | Typ | Max | Min | Max | Min | Typ | Max | Min | Typ | Max |
| SUB_LVDS ⁸ | 0.500 | 0.900 | 1.300 | 0.070 | - | - | - | - | 0.700 | 0.900 | 1.100 | 0.100 | 0.150 | 0.200 |
| LVPECL | 0.300 | 1.200 | 1.425 | 0.100 | 0.350 | 0.600 | - | - | - | - | - | - | - | - |
| SLVS_400_18 | 0.070 | 0.200 | 0.330 | 0.140 | - | 0.450 | - | - | - | - | - | - | - | - |
| SLVS_400_25 | 0.070 | 0.200 | 0.330 | 0.140 | - | 0.450 | - | - | - | - | - | - | - | - |
| MIPI_DPHY_DCI_HS ^{9, 10} | 0.070 | - | 0.330 | 0.070 | - | - | -0.040 | 0.460 | 0.150 | 0.200 | 0.250 | 0.140 | 0.200 | 0.270 |

Notes:

- V_{ICM} is the input common mode voltage.
- V_{ID} is the input differential voltage ($Q - \bar{Q}$).
- V_{IHHS} and V_{ILHS} are the single-ended input high and low voltages, respectively.
- V_{OCM} is the output common mode voltage.
- V_{OD} is the output differential voltage ($Q - \bar{Q}$).
- LVDS_25 is specified in Table 23.
- LVDS is specified in Table 24.
- Only the SUB_LVDS receiver is supported in HD I/O banks.
- High-speed option for MIPI_DPHY_DCI. The V_{ID} maximum is aligned with the standard's specification. A higher V_{ID} is acceptable as long as the V_{IN} specification is also met.
- When operating at data rates of 1.5 Gb/s to 2.5 Gb/s, the minimum V_{ID} is 0.040V. These data rates, outlined in Table 72 are supported for XC and XA devices only.

Table 18: Complementary Differential SelectIO DC Input and Output Levels for HD I/O Banks

| I/O Standard | V_{ICM} (V) ¹ | | | V_{ID} (V) ² | | V_{OL} (V) ³ | V_{OH} (V) ⁴ | I_{OL} | I_{OH} |
|-----------------|----------------------------|-------|-------|---------------------------|-----|---------------------------|---------------------------|----------|----------|
| | Min | Typ | Max | Min | Max | Max | Min | mA | mA |
| DIFF_HSTL_I | 0.300 | 0.750 | 1.125 | 0.100 | - | 0.400 | $V_{CCO} - 0.400$ | 8.0 | -8.0 |
| DIFF_HSTL_I_18 | 0.300 | 0.900 | 1.425 | 0.100 | - | 0.400 | $V_{CCO} - 0.400$ | 8.0 | -8.0 |
| DIFF_HSUL_12 | 0.300 | 0.600 | 0.850 | 0.100 | - | 20% V_{CCO} | 80% V_{CCO} | 0.1 | -0.1 |
| DIFF_SSTL12 | 0.300 | 0.600 | 0.850 | 0.100 | - | $(V_{CCO}/2) - 0.150$ | $(V_{CCO}/2) + 0.150$ | 14.25 | -14.25 |
| DIFF_SSTL135 | 0.300 | 0.675 | 1.000 | 0.100 | - | $(V_{CCO}/2) - 0.150$ | $(V_{CCO}/2) + 0.150$ | 8.9 | -8.9 |
| DIFF_SSTL135_II | 0.300 | 0.675 | 1.000 | 0.100 | - | $(V_{CCO}/2) - 0.150$ | $(V_{CCO}/2) + 0.150$ | 13.0 | -13.0 |
| DIFF_SSTL15 | 0.300 | 0.750 | 1.125 | 0.100 | - | $(V_{CCO}/2) - 0.175$ | $(V_{CCO}/2) + 0.175$ | 8.9 | -8.9 |
| DIFF_SSTL15_II | 0.300 | 0.750 | 1.125 | 0.100 | - | $(V_{CCO}/2) - 0.175$ | $(V_{CCO}/2) + 0.175$ | 13.0 | -13.0 |
| DIFF_SSTL18_I | 0.300 | 0.900 | 1.425 | 0.100 | - | $(V_{CCO}/2) - 0.470$ | $(V_{CCO}/2) + 0.470$ | 8.0 | -8.0 |
| DIFF_SSTL18_II | 0.300 | 0.900 | 1.425 | 0.100 | - | $(V_{CCO}/2) - 0.600$ | $(V_{CCO}/2) + 0.600$ | 13.4 | -13.4 |

Notes:

- V_{ICM} is the input common mode voltage.
- V_{ID} is the input differential voltage.
- V_{OL} is the single-ended low-output voltage.
- V_{OH} is the single-ended high-output voltage.

Table 19: Complementary Differential SelectIO DC Input and Output Levels for HP I/O Banks

| I/O Standard ¹ | V_{ICM} (V) ² | | | V_{ID} (V) ³ | | V_{OL} (V) ⁴ | V_{OH} (V) ⁵ | I_{OL} | I_{OH} |
|---------------------------|----------------------------|-------------|------------------------|---------------------------|-----|---------------------------|---------------------------|----------|----------|
| | Min | Typ | Max | Min | Max | Max | Min | mA | mA |
| DIFF_HSTL_I | 0.680 | $V_{CCO}/2$ | $(V_{CCO}/2) + 0.150$ | 0.100 | - | 0.400 | $V_{CCO} - 0.400$ | 5.8 | -5.8 |
| DIFF_HSTL_I_12 | $0.400 \times V_{CCO}$ | $V_{CCO}/2$ | $0.600 \times V_{CCO}$ | 0.100 | - | $0.250 \times V_{CCO}$ | $0.750 \times V_{CCO}$ | 4.1 | -4.1 |
| DIFF_HSTL_I_18 | $(V_{CCO}/2) - 0.175$ | $V_{CCO}/2$ | $(V_{CCO}/2) + 0.175$ | 0.100 | - | 0.400 | $V_{CCO} - 0.400$ | 6.2 | -6.2 |
| DIFF_HSUL_12 | $(V_{CCO}/2) - 0.120$ | $V_{CCO}/2$ | $(V_{CCO}/2) + 0.120$ | 0.100 | - | $20\% V_{CCO}$ | $80\% V_{CCO}$ | 0.1 | -0.1 |
| DIFF_SSTL12 | $(V_{CCO}/2) - 0.150$ | $V_{CCO}/2$ | $(V_{CCO}/2) + 0.150$ | 0.100 | - | $(V_{CCO}/2) - 0.150$ | $(V_{CCO}/2) + 0.150$ | 8.0 | -8.0 |
| DIFF_SSTL135 | $(V_{CCO}/2) - 0.150$ | $V_{CCO}/2$ | $(V_{CCO}/2) + 0.150$ | 0.100 | - | $(V_{CCO}/2) - 0.150$ | $(V_{CCO}/2) + 0.150$ | 9.0 | -9.0 |
| DIFF_SSTL15 | $(V_{CCO}/2) - 0.175$ | $V_{CCO}/2$ | $(V_{CCO}/2) + 0.175$ | 0.100 | - | $(V_{CCO}/2) - 0.175$ | $(V_{CCO}/2) + 0.175$ | 10.0 | -10.0 |
| DIFF_SSTL18_I | $(V_{CCO}/2) - 0.175$ | $V_{CCO}/2$ | $(V_{CCO}/2) + 0.175$ | 0.100 | - | $(V_{CCO}/2) - 0.470$ | $(V_{CCO}/2) + 0.470$ | 7.0 | -7.0 |

Notes:

1. DIFF_POD10 and DIFF_POD12 HP I/O bank specifications are shown in Table 20, Table 21, Table 22.
2. V_{ICM} is the input common mode voltage.
3. V_{ID} is the input differential voltage.
4. V_{OL} is the single-ended low-output voltage.
5. V_{OH} is the single-ended high-output voltage.

Table 20: DC Input Levels for Differential POD10 and POD12 I/O Standards

| I/O Standard ^{1,2} | V_{ICM} (V) | | | V_{ID} (V) | |
|-----------------------------|---------------|------|------|--------------|-----|
| | Min | Typ | Max | Min | Max |
| DIFF_POD10 | 0.63 | 0.70 | 0.77 | 0.14 | - |
| DIFF_POD12 | 0.76 | 0.84 | 0.92 | 0.16 | - |

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).

Table 21: DC Output Levels for Single-ended and Differential POD10 and POD12 Standards

| Symbol | Description ^{1,2} | V_{OUT} | Min | Typ | Max | Units |
|----------|----------------------------|---|-----|-----|-----|----------|
| R_{OL} | Pull-down resistance | V_{OM_DC} (as described in Table 22) | 36 | 40 | 44 | Ω |
| R_{OH} | Pull-up resistance | V_{OM_DC} (as described in Table 22) | 36 | 40 | 44 | Ω |

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).

Table 22: Definitions for DC Output Levels for Single-ended and Differential POD10 and POD12 Standards

| Symbol | Description | All Speed Grades | Units |
|--------------|--|----------------------|-------|
| V_{OM_DC} | DC output Mid measurement level (for IV curve linearity) | $0.8 \times V_{CCO}$ | V |

LVDS DC Specifications (LVDS_25)

The LVDS_25 standard is available in the HD I/O banks. See the *UltraScale Architecture SelectIO Resources User Guide* (UG571) for more information.

Table 23: LVDS_25 DC Specifications

| Symbol | DC Parameter | Min | Typ | Max | Units |
|-------------|---|-------|-------|------------------|-------|
| V_{CCO}^1 | Supply voltage | 2.375 | 2.500 | 2.625 | V |
| V_{IDIFF} | Differential input voltage: (Q - \bar{Q}), Q = High (\bar{Q} - Q), \bar{Q} = High | 100 | 350 | 600 ² | mV |
| V_{ICM} | Input common-mode voltage | 0.300 | 1.200 | 1.425 | V |

Notes:

1. LVDS_25 in HD I/O banks supports inputs only. LVDS_25 inputs without internal termination have no V_{CCO} requirements. Any V_{CCO} can be chosen as long as the input voltage levels do not violate the *Recommended Operating Condition* (Table 2) specification for the V_{IN} I/O pin voltage.
2. Maximum V_{IDIFF} value is specified for the maximum V_{ICM} specification. With a lower V_{ICM} , a higher V_{DIFF} is tolerated only when the recommended operating conditions and overshoot/undershoot V_{IN} specifications are maintained.

LVDS DC Specifications (LVDS)

The LVDS standard is available in the HP I/O banks. See the *UltraScale Architecture SelectIO Resources User Guide* (UG571) for more information.

Table 24: LVDS DC Specifications

| Symbol | DC Parameter | Conditions | Min | Typ | Max | Units |
|-----------------|--|--|-------|-------|------------------|-------|
| V_{CCO}^1 | Supply voltage | | 1.710 | 1.800 | 1.890 | V |
| V_{ODIFF}^2 | Differential output voltage: (Q - \bar{Q}), Q = High (\bar{Q} - Q), \bar{Q} = High | $R_T = 100\Omega$ across Q and \bar{Q} signals | 247 | 350 | 454 | mV |
| V_{OCM}^2 | Output common-mode voltage | $R_T = 100\Omega$ across Q and \bar{Q} signals | 1.000 | 1.250 | 1.425 | V |
| V_{IDIFF}^3 | Differential input voltage: (Q - \bar{Q}), Q = High (\bar{Q} - Q), \bar{Q} = High | | 100 | 350 | 600 ³ | mV |
| $V_{ICM_DC}^4$ | Input common-mode voltage (DC coupling) | | 0.300 | 1.200 | 1.425 | V |
| $V_{ICM_AC}^5$ | Input common-mode voltage (AC coupling) | | 0.600 | - | 1.100 | V |

Notes:

1. In HP I/O banks, when LVDS is used with input-only functionality, it can be placed in a bank where the V_{CCO} levels are different from the specified level only if internal differential termination is not used. In this scenario, V_{CCO} must be chosen to ensure the input pin voltage levels do not violate the *Recommended Operating Condition* (Table 2) specification for the V_{IN} I/O pin voltage.
2. V_{OCM} and V_{ODIFF} values are for LVDS_PRE_EMPHASIS = FALSE.
3. Maximum V_{IDIFF} value is specified for the maximum V_{ICM} specification. With a lower V_{ICM} , a higher V_{DIFF} is tolerated only when the recommended operating conditions and overshoot/undershoot V_{IN} specifications are maintained.
4. Input common mode voltage for DC coupled configurations. EQUALIZATION = EQ_NONE (Default).
5. External input common mode voltage specification for AC coupled configurations. EQUALIZATION = EQ_LEVEL0, EQ_LEVEL1, EQ_LEVEL2, EQ_LEVEL3, EQ_LEVEL4.

AC Switching Characteristics

All values represented in this data sheet are based on the speed specifications in the Vivado® Design Suite as outlined in the following table.

Table 25: Speed Specification Version By Device

| 2019.2.2 | Device |
|----------|--|
| 1.27 | XCZU2CG, XCZU2EG, XCZU3CG, XCZU3EG, XCZU4CG, XCZU4EG, XCZU4EV, XCZU5CG, XCZU5EG, XCZU5EV, XCZU6CG, XCZU6EG, XCZU7CG, XCZU7EG, XCZU7EV, XCZU9CG, XCZU9EG, XCZU11EG, XCZU15EG, XCZU17EG, XCZU19EG XQZU3EG, XQZU5EV, XQZU7EV, XQZU9EG, XQZU11EG, XQZU15EG, XQZU19EG XAZU2EG, XAZU3EG, XAZU4EV, XAZU5EV, XAZU7EV, XAZU11EG |

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

- **Advance Product Specification:** These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.
- **Preliminary Product Specification:** These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.
- **Product Specification:** These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to production before faster speed grades.

Testing of AC Switching Characteristics

Internal timing parameters are derived from measuring internal test patterns. All AC switching characteristics are representative of worst-case supply voltage and junction temperature conditions.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Zynq UltraScale+ MPSoCs.

Speed Grade Designations

Because individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. [Table 26](#) correlates the current status of the Zynq UltraScale+ MPSoC on a per speed grade basis. See [Table 3](#) for operating voltages listed by speed grade.

Table 26: Speed Grade Designations by Device

| Device | Speed Grade, Temperature Ranges, and V_{CCINT} Operating Voltages ¹ | | |
|---------|--|-------------|---|
| | Advance | Preliminary | Production |
| XCZU2CG | | | -2E ($V_{CCINT} = 0.85V$), -2I ($V_{CCINT} = 0.85V$) -1E ($V_{CCINT} = 0.85V$), -1I ($V_{CCINT} = 0.85V$) -2LE ($V_{CCINT} = 0.85V$), -2LE ($V_{CCINT} = 0.72V$) ¹ -1LI ($V_{CCINT} = 0.85V$), -1LI ($V_{CCINT} = 0.72V$) ¹ |
| XCZU2EG | | | -2E ($V_{CCINT} = 0.85V$), -2I ($V_{CCINT} = 0.85V$) -1E ($V_{CCINT} = 0.85V$), -1I ($V_{CCINT} = 0.85V$) -2LE ($V_{CCINT} = 0.85V$), -2LE ($V_{CCINT} = 0.72V$) ¹ -1LI ($V_{CCINT} = 0.85V$), -1LI ($V_{CCINT} = 0.72V$) ¹ |
| XCZU3CG | | | -2E ($V_{CCINT} = 0.85V$), -2I ($V_{CCINT} = 0.85V$) -1E ($V_{CCINT} = 0.85V$), -1I ($V_{CCINT} = 0.85V$) -2LE ($V_{CCINT} = 0.85V$), -2LE ($V_{CCINT} = 0.72V$) ¹ -1LI ($V_{CCINT} = 0.85V$), -1LI ($V_{CCINT} = 0.72V$) ¹ |
| XCZU3EG | | | -2E ($V_{CCINT} = 0.85V$), -2I ($V_{CCINT} = 0.85V$) -1E ($V_{CCINT} = 0.85V$), -1I ($V_{CCINT} = 0.85V$) -2LE ($V_{CCINT} = 0.85V$), -2LE ($V_{CCINT} = 0.72V$) ¹ -1LI ($V_{CCINT} = 0.85V$), -1LI ($V_{CCINT} = 0.72V$) ¹ |
| XCZU4CG | | | -2E ($V_{CCINT} = 0.85V$), -2I ($V_{CCINT} = 0.85V$) -1E ($V_{CCINT} = 0.85V$), -1I ($V_{CCINT} = 0.85V$) -2LE ($V_{CCINT} = 0.85V$), -2LE ($V_{CCINT} = 0.72V$) ¹ -1LI ($V_{CCINT} = 0.85V$), -1LI ($V_{CCINT} = 0.72V$) ¹ |
| XCZU4EG | | | -3E ($V_{CCINT} = 0.90V$) -2E ($V_{CCINT} = 0.85V$), -2I ($V_{CCINT} = 0.85V$) -1E ($V_{CCINT} = 0.85V$), -1I ($V_{CCINT} = 0.85V$) -2LE ($V_{CCINT} = 0.85V$), -2LE ($V_{CCINT} = 0.72V$) ¹ -1LI ($V_{CCINT} = 0.85V$), -1LI ($V_{CCINT} = 0.72V$) ¹ |
| XCZU4EV | | | -3E ($V_{CCINT} = 0.90V$) -2E ($V_{CCINT} = 0.85V$), -2I ($V_{CCINT} = 0.85V$) -1E ($V_{CCINT} = 0.85V$), -1I ($V_{CCINT} = 0.85V$) -2LE ($V_{CCINT} = 0.85V$), -2LE ($V_{CCINT} = 0.72V$) ¹ -1LI ($V_{CCINT} = 0.85V$), -1LI ($V_{CCINT} = 0.72V$) ¹ |
| XCZU5CG | | | -2E ($V_{CCINT} = 0.85V$), -2I ($V_{CCINT} = 0.85V$) -1E ($V_{CCINT} = 0.85V$), -1I ($V_{CCINT} = 0.85V$) -2LE ($V_{CCINT} = 0.85V$), -2LE ($V_{CCINT} = 0.72V$) ¹ -1LI ($V_{CCINT} = 0.85V$), -1LI ($V_{CCINT} = 0.72V$) ¹ |
| XCZU5EG | | | -3E ($V_{CCINT} = 0.90V$) -2E ($V_{CCINT} = 0.85V$), -2I ($V_{CCINT} = 0.85V$) -1E ($V_{CCINT} = 0.85V$), -1I ($V_{CCINT} = 0.85V$) -2LE ($V_{CCINT} = 0.85V$), -2LE ($V_{CCINT} = 0.72V$) ¹ -1LI ($V_{CCINT} = 0.85V$), -1LI ($V_{CCINT} = 0.72V$) ¹ |
| XCZU5EV | | | -3E ($V_{CCINT} = 0.90V$) -2E ($V_{CCINT} = 0.85V$), -2I ($V_{CCINT} = 0.85V$) -1E ($V_{CCINT} = 0.85V$), -1I ($V_{CCINT} = 0.85V$) -2LE ($V_{CCINT} = 0.85V$), -2LE ($V_{CCINT} = 0.72V$) ¹ -1LI ($V_{CCINT} = 0.85V$), -1LI ($V_{CCINT} = 0.72V$) ¹ |
| XCZU6CG | | | -2E ($V_{CCINT} = 0.85V$), -2I ($V_{CCINT} = 0.85V$) -1E ($V_{CCINT} = 0.85V$), -1I ($V_{CCINT} = 0.85V$) -2LE ($V_{CCINT} = 0.85V$), -2LE ($V_{CCINT} = 0.72V$) ¹ -1LI ($V_{CCINT} = 0.85V$), -1LI ($V_{CCINT} = 0.72V$) ¹ |

Table 26: Speed Grade Designations by Device (cont'd)

| Device | Speed Grade, Temperature Ranges, and V _{CCINT} Operating Voltages ¹ | | |
|----------|---|-------------|--|
| | Advance | Preliminary | Production |
| XCZU6EG | | | -3E (V _{CCINT} = 0.90V) -2E (V _{CCINT} = 0.85V), -2I (V _{CCINT} = 0.85V) -1E (V _{CCINT} = 0.85V), -1I (V _{CCINT} = 0.85V) -2LE (V _{CCINT} = 0.85V), -2LE (V _{CCINT} = 0.72V) ¹ -1LI (V _{CCINT} = 0.85V), -1LI (V _{CCINT} = 0.72V) ¹ |
| XCZU7CG | | | -2E (V _{CCINT} = 0.85V), -2I (V _{CCINT} = 0.85V) -1E (V _{CCINT} = 0.85V), -1I (V _{CCINT} = 0.85V) -2LE (V _{CCINT} = 0.85V), -2LE (V _{CCINT} = 0.72V) ¹ -1LI (V _{CCINT} = 0.85V), -1LI (V _{CCINT} = 0.72V) ¹ |
| XCZU7EG | | | -3E (V _{CCINT} = 0.90V) -2E (V _{CCINT} = 0.85V), -2I (V _{CCINT} = 0.85V) -1E (V _{CCINT} = 0.85V), -1I (V _{CCINT} = 0.85V) -2LE (V _{CCINT} = 0.85V), -2LE (V _{CCINT} = 0.72V) ¹ -1LI (V _{CCINT} = 0.85V), -1LI (V _{CCINT} = 0.72V) ¹ |
| XCZU7EV | | | -3E (V _{CCINT} = 0.90V) -2E (V _{CCINT} = 0.85V), -2I (V _{CCINT} = 0.85V) -1E (V _{CCINT} = 0.85V), -1I (V _{CCINT} = 0.85V) -2LE (V _{CCINT} = 0.85V), -2LE (V _{CCINT} = 0.72V) ¹ -1LI (V _{CCINT} = 0.85V), -1LI (V _{CCINT} = 0.72V) ¹ |
| XCZU9CG | | | -2E (V _{CCINT} = 0.85V), -2I (V _{CCINT} = 0.85V) -1E (V _{CCINT} = 0.85V), -1I (V _{CCINT} = 0.85V) -2LE (V _{CCINT} = 0.85V), -2LE (V _{CCINT} = 0.72V) ¹ -1LI (V _{CCINT} = 0.85V), -1LI (V _{CCINT} = 0.72V) ¹ |
| XCZU9EG | | | -3E (V _{CCINT} = 0.90V) -2E (V _{CCINT} = 0.85V), -2I (V _{CCINT} = 0.85V) -1E (V _{CCINT} = 0.85V), -1I (V _{CCINT} = 0.85V) -2LE (V _{CCINT} = 0.85V), -2LE (V _{CCINT} = 0.72V) ¹ -1LI (V _{CCINT} = 0.85V), -1LI (V _{CCINT} = 0.72V) ¹ |
| XCZU11EG | | | -3E (V _{CCINT} = 0.90V) -2E (V _{CCINT} = 0.85V), -2I (V _{CCINT} = 0.85V) -1E (V _{CCINT} = 0.85V), -1I (V _{CCINT} = 0.85V) -2LE (V _{CCINT} = 0.85V), -2LE (V _{CCINT} = 0.72V) ¹ -1LI (V _{CCINT} = 0.85V), -1LI (V _{CCINT} = 0.72V) ¹ |
| XCZU15EG | | | -3E (V _{CCINT} = 0.90V) -2E (V _{CCINT} = 0.85V), -2I (V _{CCINT} = 0.85V) -1E (V _{CCINT} = 0.85V), -1I (V _{CCINT} = 0.85V) -2LE (V _{CCINT} = 0.85V), -2LE (V _{CCINT} = 0.72V) ¹ -1LI (V _{CCINT} = 0.85V), -1LI (V _{CCINT} = 0.72V) ¹ |
| XCZU17EG | | | -3E (V _{CCINT} = 0.90V) -2E (V _{CCINT} = 0.85V), -2I (V _{CCINT} = 0.85V) -1E (V _{CCINT} = 0.85V), -1I (V _{CCINT} = 0.85V) -2LE (V _{CCINT} = 0.85V), -2LE (V _{CCINT} = 0.72V) ¹ -1LI (V _{CCINT} = 0.85V), -1LI (V _{CCINT} = 0.72V) ¹ |
| XCZU19EG | | | -3E (V _{CCINT} = 0.90V) -2E (V _{CCINT} = 0.85V), -2I (V _{CCINT} = 0.85V) -1E (V _{CCINT} = 0.85V), -1I (V _{CCINT} = 0.85V) -2LE (V _{CCINT} = 0.85V), -2LE (V _{CCINT} = 0.72V) ¹ -1LI (V _{CCINT} = 0.85V), -1LI (V _{CCINT} = 0.72V) ¹ |

Table 26: Speed Grade Designations by Device (cont'd)

| Device | Speed Grade, Temperature Ranges, and V _{CCINT} Operating Voltages ¹ | | |
|----------|---|-------------|---|
| | Advance | Preliminary | Production |
| XAZU2EG | | | -1I (V _{CCINT} = 0.85V) -1Q (V _{CCINT} = 0.85V) -1LI (V _{CCINT} = 0.72V) ¹ |
| XAZU3EG | | | -1I (V _{CCINT} = 0.85V) -1Q (V _{CCINT} = 0.85V) -1LI (V _{CCINT} = 0.72V) ¹ |
| XAZU4EV | | | -1I (V _{CCINT} = 0.85V) -1Q (V _{CCINT} = 0.85V) -1LI (V _{CCINT} = 0.72V) ¹ |
| XAZU5EV | | | -1I (V _{CCINT} = 0.85V) -1Q (V _{CCINT} = 0.85V) -1LI (V _{CCINT} = 0.72V) ¹ |
| XAZU7EV | -1I (V _{CCINT} = 0.85V) | | -1Q (V _{CCINT} = 0.85V) |
| XAZU11EG | -1I (V _{CCINT} = 0.85V) | | -1Q (V _{CCINT} = 0.85V) |
| XQZU3EG | | | -2I (V _{CCINT} = 0.85V) -1I (V _{CCINT} = 0.85V) -1M (V _{CCINT} = 0.85V) -1LI (V _{CCINT} = 0.85V), -1LI (V _{CCINT} = 0.72V) ¹ |
| XQZU5EV | | | -2I (V _{CCINT} = 0.85V) -1I (V _{CCINT} = 0.85V) -1M (V _{CCINT} = 0.85V) -1LI (V _{CCINT} = 0.85V), -1LI (V _{CCINT} = 0.72V) ¹ |
| XQZU7EV | | | -2I (V _{CCINT} = 0.85V) -1I (V _{CCINT} = 0.85V) -1M (V _{CCINT} = 0.85V) -1LI (V _{CCINT} = 0.85V), -1LI (V _{CCINT} = 0.72V) ¹ |
| XQZU9EG | | | -2I (V _{CCINT} = 0.85V) -1I (V _{CCINT} = 0.85V) -1M (V _{CCINT} = 0.85V) -1LI (V _{CCINT} = 0.85V), -1LI (V _{CCINT} = 0.72V) ¹ |
| XQZU11EG | | | -2I (V _{CCINT} = 0.85V) -1I (V _{CCINT} = 0.85V) -1M (V _{CCINT} = 0.85V) -1LI (V _{CCINT} = 0.85V), -1LI (V _{CCINT} = 0.72V) ¹ |
| XQZU15EG | | | -2I (V _{CCINT} = 0.85V) -1I (V _{CCINT} = 0.85V) -1M (V _{CCINT} = 0.85V) -1LI (V _{CCINT} = 0.85V), -1LI (V _{CCINT} = 0.72V) ¹ |
| XQZU19EG | | | -2I (V _{CCINT} = 0.85V) -1I (V _{CCINT} = 0.85V) -1M (V _{CCINT} = 0.85V) -1LI (V _{CCINT} = 0.85V), -1LI (V _{CCINT} = 0.72V) ¹ |

Notes:

1. The lowest power -1L and -2L devices, where V_{CCINT} = 0.72V, are listed in the Vivado Design Suite as -1LV and -2LV respectively.

Production Silicon and Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases.

Table 27 lists the production released Zynq UltraScale+ MPSoC, speed grade, and the minimum corresponding supported speed specification version and Vivado software revisions. The Vivado software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 27: Zynq UltraScale+ MPSoC Device Production Software and Speed Specification Release

| Device | Speed Grade and V_{CCINT} Operating Voltages ¹ | | | | | | | | | |
|----------|---|-----------------------------|----|-----|-----|-----|-----------------------------|-------|-----|--|
| | 0.90V | 0.85V | | | | | | 0.72V | | |
| | -3 | -2 | -1 | -1Q | -1M | -2L | -1L | -2L | -1L | |
| XCZU2CG | N/A | Vivado tools 2017.1 v1.10 | | | N/A | N/A | Vivado tools 2017.3.1 v1.16 | | | |
| XCZU2EG | N/A | Vivado tools 2017.1 v1.10 | | | N/A | N/A | Vivado tools 2017.3.1 v1.16 | | | |
| XCZU3CG | N/A | Vivado tools 2017.1 v1.10 | | | N/A | N/A | Vivado tools 2017.3.1 v1.16 | | | |
| XCZU3EG | N/A | Vivado tools 2017.1 v1.10 | | | N/A | N/A | Vivado tools 2017.3.1 v1.16 | | | |
| XCZU4CG | N/A | Vivado tools 2017.4 v1.17 | | | N/A | N/A | Vivado tools 2017.4.1 v1.18 | | | |
| XCZU4EG | Vivado tools 2018.2.1 v1.21 | Vivado tools 2017.4 v1.17 | | | N/A | N/A | Vivado tools 2017.4.1 v1.18 | | | |
| XCZU4EV | Vivado tools 2018.2.1 v1.21 | Vivado tools 2017.4 v1.17 | | | N/A | N/A | Vivado tools 2017.4.1 v1.18 | | | |
| XCZU5CG | N/A | Vivado tools 2017.4 v1.17 | | | N/A | N/A | Vivado tools 2017.4.1 v1.18 | | | |
| XCZU5EG | Vivado tools 2018.2.1 v1.21 | Vivado tools 2017.4 v1.17 | | | N/A | N/A | Vivado tools 2017.4.1 v1.18 | | | |
| XCZU5EV | Vivado tools 2018.2.1 v1.21 | Vivado tools 2017.4 v1.17 | | | N/A | N/A | Vivado tools 2017.4.1 v1.18 | | | |
| XCZU6CG | N/A | Vivado tools 2017.1 v1.10 | | | N/A | N/A | Vivado tools 2017.3.1 v1.16 | | | |
| XCZU6EG | Vivado tools 2018.2.1 v1.21 | Vivado tools 2017.1 v1.10 | | | N/A | N/A | Vivado tools 2017.3.1 v1.16 | | | |
| XCZU7CG | N/A | Vivado tools 2017.4 v1.17 | | | N/A | N/A | Vivado tools 2017.4.1 v1.18 | | | |
| XCZU7EG | Vivado tools 2018.2.1 v1.21 | Vivado tools 2017.4 v1.17 | | | N/A | N/A | Vivado tools 2017.4.1 v1.18 | | | |
| XCZU7EV | Vivado tools 2018.2.1 v1.21 | Vivado tools 2017.4 v1.17 | | | N/A | N/A | Vivado tools 2017.4.1 v1.18 | | | |
| XCZU9CG | N/A | Vivado tools 2017.1 v1.10 | | | N/A | N/A | Vivado tools 2017.3.1 v1.16 | | | |
| XCZU9EG | Vivado tools 2018.2.1 v1.21 | Vivado tools 2017.1 v1.10 | | | N/A | N/A | Vivado tools 2017.3.1 v1.16 | | | |
| XCZU11EG | Vivado tools 2018.1 v1.19 | Vivado tools 2017.3 v1.15 | | | N/A | N/A | Vivado tools 2017.4.1 v1.18 | | | |
| XCZU15EG | Vivado tools 2018.1 v1.19 | Vivado tools 2017.2 v1.12 | | | N/A | N/A | Vivado tools 2017.3.1 v1.16 | | | |
| XCZU17EG | Vivado tools 2018.1 v1.19 | Vivado tools 2017.2.1 v1.13 | | | N/A | N/A | Vivado tools 2017.4 v1.17 | | | |
| XCZU19EG | Vivado tools 2018.1 v1.19 | Vivado tools 2017.2.1 v1.13 | | | N/A | N/A | Vivado tools 2017.4 v1.17 | | | |

Table 27: Zynq UltraScale+ MPSoC Device Production Software and Speed Specification Release (cont'd)

| Device | Speed Grade and V _{CCINT} Operating Voltages ¹ | | | | | | | | |
|----------|--|-----------------------------|---------------------------|-----------------------------|-----------------------------|-----|-----------------------------|-------|-----------------------------|
| | 0.90V | | 0.85V | | | | | 0.72V | |
| | -3 | -2 | -1 | -1Q | -1M | -2L | -1L | -2L | -1L |
| XAZU2EG | N/A | N/A | Vivado tools 2017.3 v1.15 | | N/A | N/A | N/A | N/A | Vivado tools 2017.3.1 v1.16 |
| XAZU3EG | N/A | N/A | Vivado tools 2017.3 v1.15 | | N/A | N/A | N/A | N/A | Vivado tools 2017.3.1 v1.16 |
| XAZU4EV | N/A | N/A | Vivado tools 2017.4 v1.17 | Vivado tools 2018.2 v1.20 | N/A | N/A | N/A | N/A | Vivado tools 2017.4.1 v1.18 |
| XAZU5EV | N/A | N/A | Vivado tools 2017.4 v1.17 | Vivado tools 2018.2 v1.20 | N/A | N/A | N/A | N/A | Vivado tools 2017.4.1 v1.18 |
| XAZU7EV | N/A | N/A | | Vivado tools 2019.1.1 v1.26 | N/A | N/A | N/A | N/A | N/A |
| XAZU11EG | N/A | N/A | | Vivado tools 2019.1.1 v1.26 | N/A | N/A | N/A | N/A | N/A |
| XQZU3EG | N/A | Vivado tools 2018.3 v1.23 | | N/A | Vivado tools 2018.3 v1.23 | N/A | Vivado tools 2018.3 v1.23 | N/A | Vivado tools 2018.3 v1.23 |
| XQZU5EV | N/A | Vivado tools 2018.2.2 v1.22 | | N/A | Vivado tools 2018.2.2 v1.22 | N/A | Vivado tools 2018.2.2 v1.22 | N/A | Vivado tools 2018.2.2 v1.22 |
| XQZU7EV | N/A | Vivado tools 2018.2.2 v1.22 | | N/A | Vivado tools 2018.2.2 v1.22 | N/A | Vivado tools 2018.2.2 v1.22 | N/A | Vivado tools 2018.2.2 v1.22 |
| XQZU9EG | N/A | Vivado tools 2018.3 v1.23 | | N/A | Vivado tools 2018.3 v1.23 | N/A | Vivado tools 2018.3 v1.23 | N/A | Vivado tools 2018.3 v1.23 |
| XQZU11EG | N/A | Vivado tools 2018.3 v1.23 | | N/A | Vivado tools 2018.3 v1.23 | N/A | Vivado tools 2018.3 v1.23 | N/A | Vivado tools 2018.3 v1.23 |
| XQZU15EG | N/A | Vivado tools 2018.2.2 v1.22 | | N/A | Vivado tools 2018.2.2 v1.22 | N/A | Vivado tools 2018.2.2 v1.22 | N/A | Vivado tools 2018.2.2 v1.22 |
| XQZU19EG | N/A | Vivado tools 2018.3 v1.23 | | N/A | Vivado tools 2018.3 v1.23 | N/A | Vivado tools 2018.3 v1.23 | N/A | Vivado tools 2018.3 v1.23 |

Notes:

1. See [Table 3](#) for the complete list of operating voltages by speed grade.

Processor System (PS) Performance Characteristics

Table 28: Processor Performance

| Symbol | Description | Speed Grade | | | Units |
|---------------------|-----------------------------|-------------|------|------|-------|
| | | -3 | -2 | -1 | |
| F _{APUMAX} | Maximum APU clock frequency | 1500 | 1333 | 1200 | MHz |
| F _{RPUMAX} | Maximum RPU clock frequency | 600 | 533 | 500 | MHz |
| F _{GPUMAX} | Maximum GPU clock frequency | 667 | 600 | 600 | MHz |

Table 29: Configuration and Security Unit Performance

| Symbol | Description | Speed Grade | | | Units |
|------------------------|--|-------------|-----|-----|-------|
| | | -3 | -2 | -1 | |
| F _{CSUCIBMAX} | Maximum CSU crypto interface block frequency | 400 | 400 | 400 | MHz |

Table 30: PS DDR Performance

| Memory Standard | Package | DRAM Type | Speed Grade | | | | Units |
|---------------------|---|-----------------------------------|-------------|------|-------------|------|-------|
| | | | -3E | | -2I/-2LI | | |
| | | | -2E/-2LE | | -1I/-1M/-1Q | | |
| | | | -1E | | -1LI | | |
| | | | Min | Max | Min | Max | |
| DDR4 ⁴ | All FFV and FFR packages, FBVB900, SFVC784, and SFRC784 | Single rank component | 664 | 2400 | 1000 | 2400 | Mb/s |
| | | 1 rank DIMM ^{1,2} | 664 | 2133 | 1000 | 2133 | Mb/s |
| | | 2 rank DIMM ^{1,3} | 664 | 1866 | 1000 | 1866 | Mb/s |
| | SFVA625 ⁷ | Single rank component | 664 | 2133 | 1000 | 2133 | Mb/s |
| | | 1 rank DIMM ^{1,2} | 664 | 1866 | 1000 | 1866 | Mb/s |
| | | 2 rank DIMM ^{1,3} | 664 | 1600 | 1000 | 1600 | Mb/s |
| | SBVA484 ⁷ | Single rank component | 664 | 1066 | 1000 | 1066 | Mb/s |
| | | 1 rank DIMM ^{1,2} | 664 | 1066 | 1000 | 1066 | Mb/s |
| | | 2 rank DIMM ^{1,3} | 664 | 1066 | 1000 | 1066 | Mb/s |
| LPDDR4 ⁵ | All FFV and FFR packages, FBVB900, SFVC784, and SFRC784 | Single die package ^{6,7} | 664 | 2400 | 1000 | 2400 | Mb/s |
| | | Dual die package ^{6,7} | 664 | 2133 | 1000 | 2133 | Mb/s |
| | SFVA625 | Single die package ^{6,7} | 664 | 2133 | 1000 | 2133 | Mb/s |
| | | Dual die package ^{6,7} | 664 | 1866 | 1000 | 1866 | Mb/s |
| | SBVA484 | Single die package ^{6,7} | 664 | 1066 | 1000 | 1066 | Mb/s |
| | | Dual die package ^{6,7} | 664 | 1066 | 1000 | 1066 | Mb/s |
| DDR3 | All FFV and FFR packages, FBVB900, SFVC784, and SFRC784 | Single rank component | 664 | 2133 | 1000 | 2133 | Mb/s |
| | | 1 rank DIMM ^{1,2} | 664 | 1866 | 1000 | 1866 | Mb/s |
| | | 2 rank DIMM ^{1,3} | 664 | 1600 | 1000 | 1600 | Mb/s |
| | SFVA625 ⁷ | Single rank component | 664 | 1866 | 1000 | 1866 | Mb/s |
| | | 1 rank DIMM ^{1,2} | 664 | 1600 | 1000 | 1600 | Mb/s |
| | | 2 rank DIMM ^{1,3} | 664 | 1333 | 1000 | 1333 | Mb/s |
| | SBVA484 ⁷ | Single rank component | 664 | 1066 | 1000 | 1066 | Mb/s |
| | | 1 rank DIMM ^{1,2} | 664 | 1066 | 1000 | 1066 | Mb/s |
| | | 2 rank DIMM ^{1,3} | 664 | 1066 | 1000 | 1066 | Mb/s |
| DDR3L | All FFV and FFR packages, FBVB900, SFVC784, and SFRC784 | Single rank component | 664 | 1866 | 1000 | 1866 | Mb/s |
| | | 1 rank DIMM ^{1,2} | 664 | 1600 | 1000 | 1600 | Mb/s |
| | | 2 rank DIMM ^{1,3} | 664 | 1333 | 1000 | 1333 | Mb/s |
| | SFVA625 ⁷ | Single rank component | 664 | 1600 | 1000 | 1600 | Mb/s |
| | | 1 rank DIMM ^{1,2} | 664 | 1333 | 1000 | 1333 | Mb/s |
| | | 2 rank DIMM ^{1,3} | 664 | 1066 | 1000 | 1066 | Mb/s |
| | SBVA484 ⁷ | Single rank component | 664 | 1066 | 1000 | 1066 | Mb/s |
| | | 1 rank DIMM ^{1,2} | 664 | 1066 | 1000 | 1066 | Mb/s |
| | | 2 rank DIMM ^{1,3} | 664 | 1066 | 1000 | 1066 | Mb/s |

Table 30: PS DDR Performance (cont'd)

| Memory Standard | Package | DRAM Type | Speed Grade | | | | Units |
|-----------------|---|---------------------------------|-------------|------|-------------|------|-------|
| | | | -3E | | -2I/-2LI | | |
| | | | -2E/-2LE | | -1I/-1M/-1Q | | |
| | | | -1E | | -1LI | | |
| | | | Min | Max | Min | Max | |
| LPDDR3 | All FFV and FFR packages, FBVB900, SFVC784, and SFRC784 | Single die package ⁸ | 664 | 1600 | 1000 | 1600 | Mb/s |
| | | Dual die package ⁸ | 664 | 1333 | 1000 | 1333 | Mb/s |
| | SFVA625 ⁷ | Single die package ⁸ | 664 | 1333 | 1000 | 1333 | Mb/s |
| | | Dual die package ⁸ | 664 | 1066 | 1000 | 1066 | Mb/s |
| | SBVA484 ⁷ | Single die package ⁸ | 664 | 1066 | 1000 | 1066 | Mb/s |
| | | Dual die package ⁸ | 664 | 1066 | 1000 | 1066 | Mb/s |

Notes:

- Dual in-line memory module (DIMM) includes RDIMM, SODIMM, and UDIMM.
- Includes: 1 rank 1 slot, dual-die package 2 rank.
- Includes: 2 rank 1 slot.
- The JEDEC JESD79-4B standard for DDR4 SDRAM limits the maximum t_{CK} to 1.6 ns. Because of this limitation, Xilinx recommends working with your DRAM vendor to verify support for data rates at or less than 1066 Mb/s.
- LPDDR4 support is only available as a 32-bit interface. Byte-mode LPDDR4 devices are not supported.
- LPDDR4 single die package with ECC is limited to the performance specified for the LPDDR4 dual die package.
- In SBVA484 and SFVA625 packages, DDR4 support is only available as a 32-bit or 16-bit interface and other memory support is available only as a 32-bit interface.
- 64-bit LPDDR3 interface performance values are defined without ECC support.

Table 31: PS NAND NV-DDR Synchronous Performance

| Memory Standard | Mode | Speed Grade | | | Units |
|---------------------|------|-------------|-------|-------|-------|
| | | -3 | -2 | -1 | |
| | | Max | Max | Max | |
| NV-DDR ¹ | 5 | 200 | 200 | 200 | Mb/s |
| | 4 | 166.6 | 166.6 | 166.6 | Mb/s |
| | 3 | 133.3 | 133.3 | 133.3 | Mb/s |
| | 2 | 100 | 100 | 100 | Mb/s |
| | 1 | 66.6 | 66.6 | 66.6 | Mb/s |
| | 0 | 40 | 40 | 40 | Mb/s |

Notes:

- The PS NAND memory controller interface for NV-DDR switching characteristics meets the requirements of the ONFI 3.1 specification.

Table 32: PS NAND SDR Asynchronous Performance

| Memory Standard | Mode | Speed Grade | | | Units |
|--------------------|------|-------------|------|------|-------|
| | | -3 | -2 | -1 | |
| | | Max | Max | Max | |
| SDR ^{1,2} | 5 | 50 | 50 | 50 | Mb/s |
| | 4 | 40 | 40 | 40 | Mb/s |
| | 3 | 33.3 | 33.3 | 33.3 | Mb/s |
| | 2 | 28.5 | 28.5 | 28.5 | Mb/s |
| | 1 | 20 | 20 | 20 | Mb/s |
| | 0 | 10 | 10 | 10 | Mb/s |

Notes:

1. The PS NAND memory controller interface for SDR switching characteristics meets the requirements of the ONFI 3.1 specification.
2. The NAND controller reference clock frequency maximum is 83 MHz.

Table 33: PS-PL Interface Performance

| Symbol | Description | Min | Max | Units |
|---------------------------|---|-----|-----|-------|
| F _{EMIOGEMCLK} | EMIO gigabit Ethernet controller maximum frequency | - | 125 | MHz |
| F _{EMIOSDCLK} | EMIO SD controller maximum frequency | - | 25 | MHz |
| F _{EMIOSPICLK} | EMIO SPI controller maximum frequency | - | 25 | MHz |
| F _{EMIOTRACECLK} | EMIO trace controller maximum frequency | - | 125 | MHz |
| F _{FCIDMACLK} | Flow control interface DMA maximum frequency | - | 333 | MHz |
| F _{AXICLK} | Maximum AXI interface performance | - | 333 | MHz |
| F _{DPLIVEVIDEO} | DisplayPort controller live video interface maximum frequency | - | 300 | MHz |

PS Switching Characteristics

PS Clocks

Table 34: PS Reference Clock Requirements

| Symbol | Description ¹ | Min | Typ | Max | Units |
|-----------------------|--|-----|-----|------|-------|
| T _{RMSJPCLK} | PS_REF_CLK input RMS clock jitter | - | - | 3 | ps |
| T _{PJPCLK} | PS_REF_CLK input period jitter (peak-to-peak) Number of clock cycles = 10,000 | - | - | 50 | ps |
| T _{DCPCLK} | PS_REF_CLK duty cycle | 45 | - | 55 | % |
| T _{RFPSCLK} | PS_REF_CLK rise time (20%-80%) and fall time (80%-20%) | - | - | 2.22 | ns |
| F _{PSCLK} | PS_REF_CLK frequency | 27 | - | 60 | MHz |

Notes:

1. The values in this table are applicable to alternative PS reference clock inputs ALT_REF_CLK, AUX_REF_CLK, and VIDEO_CLK.

Table 35: PS RTC Crystal Requirements

| Symbol | Description ¹ | Min | Typ | Max | Units |
|---------------------|---|-----|------|-----|-------|
| F _{XTAL} | Parallel resonance crystal frequency | - | 32.8 | - | KHz |
| T _{FTXTAL} | Frequency tolerance | -20 | - | 20 | ppm |
| C _{XTAL} | Load capacitance for crystal parallel resonance | - | 12.5 | - | pF |
| R _{ESR} | Crystal ESR (16.8 and 19.2 MHz) | - | 70 | - | KΩ |
| C _{SHUNT} | Crystal shunt capacitance | - | 1.4 | - | pF |

Notes:

1. See the crystal circuit example in the *Zynq UltraScale+ Device Technical Reference Manual (UG1085)*.

Table 36: PS PLL Switching Characteristics

| Symbol | Description | Speed Grade | | | Units |
|--------------------------|------------------------------|-------------|------|------|-------|
| | | -3 | -2 | -1 | |
| T _{LOCKPSPLL} | PLL maximum lock time | 100 | 100 | 100 | μs |
| F _{PSPLLMAX} | PLL maximum output frequency | 1600 | 1600 | 1600 | MHz |
| F _{PSPLLMIN} | PLL minimum output frequency | 750 | 750 | 750 | MHz |
| F _{PSPLLVCOMAX} | PLL maximum VCO frequency | 3000 | 3000 | 3000 | MHz |
| F _{PSPLLVCOMIN} | PLL minimum VCO frequency | 1500 | 1500 | 1500 | MHz |

Table 37: PS Reset Assertion Timing Requirements

| Symbol | Description | Min | Typ | Max | Units |
|--------------------|---|-----|-----|-----|-------------------------|
| T _{PSPOR} | Required PS_POR_B assertion time ¹ | 10 | - | - | μs |
| T _{PSRST} | Required PS_SRST_B assertion time | 3 | - | - | PS_REF_CLK Clock Cycles |

Notes:

1. PS_POR_B must be asserted Low at power-up and continue to be asserted for a duration of T_{PSPOR} after all the PS supply voltages reach minimum levels. PS_POR_B must be asserted Low for the duration of T_{POR} when the PS and PL power-up at the same time and the application uses both the PS and PL after power-up.

Table 38: PS Clocks Switching Characteristics

| Symbol | Description | Speed Grade | | | Units |
|---------------------------------|--|-------------|-----|-----|-------|
| | | -3 | -2 | -1 | |
| F _{TOPSW_MAINMAX} | FPD AXI interconnect clock maximum frequency | 600 | 533 | 533 | MHz |
| F _{TOPSW_LSBUSMAX} | FPD APB bus clock maximum frequency | 100 | 100 | 100 | MHz |
| F _{GDMAMAX} | FPD-DMA controller clock maximum frequency | 600 | 600 | 600 | MHz |
| F _{DPMAMAX} | DisplayPort controller clock maximum frequency | 600 | 600 | 600 | MHz |
| F _{LPD_SWITCH_CTRLMAX} | LPD AXI interconnect clock maximum frequency | 600 | 500 | 500 | MHz |
| F _{LPD_LSBUS_CTRLMAX} | LPD APB bus clock maximum frequency | 100 | 100 | 100 | MHz |
| F _{ADMAMAX} | LPD-DMA maximum frequency | 600 | 500 | 500 | MHz |
| F _{APLL_TO_LPDMAX} | APLL_TO_LPD maximum frequency | 533 | 533 | 533 | MHz |
| F _{DPLL_TO_LPDMAX} | DPLL_TO_LPD maximum frequency | 533 | 533 | 533 | MHz |
| F _{VPDLL_TO_LPDMAX} | VPDLL_TO_LPD maximum frequency | 533 | 533 | 533 | MHz |
| F _{IOPLL_TO_FPDMAX} | IOPLL_TO_FPD maximum frequency | 533 | 533 | 533 | MHz |
| F _{RPDLL_TO_FPDMAX} | RPDLL_TO_FPD maximum frequency | 533 | 533 | 533 | MHz |

PS Configuration

Table 39: Processor Configuration Access Port Switching Characteristics

| Symbol | Description | Speed Grade and V _{CCINT} Operating Voltages | | | | | Units |
|---------------------|--|---|-----|-------|-----|-------|-------|
| | | 0.90V | | 0.85V | | 0.72V | |
| | | -3 | -2 | -1 | -2 | -1 | |
| F _{PCAPCK} | Maximum processor configuration access port (PCAP) frequency | 200 | 200 | 200 | 150 | 150 | MHz |

Table 40: Boundary-Scan Port Switching Characteristics

| Symbol | Description | Speed Grade and V _{CCINT} Operating Voltages | | | | | Units |
|--|--------------------------------|---|---------|---------|---------|---------|---------|
| | | 0.90V | | 0.85V | | 0.72V | |
| | | -3 | -2 | -1 | -2 | -1 | |
| F _{TCK} | JTAG clock maximum frequency | 25 | 25 | 25 | 15 | 15 | MHz |
| T _{TAPTCK} /T _{TCKTAP} | TMS and TDI setup and hold | 4.0/2.0 | 4.0/2.0 | 4.0/2.0 | 5.0/2.0 | 5.0/2.0 | ns, Min |
| T _{TCKTDO} | TCK falling edge to TDO output | 16.1 | 16.1 | 16.1 | 24 | 24 | ns, Max |

Notes:

- The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength.

PS Interface Specifications

PS Quad-SPI Controller Interface

Table 41: Generic Quad-SPI Interface

| Symbol | Description ¹ | Load Conditions ² | Min | Max | Units |
|---|---|------------------------------|------|------|-------|
| Quad-SPI device clock frequency operating at 150 MHz. Loopback enabled. LVCMOS 1.8V or LVCMOS 3.3V I/O standard. | | | | | |
| T _{DCQSPICLK1} | Quad-SPI clock duty cycle | 15 pF | 45 | 55 | % |
| T _{QSPISSCLK1} | Slave select asserted to next clock edge | 15 pF | 5.0 | – | ns |
| T _{QSPISCLKSS1} | Clock edge to slave select deasserted | 15 pF | 5.0 | – | ns |
| T _{QSPICKO1} | Clock to output delay, all outputs | 15 pF | 2.9 | 4.5 | ns |
| T _{QSPIDCK1} | Setup time, all inputs | 15 pF | 0.9 | – | ns |
| T _{QSPICKD1} | Hold time, all inputs | 15 pF | 1.0 | – | ns |
| F _{QSPICLK1} | Quad-SPI device clock frequency | 15 pF | – | 150 | MHz |
| F _{QSPIREFCLK1} | Quad-SPI reference clock frequency | 15 pF | – | 300 | MHz |
| Quad-SPI device clock frequency operating at 100 MHz. Loopback enabled. LVCMOS 1.8V or LVCMOS 3.3V I/O standard. | | | | | |
| T _{DCQSPICLK2} | Quad-SPI clock duty cycle | 15 pF | 45 | 55 | % |
| | | 30 pF | 45 | 55 | % |
| T _{QSPISSCLK2} | Slave select asserted to next clock edge | 15 pF | 5.0 | – | ns |
| | | 30 pF | 5.0 | – | ns |
| T _{QSPISCLKSS2} | Clock edge to slave select deasserted | 15 pF | 5.0 | – | ns |
| | | 30 pF | 5.0 | – | ns |
| T _{QSPICKO2} | Clock to output delay, all outputs | 15 pF | 3.2 | 7.4 | ns |
| | | 30 pF | 3.2 | 7.4 | ns |
| T _{QSPIDCK2} | Setup time, all inputs | 15 pF | 2.3 | – | ns |
| | | 30 pF | 2.3 | – | ns |
| T _{QSPICKD2} | Hold time, all inputs | 15 pF | 0.0 | – | ns |
| | | 30 pF | 0.0 | – | ns |
| F _{QSPICLK2} | Quad-SPI device clock frequency | 15 pF | – | 100 | MHz |
| | | 30 pF | – | 100 | MHz |
| F _{QSPIREFCLK2} | Quad-SPI reference clock frequency | 15 pF | – | 200 | MHz |
| | | 30 pF | – | 200 | MHz |
| Quad-SPI device clock frequency operating at 40 MHz. Loopback disabled. LVCMOS 1.8V I/O standard. | | | | | |
| T _{DCQSPICLK3} | Quad-SPI clock duty cycle | 15 pF | 45 | 55 | % |
| | | 30 pF | 45 | 55 | % |
| T _{QSPISSCLK3} | Slave select asserted to next clock edge ³ | 15 pF | 7.0 | – | ns |
| | | 30 pF | 7.0 | – | ns |
| T _{QSPISCLKSS3} | Clock edge to slave select deasserted | 15 pF | 7.0 | – | ns |
| | | 30 pF | 7.0 | – | ns |
| T _{QSPICKO3} | Clock to output delay, all outputs | 15 pF | 5.2 | 14.8 | ns |
| | | 30 pF | 5.2 | 14.8 | ns |
| T _{QSPIDCK3} | Setup time, all inputs | 15 pF | 13.4 | – | ns |
| | | 30 pF | 14.1 | – | ns |

Table 41: Generic Quad-SPI Interface (cont'd)

| Symbol | Description ¹ | Load Conditions ² | Min | Max | Units |
|--|---|------------------------------|------|------|-------|
| T _{QSPICKD3} | Hold time, all inputs | 15 pF | 0.0 | - | ns |
| | | 30 pF | 0.0 | - | ns |
| F _{QSPIREFCLK3} | Quad-SPI reference clock frequency | 15 pF | - | 160 | MHz |
| | | 30 pF | - | 160 | MHz |
| F _{QSPICLK3} | Quad-SPI clock frequency | 15 pF | - | 40 | MHz |
| | | 30 pF | - | 40 | MHz |
| Quad-SPI device clock frequency operating at 40 MHz. Loopback disabled. LVCMOS 3.3V I/O standard. | | | | | |
| T _{DCQSPICLK4} | Quad-SPI clock duty cycle | 15 pF | 45 | 55 | % |
| | | 30 pF | 45 | 55 | % |
| T _{QSPISSECLK4} | Slave select asserted to next clock edge ³ | 15 pF | 7.0 | - | ns |
| | | 30 pF | 7.0 | - | ns |
| T _{QSPISCLKSS4} | Clock edge to slave select deasserted | 15 pF | 7.0 | - | ns |
| | | 30 pF | 7.0 | - | ns |
| T _{QSPICKO4} | Clock to output delay, all outputs | 15 pF | 5.2 | 14.8 | ns |
| | | 30 pF | 5.2 | 14.8 | ns |
| T _{QSPIDCK4} | Setup time, all inputs | 15 pF | 13.9 | - | ns |
| | | 30 pF | 14.9 | - | ns |
| T _{QSPICKD4} | Hold time, all inputs | 15 pF | 0.0 | - | ns |
| | | 30 pF | 0.0 | - | ns |
| F _{QSPIREFCLK4} | Quad-SPI reference clock frequency | 15 pF | - | 160 | MHz |
| | | 30 pF | - | 160 | MHz |
| F _{QSPICLK4} | Quad-SPI clock frequency | 15 pF | - | 40 | MHz |
| | | 30 pF | - | 40 | MHz |

Notes:

1. The test conditions are configured for the generic Quad-SPI interface at 150/100 MHz with a 12 mA drive strength and fast slew rate.
2. 30 pF loads are for dual-parallel stacked or stacked modes.
3. T_{QSPISSECLK3} and T_{QSPISSECLK4} are only valid when two reference clock cycles are programmed between the chip select and clock.

Table 42: Linear Quad-SPI Interface

| Symbol | Description ¹ | Load Conditions ² | Min | Max | Units |
|---|---|------------------------------|-----|-----|-------|
| Quad-SPI device clock frequency operating at 100 MHz. Loopback enabled. LVCMOS 1.8V or LVCMOS 3.3V I/O standard. | | | | | |
| T _{DCQSPICLK5} | Quad-SPI clock duty cycle | 15 pF | 45 | 55 | % |
| | | 30 pF | 45 | 55 | % |
| T _{QSPISSECLK5} | Slave select asserted to next clock edge ³ | 15 pF | 5.0 | - | ns |
| | | 30 pF | 5.0 | - | ns |
| T _{QSPISCLKSS5} | Clock edge to slave select deasserted | 15 pF | 5.0 | - | ns |
| | | 30 pF | 5.0 | - | ns |
| T _{QSPICKO5} | Clock to output delay, all outputs | 15 pF | 3.2 | 7.4 | ns |
| | | 30 pF | 3.2 | 7.4 | ns |
| T _{QSPIDCK5} | Setup time, all inputs | 15 pF | 2.4 | - | ns |
| | | 30 pF | 2.4 | - | ns |

Table 42: Linear Quad-SPI Interface (cont'd)

| Symbol | Description ¹ | Load Conditions ² | Min | Max | Units |
|--|--|------------------------------|------|------|-------|
| T _{QSPICKD5} | Hold time, all inputs | 15 pF | 0.0 | - | ns |
| | | 30 pF | 0.0 | - | ns |
| F _{QSPIREFCLK5} | Quad-SPI reference clock frequency | 15 pF | - | 200 | MHz |
| | | 30 pF | - | 200 | MHz |
| F _{QSPICLK5} | Quad-SPI device clock frequency | 15 pF | - | 100 | MHz |
| | | 30 pF | - | 100 | MHz |
| Quad-SPI device clock frequency operating at 40 MHz. Loopback disabled. LVCMOS 1.8V I/O standard. | | | | | |
| T _{DCQSPICLK6} | Quad-SPI clock duty cycle | 15 pF | 45 | 55 | % |
| | | 30 pF | 45 | 55 | % |
| T _{QSPISSSCLK6} | Slave select asserted to next clock edge | 15 pF | 7.0 | - | ns |
| | | 30 pF | 7.0 | - | ns |
| T _{QSPISCLKSS6} | Clock edge to slave select deasserted | 15 pF | 7.0 | - | ns |
| | | 30 pF | 7.0 | - | ns |
| T _{QSPICKO6} | Clock to output delay, all outputs | 15 pF | 5.2 | 14.8 | ns |
| | | 30 pF | 5.2 | 14.8 | ns |
| T _{QSPIDCK6} | Setup time, all inputs | 15 pF | 13.4 | - | ns |
| | | 30 pF | 13.4 | - | ns |
| T _{QSPICKD6} | Hold time, all inputs | 15 pF | 0.0 | - | ns |
| | | 30 pF | 0.0 | - | ns |
| F _{QSPIREFCLK6} | Quad-SPI reference clock frequency | 15 pF | - | 160 | MHz |
| | | 30 pF | - | 160 | MHz |
| F _{QSPICLK6} | Quad-SPI device clock frequency | 15 pF | - | 40 | MHz |
| | | 30 pF | - | 40 | MHz |
| Quad-SPI device clock frequency operating at 40 MHz. Loopback disabled. LVCMOS 3.3V I/O standard. | | | | | |
| T _{DCQSPICLK7} | Quad-SPI clock duty cycle | 15 pF | 45 | 55 | % |
| | | 30 pF | 45 | 55 | % |
| T _{QSPISSSCLK7} | Slave select asserted to next clock edge | 15 pF | 7.0 | - | ns |
| | | 30 pF | 7.0 | - | ns |
| T _{QSPISCLKSS7} | Clock edge to slave select deasserted | 15 pF | 7.0 | - | ns |
| | | 30 pF | 7.0 | - | ns |
| T _{QSPICKO7} | Clock to output delay, all outputs | 15 pF | 5.2 | 14.8 | ns |
| | | 30 pF | 5.2 | 14.8 | ns |
| T _{QSPIDCK7} | Setup time, all inputs | 15 pF | 14.0 | - | ns |
| | | 30 pF | 14.0 | - | ns |
| T _{QSPICKD7} | Hold time, all inputs | 15 pF | 0.0 | - | ns |
| | | 30 pF | 0.0 | - | ns |
| F _{QSPIREFCLK7} | Quad-SPI reference clock frequency | 15 pF | - | 160 | MHz |
| | | 30 pF | - | 160 | MHz |

Table 42: Linear Quad-SPI Interface (cont'd)

| Symbol | Description ¹ | Load Conditions ² | Min | Max | Units |
|-----------------------|---------------------------------|------------------------------|-----|-----|-------|
| F _{QSPICLK7} | Quad-SPI device clock frequency | 15 pF | - | 40 | MHz |
| | | 30 pF | - | 40 | MHz |

Notes:

1. The test conditions are configured for the linear Quad-SPI interface at 100 MHz with a 12 mA drive strength and fast slew rate.
2. 30 pF loads are for stacked modes.
3. T_{QSPISSCLK5} is only valid when two reference clock cycles are programmed between chip select and clock.

PS USB Interface

Table 43: ULPI Interface

| Symbol | Description ¹ | Min | Max | Units |
|----------------------|---|-----|------|-------|
| T _{ULPIDCK} | Input setup to ULPI clock, all inputs | 4.5 | - | ns |
| T _{ULPICKD} | Input hold to ULPI clock, all inputs | 0 | - | ns |
| T _{ULPICKO} | ULPI clock to output valid, all outputs | 2.0 | 8.86 | ns |
| F _{ULPICLK} | ULPI reference clock frequency | - | 60 | MHz |

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.

PS Gigabit Ethernet Controller Interface

Table 44: RGMII Interface

| Symbol | Description ¹ | Min | Max | Units |
|---------------------------|---------------------------------------|------|-----|-------|
| T _{DCGEMTXCLK} | Transmit clock duty cycle | 45 | 55 | % |
| T _{GEMTXCKO} | TXD output clock to out time | -0.5 | 0.5 | ns |
| T _{GEMRXDCK} | RXD input setup time | 0.8 | - | ns |
| T _{GEMRXCKD} | RXD input hold time | 0.8 | - | ns |
| T _{MDIOCLK} | MDC output clock period | 400 | - | ns |
| T _{MDIOCKL} | MDC low time | 160 | - | ns |
| T _{MDIOCKH} | MDC high time | 160 | - | ns |
| T _{MDIODCK} | MDIO input data setup time | 80 | - | ns |
| T _{MDIOCKD} | MDIO input data hold time | 0.0 | - | ns |
| T _{MDIOCKO} | MDIO output data delay time | -1.0 | 15 | ns |
| F _{GETXCLK} | RGMII_TX_CLK transmit clock frequency | - | 125 | MHz |
| F _{GERXCLK} | RGMII_RX_CLK receive clock frequency | - | 125 | MHz |
| F _{ENET_REF_CLK} | Ethernet reference clock frequency | - | 125 | MHz |

Notes:

1. The test conditions are configured to the LVCMOS 2.5V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.

PS SD/SDIO Controller Interface

Table 45: SD/SDIO Interface

| Symbol | Description ¹ | Min | Max | Units |
|--|---|------|------|-------|
| SD/SDIO Interface DDR50 Mode | | | | |
| T _{DCDDRCLK} | SD device clock duty cycle | 45 | 55 | % |
| T _{SDDDRCKO1} | Clock to output delay, data ² | 1.0 | 6.8 | ns |
| T _{SDDDRIVW} | Input valid data window ³ | 3.5 | - | ns |
| T _{SDDDRDCK2} | Input setup time, command | 4.7 | - | ns |
| T _{SDDDRCKD2} | Input hold time, command | 1.5 | - | ns |
| T _{SDDDRCKO2} | Clock to output delay, command | 1.0 | 13.8 | ns |
| F _{SDDDRCLK} | High-speed mode SD device clock frequency | - | 50 | MHz |
| SD/SDIO Interface SDR104 | | | | |
| T _{DCSDHCLK1} | SD device clock duty cycle | 40 | 60 | % |
| T _{SSDRCKO1} | Clock to output delay, all output ² | 1.0 | 3.2 | ns |
| T _{SSDR1IVW} | Input valid data window ³ | 0.5 | - | UI |
| F _{SSDRCLK1} | SDR104 mode device clock frequency | - | 200 | MHz |
| SD/SDIO Interface SDR50/25 | | | | |
| T _{DCSDHCLK2} | SD device clock duty cycle | 40 | 60 | % |
| T _{SSDRCKO2} | Clock to output delay, all outputs ² | 1.0 | 6.8 | ns |
| T _{SSDR2IVW} | Input valid data window ³ | 0.3 | - | UI |
| F _{SSDRCLK2} | SDR50 mode device clock frequency | - | 100 | MHz |
| | SDR25 mode device clock frequency | - | 50 | MHz |
| SD/SDIO Interface SDR12 | | | | |
| T _{DCSDHCLK3} | SD device clock duty cycle | 40 | 60 | % |
| T _{SSDRCKO3} | Clock to output delay, all outputs | 1.0 | 36.8 | ns |
| T _{SSDRDCK3} | Input setup time, all inputs | 10.0 | - | ns |
| T _{SSDRCKD3} | Input hold time, all inputs | 1.5 | - | ns |
| F _{SSDRCLK3} | SDR12 mode device clock frequency | - | 25 | MHz |
| SD/SDIO Interface High-Speed Mode | | | | |
| T _{DCSDHCLK} | SD device clock duty cycle | 47 | 53 | % |
| T _{SDHCKO} | Clock to output delay, all outputs ² | 2.2 | 13.8 | ns |
| T _{SDHSDIVW} | Input valid data window ³ | 0.35 | - | UI |
| F _{SDHCLK} | High-speed mode SD device clock frequency | - | 50 | MHz |
| SD/SDIO Interface Standard Mode | | | | |
| T _{DCSDCLK} | SD device clock duty cycle | 45 | 55 | % |
| T _{SDCKO} | Clock to output delay, all outputs | -2.0 | 4.5 | ns |
| T _{SDSDCK} | Input setup time, all inputs | 2.0 | - | ns |
| T _{SDCKD} | Input hold time, all inputs | 2.0 | - | ns |
| F _{SDIDCLK} | Clock frequency in identification mode | - | 400 | KHz |

Table 45: SD/SDIO Interface (cont'd)

| Symbol | Description ¹ | Min | Max | Units |
|---------------------|------------------------------------|-----|-----|-------|
| F _{SDSCLK} | Standard SD device clock frequency | - | 19 | MHz |

Notes:

1. The test conditions SD/SDIO standard mode (default speed mode) use an 8 mA drive strength, fast slew rate, and a 30 pF load. For SD/SDIO high-speed mode, the test conditions use a 12 mA drive strength, fast slew rate, and a 30 pF load. For other SD/SDIO modes, the test conditions use a 12 mA drive strength, fast slew rate, and a 15 pF load.
2. This specification is achieved using pre-determined DLL tuning.
3. This specification is required for capturing input data using DLL tuning.

PS eMMC Standard Interface

Table 46: eMMC Standard Interface

| Symbol | Description ¹ | Min | Max | Units |
|--------------------------------------|---|------|------|-------|
| eMMC Standard Interface | | | | |
| T _{DCEMMCHSCLK} | eMMC clock duty cycle | 45 | 55 | % |
| T _{EMMCHSCKO} | Clock to output delay, all outputs | -2.0 | 4.5 | ns |
| T _{EMMCHSDCK} | Input setup time, all inputs | 2.0 | - | ns |
| T _{EMMCHSCKD} | Input hold time, all inputs | 2.0 | - | ns |
| F _{EMMCHSCLK} | eMMC clock frequency | - | 25 | MHz |
| eMMC High-Speed SDR Interface | | | | |
| T _{DCEMMCHSCLK} | eMMC high-speed SDR clock duty cycle | 45 | 55 | % |
| T _{EMMCHSCKO} | Clock to output delay, all outputs ² | 3.2 | 16.8 | ns |
| T _{EMMCHSDIVW} | Input valid data window ³ | 0.4 | - | UI |
| F _{EMMCHSCLK} | eMMC high speed SDR clock frequency | - | 50 | MHz |
| eMMC High-Speed DDR Interface | | | | |
| T _{DCEMMCDRCLK} | eMMC high-speed DDR clock duty cycle | 45 | 55 | % |
| T _{EMMCDRSCO1} | Data clock to output delay ² | 2.7 | 7.3 | ns |
| T _{EMMCDRIVW} | Input valid data window ³ | 3.5 | - | ns |
| T _{EMMCDRSCO2} | Command clock to output delay | 3.2 | 16 | ns |
| T _{EMMCDRDCK2} | Command input setup time | 3.9 | - | ns |
| T _{EMMCDRCKD2} | Command input hold time | 2.5 | - | ns |
| F _{EMMCDRCLK} | eMMC high-speed DDR clock frequency | - | 50 | MHz |
| eMMC HS200 Interface | | | | |
| T _{DCEMMCHS200CLK} | eMMC HS200 clock duty cycle | 40 | 60 | % |
| T _{EMMCHS200CKO} | Clock to output delay, all outputs ² | 1.0 | 3.4 | ns |
| T _{EMMCHSDR1IVW} | Input valid data window ³ | 0.4 | - | UI |
| F _{EMMCHS200CLK} | eMMC HS200 clock frequency | - | 200 | MHz |

Notes:

1. The test conditions for eMMC standard mode use an 8 mA drive strength, fast slew rate, and a 30 pF load. For eMMC high-speed mode, the test conditions use a 12 mA drive strength, fast slew rate, and a 30 pF load. For other eMMC modes, the test conditions use a 12 mA drive strength, fast slew rate, and a 15 pF load.
2. This specification is achieved using pre-determined DLL tuning.
3. This specification is required for capturing input data using DLL tuning.

PS I2C Controller Interface

Table 47: I2C Interface

| Symbol | Description ¹ | Min | Max | Units |
|------------------------------------|--------------------------|-----|------|-------|
| I2C Fast-mode Interface | | | | |
| T _{I2CFCKL} | SCL Low time | 1.3 | - | μs |
| T _{I2CFCKH} | SCL High time | 0.6 | - | μs |
| T _{I2CFCKO} | SDA clock to out delay | - | 900 | ns |
| T _{I2CFDCK} | SDA input setup time | 100 | - | ns |
| F _{I2CFCLK} | SCL clock frequency | - | 400 | KHz |
| I2C Standard-mode Interface | | | | |
| T _{I2CSCKL} | SCL Low time | 4.7 | - | μs |
| T _{I2CSCKH} | SCL High time | 4.0 | - | μs |
| T _{I2CSCKO} | SDA clock to out delay | - | 3450 | ns |
| T _{I2CSDCK} | SDA input setup time | 250 | - | ns |
| F _{I2CSCLK} | SCL clock frequency | - | 100 | KHz |

Notes:

- The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.

PS SPI Controller Interface

Table 48: SPI Interfaces

| Symbol | Description ¹ | Min | Max | Units |
|-----------------------------|---|----------------|------|---------------------------------|
| SPI Master Interface | | | | |
| T _{DCMSPICLK} | SPI master mode clock duty cycle | 45 | 55 | % |
| T _{MSPISSCLK} | Slave select asserted to first active clock edge | 1 ² | - | F _{SPI_REF_CLK} cycles |
| T _{MSPISCLKSS} | Last active clock edge to slave select deasserted | 1 ² | - | F _{SPI_REF_CLK} cycles |
| T _{MSPIDCK} | Input setup time for MISO | -2.0 | - | ns |
| T _{MSPICKD} | Input hold time for MISO | 0.3 | - | F _{MSPICLK} cycles |
| T _{MSPICKO} | MOSI and slave select clock to out delay | -2.0 | 5.0 | ns |
| F _{MSPICLK} | SPI master device clock frequency | - | 50 | MHz |
| F _{SPI_REF_CLK} | SPI reference clock frequency | - | 200 | MHz |
| SPI Slave Interface | | | | |
| T _{SSPISSCLK} | Slave select asserted to first active clock edge | 2 | - | F _{SPI_REF_CLK} cycles |
| T _{SSPISCLKSS} | Last active clock edge to slave select deasserted | 2 | - | F _{SPI_REF_CLK} cycles |
| T _{SSPIDCK} | Input setup time for MOSI | 5.0 | - | ns |
| T _{SSPICKD} | Input hold time for MOSI | 1 | - | F _{SPI_REF_CLK} cycles |
| T _{SSPICKO} | MISO clock to out delay | 0.0 | 13.0 | ns |
| F _{SSPICLK} | SPI slave mode device clock frequency | - | 25 | MHz |

Table 48: SPI Interfaces (cont'd)

| Symbol | Description ¹ | Min | Max | Units |
|--------------------------|-------------------------------|-----|-----|-------|
| F _{SPI_REF_CLK} | SPI reference clock frequency | - | 200 | MHz |

Notes:

- The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 30 pF load.
- Valid when two SPI_REF_CLK delays are programmed between CS and CLK for T_{MSPISSECLK}, and between CLK and CS for T_{MSPISCLKSS} in the SPI delay_reg0 register.

PS CAN Controller Interface

Table 49: CAN Interface

| Symbol | Description ¹ | Min | Max | Units |
|--------------------------|--|-----|-----|-------|
| T _{PWCANRX} | Receive pulse width | 1.0 | - | μs |
| T _{PWCANTX} | Transmit pulse width | 1.0 | - | μs |
| F _{CAN_REF_CLK} | Internally sourced CAN reference clock frequency | - | 100 | MHz |
| | Externally sourced CAN reference clock frequency | - | 40 | MHz |

Notes:

- The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.

PS DAP Interface

Table 50: DAP Interface

| Symbol | Description ^{1,2} | Min | Max | Units |
|----------------------|----------------------------|-----|-------|-------|
| T _{PDAPDCK} | PS DAP input setup time | 3.0 | - | ns |
| T _{PDAPCKD} | PS DAP input hold time | 2.0 | - | ns |
| T _{PDAPCKO} | PS DAP clock to out delay | - | 10.86 | ns |
| F _{PDAPCLK} | PS DAP clock frequency | - | 44 | MHz |

Notes:

- The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.
- PS DAP interface signals connect to MIO pins.

PS UART Interface

Table 51: UART Interface

| Symbol | Description ¹ | Min | Max | Units |
|---------------------------|--------------------------------|-----|------|-------|
| BAUD _{TXMAX} | Transmit baud rate | - | 6.25 | Mb/s |
| BAUD _{RXMAX} | Receive baud rate | - | 6.25 | Mb/s |
| F _{UART_REF_CLK} | UART reference clock frequency | - | 100 | MHz |

Notes:

- The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.

PS General Purpose I/O Interface

Table 52: General Purpose I/O (GPIO) Interface

| Symbol | Description | Min | Max | Units |
|----------------------|------------------------|---------------------------------------|-----|-------|
| T _{PWGPIOH} | Input High pulse width | $10 \times 1/F_{LPD_LSBUS_CTRLMAX}$ | - | μs |
| T _{PWGPIOL} | Input Low pulse width | $10 \times 1/F_{LPD_LSBUS_CTRLMAX}$ | - | μs |

PS Trace Interface

Table 53: Trace Interface

| Symbol | Description ¹ | Min | Max | Units |
|-----------------------|--|------|-----|-------|
| T _{TCECKO} | Trace clock to output delay, all outputs | -0.5 | 0.5 | ns |
| T _{DCTCECLK} | Trace clock duty cycle | 45 | 55 | % |
| F _{TCECLK} | Trace clock frequency | - | 125 | MHz |

Notes:

- The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.

PS Triple-timer Counter Interface

Table 54: Triple-timer Counter Interface

| Symbol | Description | Min | Max | Units |
|------------------------|---|--|-----------------------------|-------|
| T _{PWTTCOCLK} | Triple-timer counter output clock pulse width | 60.4 | - | ns |
| F _{TTCOCLK} | Triple-timer counter output clock frequency | - | 16.5 | MHz |
| T _{TTICLKL} | Triple-timer counter input clock high pulse width | $1.5 \times 1/F_{LPD_LSBUS_CTRLMAX}$ | - | ns |
| T _{TTICLKH} | Triple-timer counter input clock low pulse width | $1.5 \times 1/F_{LPD_LSBUS_CTRLMAX}$ | - | ns |
| F _{TTICLCK} | Triple-timer counter input clock frequency | - | $F_{LPD_LSBUS_CTRLMAX}/3$ | MHz |

Notes:

- All timing values assume an ideal external input clock. Your actual timing budget must account for additional external clock jitter.

PS Watchdog Timer Interface

Table 55: Watchdog Timer Interface

| Symbol | Description | Min | Max | Units |
|--------------------|--------------------------------------|-----|-----|-------|
| F _{WDCLK} | Watchdog timer input clock frequency | - | 100 | MHz |

PS-GTR Transceiver

Table 56: PS-GTR Transceiver DC Specifications

| Symbol | DC Parameter | Conditions | Min | Typ | Max | Units |
|----------------------|---|--|-----------------------------------|-----|--------------------------|-------|
| DV _{PPIN} | Differential peak-to-peak input voltage (external AC coupled) | | 100 | – | 1200 | mV |
| V _{IN} | Single-ended input voltage. Voltage measured at the pin referenced to GND | | 75 | – | V _{PS_MGTRAVCC} | mV |
| V _{CMIN} | Common mode input voltage | | – | 0 | – | mV |
| DV _{PPOUT} | Differential peak-to-peak output voltage ¹ | Transmitter output swing is set to maximum value | 800 | – | – | mV |
| V _{CMOUTAC} | Common mode output voltage: AC coupled (equation based) | | $V_{PS_MGTRAVCC} - D_{VPPOUT}/2$ | | | mV |
| R _{IN} | Differential input resistance | | – | 100 | – | Ω |
| R _{OUT} | Differential output resistance | | – | 100 | – | Ω |
| R _{MGTRREF} | Resistor value between calibration resistor pin to GND | | 497.5 | 500 | 502.5 | Ω |
| T _{OSKEW} | Transmitter output pair (TXP and TXN) intra-pair skew (All packages) | | – | – | 20 | ps |
| C _{EXT} | Recommended external AC coupling capacitor ² | | – | 100 | – | nF |

Notes:

1. The output swing and pre-emphasis levels are programmable using the attributes discussed in the *Zynq UltraScale+ Device Technical Reference Manual (UG1085)*, and can result in values lower than reported in this table.
2. Other values can be used as appropriate to conform to specific protocols and standards.

Table 57: PS-GTR Transceiver Clock DC Input Level Specification

| Symbol | DC Parameter | Min | Typ | Max | Units |
|--------------------|---|-----|-----|------|-------|
| V _{IDIFF} | Differential peak-to-peak input voltage | 250 | – | 2000 | mV |
| R _{IN} | Differential input resistance | – | 100 | – | Ω |
| C _{EXT} | Required external AC coupling capacitor | – | 10 | – | nF |

Table 58: PS-GTR Transceiver Performance

| Symbol | Description | Speed Grade | | | Units |
|---------------------|--------------------------|-------------|------|------|-------|
| | | -3 | -2 | -1 | |
| F _{GTRMAX} | PS-GTR maximum line rate | 6.0 | 6.0 | 6.0 | Gb/s |
| F _{GTRMIN} | PS-GTR minimum line rate | 1.25 | 1.25 | 1.25 | Gb/s |

Table 59: PS-GTR Transceiver PLL/Lock Time Adaptation

| Symbol | Description | Min | Typ | Max | Units |
|--------------------|--|-----|-----|----------------------|-------|
| T _{LOCK} | Initial PLL lock | – | – | 0.11 | ms |
| T _{DLOCK} | Clock recovery phase acquisition and adaptation time | – | – | 24 x 10 ⁶ | UI |

Table 60: PS-GTR Transceiver Reference Clock Switching Characteristics

| Symbol | Description | Conditions | All Speed Grades | | | Units |
|--------------------|---------------------------------------|--------------------------------------|-----------------------------|-----|------|-------|
| | | | Min | Typ | Max | |
| F _{GCLK} | Reference clock frequencies supported | PCI Express® | 100 MHz | | | |
| | | SATA | 125 MHz or 150 MHz | | | |
| | | USB 3.0 | 26 MHz, 52 MHz, or 100 MHz | | | |
| | | DisplayPort | 27 MHz, 108 MHz, or 135 MHz | | | |
| | | SGMII | 125 MHz | | | |
| T _{RCLK} | Reference clock rise time | 20% - 80% | - | 200 | - | ps |
| T _{FCLK} | Reference clock fall time | 80% - 20% | - | 200 | - | ps |
| T _{DCREF} | Reference clock duty cycle | Transceiver PLL only | 40 | - | 60 | % |
| | | USB 3.0 with reference clock <40 MHz | 47.5 | - | 52.5 | % |

Table 61: PS-GTR Transceiver Reference Clock Oscillator Selection Phase Noise Mask

| Symbol | Description ¹ | Offset Frequency | Min | Typ | Max | Units |
|---|---|------------------|-----|------|--------|--------|
| PLL _{REFCLK} MASK | PLL reference clock select phase noise mask at REFCLK frequency = 25 MHz | 100 | - | - | -102 | dBc/Hz |
| | | 1 KHz | - | - | -124 | |
| | | 10 KHz | - | - | -132 | |
| | | 100 KHz | - | - | -139 | |
| | | 1 MHz | - | - | -152 | |
| | | 10 MHz | - | - | -154 | |
| | PLL reference clock select phase noise mask at REFCLK frequency = 50 MHz | 100 | - | - | -96 | dBc/Hz |
| | | 1 KHz | - | - | -118 | |
| | | 10 KHz | - | - | -126 | |
| | | 100 KHz | - | - | -133 | |
| | | 1 MHz | - | - | -146 | |
| | | 10 MHz | - | - | -148 | |
| | PLL reference clock select phase noise mask at REFCLK frequency = 100 MHz | 100 | - | - | -90 | dBc/Hz |
| | | 1 KHz | - | - | -112 | |
| | | 10 KHz | - | - | -120 | |
| | | 100 KHz | - | - | -127 | |
| | | 1 MHz | - | - | -140 | |
| | | 10 MHz | - | - | -142 | |
| | PLL reference clock select phase noise mask at REFCLK frequency = 125 MHz | 100 | - | - | -88 | dBc/Hz |
| | | 1 KHz | - | - | -110 | |
| | | 10 KHz | - | - | -118 | |
| 100 KHz | | - | - | -125 | | |
| 1 MHz | | - | - | -138 | | |
| 10 MHz | | - | - | -140 | | |
| PLL reference clock select phase noise mask at REFCLK frequency = 150 MHz | 100 | - | - | -86 | dBc/Hz | |
| | 1 KHz | - | - | -108 | | |
| | 10 KHz | - | - | -116 | | |
| | 100 KHz | - | - | -123 | | |
| | 1 MHz | - | - | -136 | | |
| | 10 MHz | - | - | -138 | | |

Notes:

- For reference clock frequencies not in this table, use the phase noise mask for the nearest reference clock frequency.

Table 62: PS-GTR Transceiver Transmitter Switching Characteristics

| Symbol | Description | Condition | Min | Typ | Max | Units |
|--------------------|------------------------|-----------|------|-----|-----|-------|
| F _{GTRTX} | Serial data rate range | | 1.25 | - | 6.0 | Gb/s |
| T _{RTX} | TX rise time | 20%–80% | - | 65 | - | ps |
| T _{FTX} | TX fall time | 80%–20% | - | 65 | - | ps |

Table 63: PS-GTR Transceiver Receiver Switching Characteristics

| Symbol | Description | Condition | Min | Typ | Max | Units |
|----------------------|-----------------------------------|---------------------|-------|-----|-----|-------|
| F _{GTRRX} | Serial data rate | | 1.25 | - | 6 | Gb/s |
| RX _{SST} | Receiver spread-spectrum tracking | Modulated at 33 KHz | -5000 | - | 0 | ppm |
| RX _{PPMTOL} | Data/REFCLK PPM offset tolerance | All data rates | -350 | - | 350 | ppm |

Table 64: PCI Express Protocol Characteristics (PS-GTR Transceivers)

| Standard | Description ¹ | Line Rate (Mb/s) | Min | Max | Units |
|---|--|------------------|------|------|-------|
| PCI Express Transmitter Jitter Generation | | | | | |
| PCI Express Gen 1 | Total transmitter jitter | 2500 | - | 0.25 | UI |
| PCI Express Gen 2 | Total transmitter jitter | 5000 | - | 0.25 | UI |
| PCI Express Receiver High Frequency Jitter Tolerance | | | | | |
| PCI Express Gen 1 | Total receiver jitter tolerance | 2500 | 0.65 | - | UI |
| PCI Express Gen 2 ² | Receiver inherent timing error | 5000 | 0.4 | - | UI |
| | Receiver inherent deterministic timing error | 5000 | 0.3 | - | UI |

Notes:

1. Tested per card electromechanical (CEM) methodology.
2. Between 1 MHz and 10 MHz the minimum sinusoidal jitter roll-off with a slope of 20 dB/decade.

Table 65: Serial ATA (SATA) Protocol Characteristics (PS-GTR Transceivers)

| Standard | Description | Line Rate (Mb/s) | Min | Max | Units |
|--|---------------------------------|------------------|------|------|-------|
| Serial ATA Transmitter Jitter Generation | | | | | |
| SATA Gen 1 | Total transmitter jitter | 1500 | - | 0.37 | UI |
| SATA Gen 2 | Total transmitter jitter | 3000 | - | 0.37 | UI |
| SATA Gen 3 | Total transmitter jitter | 6000 | - | 0.52 | UI |
| Serial ATA Receiver High Frequency Jitter Tolerance | | | | | |
| SATA Gen 1 | Total receiver jitter tolerance | 1500 | 0.27 | - | UI |
| SATA Gen 2 | Total receiver jitter tolerance | 3000 | 0.27 | - | UI |
| SATA Gen 3 | Total receiver jitter tolerance | 6000 | 0.16 | - | UI |

Table 66: DisplayPort Protocol Characteristics (PS-GTR Transceivers)

| Standard | Description ¹ | Line Rate (Mb/s) | Min | Max | Units |
|--|--------------------------|------------------|-----|------|-------|
| DisplayPort Transmitter Jitter Generation | | | | | |
| RBR | Total transmitter jitter | 1620 | - | 0.42 | UI |
| HBR | Total transmitter jitter | 2700 | - | 0.42 | UI |
| HBR2 D10.2 | Total transmitter jitter | 5400 | - | 0.40 | UI |
| HBR2 CPAT | Total transmitter jitter | 5400 | - | 0.58 | UI |

Notes:

1. Only the transmitter is supported.

Table 67: USB 3.0 Protocol Characteristics (PS-GTR Transceivers)

| Standard | Description | Line Rate (Mb/s) | Min | Max | Units |
|---|---------------------------------|------------------|-----|------|-------|
| USB 3.0 Transmitter Jitter Generation | | | | | |
| USB 3.0 | Total transmitter jitter | 5000 | - | 0.66 | UI |
| USB 3.0 Receiver High Frequency Jitter Tolerance | | | | | |
| USB 3.0 | Total receiver jitter tolerance | 5000 | 0.2 | - | UI |

Table 68: Serial-GMII Protocol Characteristics (PS-GTR Transceivers)

| Standard | Description | Line Rate (Mb/s) | Min | Max | Units |
|---|----------------------------------|------------------|------|------|-------|
| Serial-GMII Transmitter Jitter Generation | | | | | |
| SGMII | Deterministic transmitter jitter | 1250 | - | 0.25 | UI |
| Serial-GMII Receiver High Frequency Jitter Tolerance | | | | | |
| SGMII | Total receiver jitter tolerance | 1250 | 0.25 | - | UI |

PS System Monitor Specifications

Table 69: PS SYSMON Specifications

| Parameter | Comments | Conditions | Min | Typ | Max | Units |
|--|--|--------------------------------------|-----|-----|-----------|------------|
| $V_{CC_PSADC} = 1.8V \pm 3\%$, $T_j = -40^\circ C$ to $100^\circ C$, typical values at $T_j = 40^\circ C$ | | | | | | |
| ADC Accuracy ($T_j = -55^\circ C$ to $125^\circ C$)¹ | | | | | | |
| Resolution | | | 10 | - | - | Bits |
| Sample rate | | | - | - | 1 | MS/s |
| RMS code noise | On-chip reference | | - | 1 | - | LSBs |
| On-Chip Sensor Accuracy | | | | | | |
| Temperature sensor error | | $T_j = -55^\circ C$ to $110^\circ C$ | - | - | ± 3.5 | $^\circ C$ |
| | | $T_j = 110^\circ C$ to $125^\circ C$ | - | - | ± 5 | $^\circ C$ |
| Supply sensor error ² | Supply voltages less than or electrically connected to V_{CC_PSADC} | $T_j = -55^\circ C$ to $125^\circ C$ | - | - | ± 1 | % |
| | Supply voltages nominally at 1.8V but with the potential to go above V_{CC_PSADC} | $T_j = -55^\circ C$ to $125^\circ C$ | - | - | ± 1.5 | % |
| | Supply voltages nominally in the 2.0V to 3.3V range | $T_j = -55^\circ C$ to $125^\circ C$ | - | - | ± 2.5 | % |
| Conversion Rate³ | | | | | | |
| Conversion time—continuous | t_{CONV} | Number of ADCCLK cycles | 26 | - | 32 | Cycles |
| Conversion time—event | t_{CONV} | Number of ADCCLK cycles | - | - | 21 | Cycles |
| DRP clock frequency | DCLK | AMS REFCLK frequency | 8 | - | 250 | MHz |
| ADC clock frequency | ADCCLK | Derived from DCLK | 1 | - | 26 | MHz |

Notes:

1. ADC offset errors are removed by enabling the ADC automatic offset calibration feature. The values are specified for when this feature is enabled.
2. Supply sensor offset and gain errors are removed by enabling the automatic offset and gain calibration feature. The values are specified for when this feature is enabled.
3. See the Adjusting the Acquisition Settling Time section in the *UltraScale Architecture System Monitor User Guide* (UG580).

Programmable Logic (PL) Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in the Zynq UltraScale+ MPSoCs. These values are subject to the same guidelines as the [AC Switching Characteristics](#) section.

In each of the following LVDS performance tables, the I/O bank type is either high performance (HP) or high density (HD).

In LVDS component mode:

- For the input/output registers in HP I/O banks, the Vivado tools limit clock frequencies to 312.9 MHz for all speed grades.
- For IDDR in HP I/O banks, Vivado tools limit clock frequencies to 625.0 MHz for all speed grades.

- For ODDR in HP I/O banks, Vivado tools limit clock frequencies to 625.0 MHz for all speed grades.

Table 70: LVDS Component Mode Performance

| Description | I/O Bank Type | Speed Grade and V _{CCINT} Operating Voltages | | | | | | | | | | Units |
|---|---------------|---|------|-------|------|-----|------|-------|------|-----|------|-------|
| | | 0.90V | | 0.85V | | | | 0.72V | | | | |
| | | -3 | | -2 | | -1 | | -2 | | -1 | | |
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| LVDS TX DDR (OSERDES 4:1, 8:1) | HP | 0 | 1250 | 0 | 1250 | 0 | 1250 | 0 | 1250 | 0 | 1250 | Mb/s |
| LVDS TX SDR (OSERDES 2:1, 4:1) | HP | 0 | 625 | 0 | 625 | 0 | 625 | 0 | 625 | 0 | 625 | Mb/s |
| LVDS RX DDR (ISERDES 1:4, 1:8) ¹ | HP | 0 | 1250 | 0 | 1250 | 0 | 1250 | 0 | 1250 | 0 | 1250 | Mb/s |
| LVDS RX DDR | HD | 0 | 250 | 0 | 250 | 0 | 250 | 0 | 250 | 0 | 250 | Mb/s |
| LVDS RX SDR (ISERDES 1:2, 1:4) ¹ | HP | 0 | 625 | 0 | 625 | 0 | 625 | 0 | 625 | 0 | 625 | Mb/s |
| LVDS RX SDR | HD | 0 | 125 | 0 | 125 | 0 | 125 | 0 | 125 | 0 | 125 | Mb/s |

Notes:

- LVDS receivers are typically bounded with certain applications to achieve maximum performance. Package skews are not included and should be removed through PCB routing.

Table 71: LVDS Native Mode Performance

| Description ^{1, 2} | DATA_WIDTH | I/O Bank Type | Speed Grade and V _{CCINT} Operating Voltages | | | | | | | | | | Units |
|--|------------|---------------|---|-------------------|-----------------|-------------------|-------|-------------------|-----------------|-------------------|-------|-------------------|-------|
| | | | 0.90V | | 0.85V | | | | 0.72V | | | | |
| | | | -3 ³ | | -2 ³ | | -1 | | -2 ³ | | -1 | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| LVDS TX DDR (TX_BITSLICE) | 4 | HP | 375 | 1600 | 375 | 1600 | 375 | 1600 | 375 | 1400 | 375 | 1260 | Mb/s |
| | 8 | | 375 | 1600 | 375 | 1600 | 375 | 1600 | 375 | 1600 | 375 | 1600 | Mb/s |
| LVDS TX SDR (TX_BITSLICE) | 4 | HP | 187.5 | 800 | 187.5 | 800 | 187.5 | 800 | 187.5 | 700 | 187.5 | 630 | Mb/s |
| | 8 | | 187.5 | 800 | 187.5 | 800 | 187.5 | 800 | 187.5 | 800 | 187.5 | 800 | Mb/s |
| LVDS RX DDR (RX_BITSLICE) ⁴ | 4 | HP | 375 | 1600 ⁵ | 375 | 1600 ⁵ | 375 | 1600 ⁵ | 375 | 1400 ⁵ | 375 | 1260 ⁵ | Mb/s |
| | 8 | | 375 | 1600 ⁵ | 375 | 1600 ⁵ | 375 | 1600 ⁵ | 375 | 1600 ⁵ | 375 | 1600 ⁵ | Mb/s |
| LVDS RX SDR (RX_BITSLICE) ⁴ | 4 | HP | 187.5 | 800 | 187.5 | 800 | 187.5 | 800 | 187.5 | 700 | 187.5 | 630 | Mb/s |
| | 8 | | 187.5 | 800 | 187.5 | 800 | 187.5 | 800 | 187.5 | 800 | 187.5 | 800 | Mb/s |

Notes:

- Native mode is supported through the [High-Speed SelectIO Interface Wizard](#) available with the Vivado Design Suite. The performance values assume a source-synchronous interface.
- PLL settings can restrict the minimum allowable data rate. For example, when using the PLL with CLKOUTPHY_MODE = VCO_HALF the minimum frequency is PLL_FVCOMIN/2.
- In the SBVA484 and SFRA484 packages, the maximum data rate is 1260 Mb/s for DDR interfaces and 630 Mb/s for SDR interfaces.
- LVDS receivers are typically bounded with certain applications to achieve maximum performance. Package skews are not included and should be removed through PCB routing.
- Asynchronous receiver performance is limited to 1300 Mb/s for -3/-2 speed grades and to 1250 Mb/s for -1 speed grades.

Table 72: MIPI D-PHY Performance

| Description | I/O Bank Type | Speed Grade and V _{CCINT} Operating Voltages | | | | | Units |
|------------------------------------|---------------|---|-------------------|-------------------|-------------------|------|-------|
| | | 0.90V | 0.85V | | 0.72V | | |
| | | -3 ¹ | -2 ¹ | -1 | -2 | -1 | |
| MIPI D-PHY transmitter or receiver | HP | 1500 ² | 1500 ² | 1260 ³ | 1260 ³ | 1260 | Mb/s |

Notes:

1. In the SBVA484 and SFRA484 packages, the data rate is 1260 Mb/s. Notes 2 and 3 do not apply to these packages.
2. The Zynq UltraScale+ MPSoCs performance is specified at 1500 Mb/s when designing with Vivado Design Suite v2019.1 or earlier. For XC and XA devices, the performance is specified at 2500 Mb/s when designing with Vivado Design Suite v2019.1.1 or later. XQ devices are specified at 1500 Mb/s.
3. The Zynq UltraScale+ MPSoCs performance is specified at 1260 Mb/s when designing with Vivado Design Suite v2019.1 or earlier. For XC and XA devices, the performance is specified at 2500 Mb/s when designing with Vivado Design Suite v2019.1.1 or later. XQ devices are specified at 1260 Mb/s.

Table 73: LVDS Native-Mode 1000BASE-X Support

| Description ¹ | I/O Bank Type | Speed Grade and V _{CCINT} Operating Voltages | | | | |
|--------------------------|---------------|---|-------|----|-------|----|
| | | 0.90V | 0.85V | | 0.72V | |
| | | -3 | -2 | -1 | -2 | -1 |
| 1000BASE-X | HP | Yes | | | | |

Notes:

1. 1000BASE-X support is based on the *IEEE Standard for CSMA/CD Access Method and Physical Layer Specifications* (IEEE Std 802.3-2008).

The following table provides the maximum data rates for applicable memory standards using the Zynq UltraScale+ MPSoC memory PHY. Refer to [Memory Interfaces](#) for the complete list of memory interface standards supported and detailed specifications. The final performance of the memory interface is determined through a complete design implemented in the Vivado Design Suite, following guidelines in the *UltraScale Architecture PCB Design User Guide* (UG583), electrical analysis, and characterization of the system.

Table 74: Maximum Physical Interface (PHY) Rate for Memory Interfaces

| Memory Standard | Packages ¹ | DRAM Type | Speed Grade and V _{CCINT} Operating Voltages | | | | | Units |
|-----------------|------------------------------------|------------------------------|---|-------|------|-------|------|-------|
| | | | 0.90V | 0.85V | | 0.72V | | |
| | | | -3 | -2 | -1 | -2 | -1 | |
| DDR4 | All FFV, FFR, and FBVB900 packages | Single rank component | 2666 | 2666 | 2400 | 2400 | 2133 | Mb/s |
| | | 1 rank DIMM ^{2,3,4} | 2400 | 2400 | 2133 | 2133 | 1866 | Mb/s |
| | | 2 rank DIMM ^{2,5} | 2133 | 2133 | 1866 | 1866 | 1600 | Mb/s |
| | | 4 rank DIMM ^{2,6} | 1600 | 1600 | 1333 | 1333 | N/A | Mb/s |
| | SFVC784 and SFRC784 | Single rank component | 2400 | 2400 | 2133 | 2133 | 1866 | Mb/s |
| | | 1 rank DIMM ^{2,3} | 2133 | 2133 | 1866 | 1866 | 1600 | Mb/s |
| | | 2 rank DIMM ^{2,5} | 1866 | 1866 | 1600 | 1600 | 1600 | Mb/s |

Table 74: Maximum Physical Interface (PHY) Rate for Memory Interfaces (cont'd)

| Memory Standard | Packages ¹ | DRAM Type | Speed Grade and V _{CCINT} Operating Voltages | | | | | Units |
|-----------------|------------------------------------|------------------------------------|---|-------|------|-------|------|-------|
| | | | 0.90V | 0.85V | | 0.72V | | |
| | | | -3 | -2 | -1 | -2 | -1 | |
| DDR3 | All FFV, FFR, and FBVB900 packages | Single rank component | 2133 | 2133 | 2133 | 2133 | 1866 | Mb/s |
| | | 1 rank DIMM ^{2,3} | 1866 | 1866 | 1866 | 1866 | 1600 | Mb/s |
| | | 2 rank DIMM ^{2,5} | 1600 | 1600 | 1600 | 1600 | 1333 | Mb/s |
| | | 4 rank DIMM ^{2,6} | 1066 | 1066 | 1066 | 1066 | 800 | Mb/s |
| | SFVC784 and SFRC784 | Single rank component | 1866 | 1866 | 1866 | 1866 | 1600 | Mb/s |
| | | 1 rank DIMM ^{2,3} | 1600 | 1600 | 1600 | 1600 | 1600 | Mb/s |
| | | 2 rank DIMM ^{2,5} | 1600 | 1600 | 1600 | 1600 | 1333 | Mb/s |
| | | 4 rank DIMM ^{2,6} | 1066 | 1066 | 1066 | 1066 | 800 | Mb/s |
| DDR3L | All FFV, FFR, and FBVB900 packages | Single rank component | 1866 | 1866 | 1866 | 1866 | 1600 | Mb/s |
| | | 1 rank DIMM ^{2,3} | 1600 | 1600 | 1600 | 1600 | 1333 | Mb/s |
| | | 2 rank DIMM ^{2,5} | 1333 | 1333 | 1333 | 1333 | 1066 | Mb/s |
| | | 4 rank DIMM ^{2,6} | 800 | 800 | 800 | 800 | 606 | Mb/s |
| | SFVC784 and SFRC784 | Single rank component | 1600 | 1600 | 1600 | 1600 | 1600 | Mb/s |
| | | 1 rank DIMM ^{2,3} | 1600 | 1600 | 1600 | 1600 | 1333 | Mb/s |
| | | 2 rank DIMM ^{2,5} | 1333 | 1333 | 1333 | 1333 | 1066 | Mb/s |
| | | 4 rank DIMM ^{2,6} | 800 | 800 | 800 | 800 | 606 | Mb/s |
| QDR II+ | All | Single rank component ⁷ | 633 | 633 | 600 | 600 | 550 | MHz |
| RLDRAM 3 | All FFV, FFR, and FBVB900 packages | Single rank component | 1200 | 1200 | 1066 | 1066 | 933 | MHz |
| | SFVC784 and SFRC784 | Single rank component | 1066 | 1066 | 933 | 933 | 800 | MHz |
| QDR IV XP | All | Single rank component | 1066 | 1066 | 1066 | 933 | 933 | MHz |
| LPDDR3 | All | Single rank component | 1600 | 1600 | 1600 | 1600 | 1600 | Mb/s |

Notes:

1. The SBVA484, SFRA484, and SFVA625 packages do not support the PL memory interfaces.
2. Dual in-line memory module (DIMM) includes RDIMM, SODIMM, UDIMM, and LRDIMM.
3. Includes: 1 rank 1 slot, DDP 2 rank, LRDIMM 2 or 4 rank 1 slot.
4. For the DDR4 DDP components at -3 and -2 (V_{CCINT} = 0.85V) speed grades, the maximum data rate is 2133 Mb/s for six or more DDP devices. For five or less DDP devices, use the single rank DIMM data rates for the -3 and -2 (V_{CCINT} = 0.85V) speed grades.
5. Includes: 2 rank 1 slot, 1 rank 2 slot, LRDIMM 2 rank 2 slot.
6. Includes: 2 rank 2 slot, 4 rank 1 slot.
7. The QDR II+ performance specifications are for burst-length 4 (BL = 4) implementations.

Programmable Logic (PL) Switching Characteristics

The following IOB high-density (HD) and IOB high-performance (HP) tables summarize the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

- T_{INBUF_DELAY_PAD_I} is the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.
- T_{OUTBUF_DELAY_O_PAD} is the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.

- $T_{\text{OUTBUF_DELAY_TD_PAD}}$ is the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer. In HP I/O banks, the internal DCI termination turn-on time is always faster than $T_{\text{OUTBUF_DELAY_TD_PAD}}$ when the DCITERMDISABLE pin is used. In HD I/O banks, the on-die termination turn-on time is always faster than $T_{\text{OUTBUF_DELAY_TD_PAD}}$ when the INTERMDISABLE pin is used.

IOB High Density (HD) Switching Characteristics

Table 75: IOB High Density (HD) Switching Characteristics

| I/O Standards | $T_{\text{INBUF_DELAY_PAD_I}}$ | | | | | $T_{\text{OUTBUF_DELAY_O_PAD}}$ | | | | | $T_{\text{OUTBUF_DELAY_TD_PAD}}$ | | | | | Units |
|-------------------|-----------------------------------|-------|-------|-------|-------|------------------------------------|-------|-------|-------|-------|-------------------------------------|-------|-------|-------|-------|-------|
| | 0.90V | | 0.85V | | 0.72V | 0.90V | | 0.85V | | 0.72V | 0.90V | | 0.85V | | 0.72V | |
| | -3 | -2 | -1 | -2 | -1 | -3 | -2 | -1 | -2 | -1 | -3 | -2 | -1 | -2 | -1 | |
| DIFF_HSTL_I_18_F | 0.873 | 0.978 | 1.058 | 0.978 | 1.058 | 1.510 | 1.574 | 1.718 | 1.966 | 2.101 | 1.160 | 1.160 | 1.271 | 1.515 | 1.544 | ns |
| DIFF_HSTL_I_18_S | 0.873 | 0.978 | 1.058 | 0.978 | 1.058 | 1.742 | 1.805 | 1.950 | 2.197 | 2.333 | 1.748 | 1.748 | 1.867 | 2.103 | 2.104 | ns |
| DIFF_HSTL_I_F | 0.873 | 0.978 | 1.058 | 0.978 | 1.058 | 1.563 | 1.611 | 1.762 | 2.003 | 2.145 | 1.313 | 1.313 | 1.417 | 1.668 | 1.668 | ns |
| DIFF_HSTL_I_S | 0.873 | 0.978 | 1.058 | 0.978 | 1.058 | 1.696 | 1.798 | 1.913 | 2.190 | 2.296 | 1.630 | 1.630 | 1.780 | 1.985 | 1.986 | ns |
| DIFF_HSUL_12_F | 0.796 | 0.911 | 0.977 | 0.911 | 0.977 | 1.493 | 1.573 | 1.703 | 1.965 | 2.086 | 1.222 | 1.222 | 1.335 | 1.577 | 1.578 | ns |
| DIFF_HSUL_12_S | 0.796 | 0.911 | 0.977 | 0.911 | 0.977 | 1.653 | 1.711 | 1.864 | 2.103 | 2.247 | 1.536 | 1.536 | 1.665 | 1.891 | 1.891 | ns |
| DIFF_SSTL12_F | 0.796 | 0.906 | 0.977 | 0.906 | 0.977 | 1.577 | 1.643 | 1.792 | 2.035 | 2.175 | 1.285 | 1.285 | 1.423 | 1.640 | 1.640 | ns |
| DIFF_SSTL12_S | 0.796 | 0.906 | 0.977 | 0.906 | 0.977 | 1.726 | 1.784 | 1.948 | 2.176 | 2.331 | 1.567 | 1.567 | 1.706 | 1.922 | 1.922 | ns |
| DIFF_SSTL135_F | 0.807 | 0.927 | 0.995 | 0.927 | 0.995 | 1.558 | 1.625 | 1.765 | 2.017 | 2.148 | 1.341 | 1.341 | 1.458 | 1.696 | 1.696 | ns |
| DIFF_SSTL135_II_F | 0.807 | 0.927 | 0.995 | 0.927 | 0.995 | 1.560 | 1.623 | 1.770 | 2.015 | 2.153 | 1.325 | 1.325 | 1.470 | 1.680 | 1.689 | ns |
| DIFF_SSTL135_II_S | 0.807 | 0.927 | 0.995 | 0.927 | 0.995 | 1.694 | 1.768 | 1.916 | 2.160 | 2.299 | 1.722 | 1.722 | 1.911 | 2.077 | 2.078 | ns |
| DIFF_SSTL135_S | 0.807 | 0.927 | 0.995 | 0.927 | 0.995 | 1.796 | 1.869 | 2.025 | 2.261 | 2.408 | 1.814 | 1.814 | 1.976 | 2.169 | 2.169 | ns |
| DIFF_SSTL15_F | 0.840 | 0.928 | 1.020 | 0.928 | 1.020 | 1.559 | 1.628 | 1.771 | 2.020 | 2.154 | 1.374 | 1.374 | 1.483 | 1.729 | 1.729 | ns |
| DIFF_SSTL15_II_F | 0.840 | 0.928 | 1.020 | 0.928 | 1.020 | 1.574 | 1.622 | 1.778 | 2.014 | 2.161 | 1.356 | 1.356 | 1.442 | 1.711 | 1.712 | ns |
| DIFF_SSTL15_II_S | 0.840 | 0.928 | 1.020 | 0.928 | 1.020 | 1.769 | 1.821 | 1.987 | 2.213 | 2.370 | 1.895 | 1.895 | 2.047 | 2.250 | 2.250 | ns |
| DIFF_SSTL15_S | 0.840 | 0.928 | 1.020 | 0.928 | 1.020 | 1.752 | 1.824 | 1.977 | 2.216 | 2.360 | 1.743 | 1.743 | 1.907 | 2.098 | 2.098 | ns |
| DIFF_SSTL18_II_F | 0.873 | 0.961 | 1.038 | 0.961 | 1.038 | 1.672 | 1.729 | 1.880 | 2.121 | 2.263 | 1.377 | 1.377 | 1.492 | 1.732 | 1.732 | ns |
| DIFF_SSTL18_II_S | 0.873 | 0.961 | 1.038 | 0.961 | 1.038 | 1.748 | 1.796 | 1.965 | 2.188 | 2.348 | 1.616 | 1.616 | 1.800 | 1.971 | 1.972 | ns |
| DIFF_SSTL18_I_F | 0.873 | 0.961 | 1.038 | 0.961 | 1.038 | 1.539 | 1.609 | 1.755 | 2.001 | 2.138 | 1.220 | 1.220 | 1.313 | 1.575 | 1.575 | ns |
| DIFF_SSTL18_I_S | 0.873 | 0.961 | 1.038 | 0.961 | 1.038 | 1.728 | 1.786 | 1.942 | 2.178 | 2.325 | 1.677 | 1.677 | 1.836 | 2.032 | 2.033 | ns |
| HSTL_I_18_F | 0.854 | 0.947 | 1.021 | 0.947 | 1.021 | 1.510 | 1.574 | 1.718 | 1.966 | 2.101 | 1.160 | 1.160 | 1.271 | 1.515 | 1.544 | ns |
| HSTL_I_18_S | 0.854 | 0.947 | 1.021 | 0.947 | 1.021 | 1.742 | 1.805 | 1.950 | 2.197 | 2.333 | 1.748 | 1.748 | 1.867 | 2.103 | 2.104 | ns |
| HSTL_I_F | 0.748 | 0.856 | 0.900 | 0.856 | 0.900 | 1.563 | 1.611 | 1.762 | 2.003 | 2.145 | 1.313 | 1.313 | 1.417 | 1.668 | 1.668 | ns |
| HSTL_I_S | 0.748 | 0.856 | 0.900 | 0.856 | 0.900 | 1.696 | 1.798 | 1.913 | 2.190 | 2.296 | 1.630 | 1.630 | 1.780 | 1.985 | 1.986 | ns |
| HSUL_12_F | 0.712 | 0.780 | 0.867 | 0.780 | 0.867 | 1.493 | 1.573 | 1.703 | 1.965 | 2.086 | 1.222 | 1.222 | 1.335 | 1.577 | 1.578 | ns |
| HSUL_12_S | 0.712 | 0.780 | 0.867 | 0.780 | 0.867 | 1.653 | 1.711 | 1.864 | 2.103 | 2.247 | 1.536 | 1.536 | 1.665 | 1.891 | 1.891 | ns |
| LVC MOS12_F_12 | 0.761 | 0.918 | 0.976 | 0.918 | 0.976 | 1.652 | 1.689 | 1.856 | 2.081 | 2.239 | 1.202 | 1.202 | 1.317 | 1.557 | 1.557 | ns |
| LVC MOS12_F_4 | 0.761 | 0.918 | 0.976 | 0.918 | 0.976 | 1.714 | 1.742 | 1.922 | 2.134 | 2.305 | 1.353 | 1.353 | 1.478 | 1.708 | 1.708 | ns |
| LVC MOS12_F_8 | 0.761 | 0.918 | 0.976 | 0.918 | 0.976 | 1.668 | 1.714 | 1.879 | 2.106 | 2.262 | 1.292 | 1.292 | 1.432 | 1.647 | 1.647 | ns |
| LVC MOS12_S_12 | 0.761 | 0.918 | 0.976 | 0.918 | 0.976 | 2.019 | 2.073 | 2.247 | 2.465 | 2.630 | 1.581 | 1.581 | 1.717 | 1.936 | 1.937 | ns |
| LVC MOS12_S_4 | 0.761 | 0.918 | 0.976 | 0.918 | 0.976 | 1.979 | 1.979 | 2.182 | 2.371 | 2.565 | 1.633 | 1.633 | 1.772 | 1.988 | 1.989 | ns |
| LVC MOS12_S_8 | 0.761 | 0.918 | 0.976 | 0.918 | 0.976 | 2.132 | 2.205 | 2.406 | 2.597 | 2.789 | 1.767 | 1.767 | 1.928 | 2.122 | 2.123 | ns |

Table 75: IOB High Density (HD) Switching Characteristics (cont'd)

| I/O Standards | $T_{INBUF_DELAY_PAD_I}$ | | | | | $T_{OUTBUF_DELAY_O_PAD}$ | | | | | $T_{OUTBUF_DELAY_TD_PAD}$ | | | | | Units |
|----------------|----------------------------|-------|-------|-------|-------|-----------------------------|-------|-------|-------|-------|------------------------------|-------|-------|-------|-------|-------|
| | 0.90V | | 0.85V | | 0.72V | 0.90V | | 0.85V | | 0.72V | 0.90V | | 0.85V | | 0.72V | |
| | -3 | -2 | -1 | -2 | -1 | -3 | -2 | -1 | -2 | -1 | -3 | -2 | -1 | -2 | -1 | |
| LVC MOS15_F_12 | 0.775 | 0.905 | 0.958 | 0.905 | 0.958 | 1.691 | 1.713 | 1.892 | 2.105 | 2.275 | 1.275 | 1.275 | 1.428 | 1.630 | 1.630 | ns |
| LVC MOS15_F_16 | 0.775 | 0.905 | 0.958 | 0.905 | 0.958 | 1.665 | 1.722 | 1.881 | 2.114 | 2.264 | 1.260 | 1.260 | 1.407 | 1.615 | 1.615 | ns |
| LVC MOS15_F_4 | 0.775 | 0.905 | 0.958 | 0.905 | 0.958 | 1.747 | 1.825 | 1.959 | 2.217 | 2.342 | 1.453 | 1.453 | 1.557 | 1.808 | 1.809 | ns |
| LVC MOS15_F_8 | 0.775 | 0.905 | 0.958 | 0.905 | 0.958 | 1.721 | 1.778 | 1.930 | 2.170 | 2.313 | 1.378 | 1.378 | 1.458 | 1.733 | 1.733 | ns |
| LVC MOS15_S_12 | 0.775 | 0.905 | 0.958 | 0.905 | 0.958 | 1.936 | 1.991 | 2.139 | 2.383 | 2.522 | 1.516 | 1.516 | 1.648 | 1.871 | 1.871 | ns |
| LVC MOS15_S_16 | 0.775 | 0.905 | 0.958 | 0.905 | 0.958 | 2.172 | 2.172 | 2.389 | 2.564 | 2.772 | 1.707 | 1.707 | 1.888 | 2.062 | 2.062 | ns |
| LVC MOS15_S_4 | 0.775 | 0.905 | 0.958 | 0.905 | 0.958 | 2.274 | 2.313 | 2.483 | 2.705 | 2.866 | 1.952 | 1.952 | 2.123 | 2.307 | 2.307 | ns |
| LVC MOS15_S_8 | 0.775 | 0.905 | 0.958 | 0.905 | 0.958 | 2.170 | 2.170 | 2.400 | 2.562 | 2.783 | 1.817 | 1.817 | 1.984 | 2.172 | 2.173 | ns |
| LVC MOS18_F_12 | 0.810 | 0.915 | 0.958 | 0.915 | 0.958 | 1.741 | 1.805 | 1.962 | 2.197 | 2.345 | 1.383 | 1.383 | 1.471 | 1.738 | 1.738 | ns |
| LVC MOS18_F_16 | 0.810 | 0.915 | 0.958 | 0.915 | 0.958 | 1.698 | 1.785 | 1.917 | 2.177 | 2.300 | 1.338 | 1.338 | 1.446 | 1.693 | 1.693 | ns |
| LVC MOS18_F_4 | 0.810 | 0.915 | 0.958 | 0.915 | 0.958 | 1.815 | 1.868 | 2.013 | 2.260 | 2.396 | 1.472 | 1.472 | 1.599 | 1.827 | 1.832 | ns |
| LVC MOS18_F_8 | 0.810 | 0.915 | 0.958 | 0.915 | 0.958 | 1.785 | 1.797 | 1.979 | 2.189 | 2.362 | 1.384 | 1.384 | 1.487 | 1.739 | 1.739 | ns |
| LVC MOS18_S_12 | 0.810 | 0.915 | 0.958 | 0.915 | 0.958 | 2.163 | 2.201 | 2.408 | 2.593 | 2.791 | 1.762 | 1.762 | 1.894 | 2.117 | 2.118 | ns |
| LVC MOS18_S_16 | 0.810 | 0.915 | 0.958 | 0.915 | 0.958 | 2.102 | 2.173 | 2.362 | 2.565 | 2.745 | 1.702 | 1.702 | 1.834 | 2.057 | 2.057 | ns |
| LVC MOS18_S_4 | 0.810 | 0.915 | 0.958 | 0.915 | 0.958 | 2.342 | 2.346 | 2.567 | 2.738 | 2.950 | 1.951 | 1.951 | 2.092 | 2.306 | 2.306 | ns |
| LVC MOS18_S_8 | 0.810 | 0.915 | 0.958 | 0.915 | 0.958 | 2.275 | 2.292 | 2.511 | 2.684 | 2.894 | 1.848 | 1.848 | 2.008 | 2.203 | 2.204 | ns |
| LVC MOS25_F_12 | 0.963 | 0.988 | 1.042 | 0.988 | 1.042 | 2.153 | 2.153 | 2.453 | 2.545 | 2.836 | 1.692 | 1.692 | 1.856 | 2.047 | 2.047 | ns |
| LVC MOS25_F_16 | 0.963 | 0.988 | 1.042 | 0.988 | 1.042 | 2.105 | 2.105 | 2.406 | 2.497 | 2.789 | 1.623 | 1.623 | 1.786 | 1.978 | 1.979 | ns |
| LVC MOS25_F_4 | 0.963 | 0.988 | 1.042 | 0.988 | 1.042 | 2.317 | 2.344 | 2.554 | 2.736 | 2.937 | 1.842 | 1.842 | 2.039 | 2.197 | 2.197 | ns |
| LVC MOS25_F_8 | 0.963 | 0.988 | 1.042 | 0.988 | 1.042 | 2.184 | 2.184 | 2.516 | 2.576 | 2.899 | 1.726 | 1.726 | 1.910 | 2.081 | 2.081 | ns |
| LVC MOS25_S_12 | 0.963 | 0.988 | 1.042 | 0.988 | 1.042 | 2.550 | 2.558 | 2.840 | 2.950 | 3.223 | 1.971 | 1.971 | 2.194 | 2.326 | 2.327 | ns |
| LVC MOS25_S_16 | 0.963 | 0.988 | 1.042 | 0.988 | 1.042 | 2.449 | 2.449 | 2.740 | 2.841 | 3.123 | 1.852 | 1.852 | 2.063 | 2.207 | 2.207 | ns |
| LVC MOS25_S_4 | 0.963 | 0.988 | 1.042 | 0.988 | 1.042 | 2.770 | 2.770 | 3.066 | 3.162 | 3.449 | 2.224 | 2.224 | 2.458 | 2.579 | 2.579 | ns |
| LVC MOS25_S_8 | 0.963 | 0.988 | 1.042 | 0.988 | 1.042 | 2.663 | 2.663 | 2.963 | 3.055 | 3.346 | 2.091 | 2.091 | 2.373 | 2.446 | 2.446 | ns |
| LVC MOS33_F_12 | 1.154 | 1.154 | 1.213 | 1.154 | 1.213 | 2.415 | 2.415 | 2.651 | 2.807 | 3.034 | 1.754 | 1.754 | 1.915 | 2.109 | 2.109 | ns |
| LVC MOS33_F_16 | 1.154 | 1.154 | 1.213 | 1.154 | 1.213 | 2.381 | 2.383 | 2.603 | 2.775 | 2.986 | 1.734 | 1.734 | 1.869 | 2.089 | 2.089 | ns |
| LVC MOS33_F_4 | 1.154 | 1.154 | 1.213 | 1.154 | 1.213 | 2.541 | 2.541 | 2.765 | 2.933 | 3.148 | 1.932 | 1.932 | 2.135 | 2.287 | 2.287 | ns |
| LVC MOS33_F_8 | 1.154 | 1.154 | 1.213 | 1.154 | 1.213 | 2.603 | 2.603 | 2.822 | 2.995 | 3.205 | 1.937 | 1.937 | 2.130 | 2.292 | 2.294 | ns |
| LVC MOS33_S_12 | 1.154 | 1.154 | 1.213 | 1.154 | 1.213 | 2.705 | 2.705 | 3.047 | 3.097 | 3.430 | 2.049 | 2.049 | 2.318 | 2.404 | 2.404 | ns |
| LVC MOS33_S_16 | 1.154 | 1.154 | 1.213 | 1.154 | 1.213 | 2.714 | 2.714 | 3.024 | 3.106 | 3.407 | 2.028 | 2.028 | 2.232 | 2.383 | 2.383 | ns |
| LVC MOS33_S_4 | 1.154 | 1.154 | 1.213 | 1.154 | 1.213 | 2.999 | 2.999 | 3.340 | 3.391 | 3.723 | 2.320 | 2.320 | 2.610 | 2.675 | 2.675 | ns |
| LVC MOS33_S_8 | 1.154 | 1.154 | 1.213 | 1.154 | 1.213 | 2.929 | 2.929 | 3.260 | 3.321 | 3.643 | 2.260 | 2.260 | 2.532 | 2.615 | 2.616 | ns |
| LVDS_25 | 0.980 | 1.003 | 1.116 | 1.003 | 1.116 | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A | ns |
| LVPECL | 0.980 | 1.003 | 1.116 | 1.003 | 1.116 | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A | ns |
| LVTTTL_F_12 | 1.164 | 1.164 | 1.223 | 1.164 | 1.223 | 2.415 | 2.415 | 2.651 | 2.807 | 3.034 | 1.754 | 1.754 | 1.915 | 2.109 | 2.109 | ns |
| LVTTTL_F_16 | 1.164 | 1.164 | 1.223 | 1.164 | 1.223 | 2.464 | 2.464 | 2.732 | 2.856 | 3.115 | 1.750 | 1.750 | 1.986 | 2.105 | 2.117 | ns |
| LVTTTL_F_4 | 1.164 | 1.164 | 1.223 | 1.164 | 1.223 | 2.541 | 2.541 | 2.765 | 2.933 | 3.148 | 1.932 | 1.932 | 2.135 | 2.287 | 2.287 | ns |
| LVTTTL_F_8 | 1.164 | 1.164 | 1.223 | 1.164 | 1.223 | 2.582 | 2.582 | 2.787 | 2.974 | 3.170 | 1.910 | 1.910 | 2.063 | 2.265 | 2.265 | ns |
| LVTTTL_S_12 | 1.164 | 1.164 | 1.223 | 1.164 | 1.223 | 2.731 | 2.731 | 3.075 | 3.123 | 3.458 | 2.072 | 2.072 | 2.343 | 2.427 | 2.427 | ns |

Table 75: IOB High Density (HD) Switching Characteristics (cont'd)

| I/O Standards | $T_{INBUF_DELAY_PAD_I}$ | | | | | $T_{OUTBUF_DELAY_O_PAD}$ | | | | | $T_{OUTBUF_DELAY_TD_PAD}$ | | | | | Units |
|---------------|----------------------------|-------|-------|-------|-------|-----------------------------|-------|-------|-------|-------|------------------------------|-------|-------|-------|-------|-------|
| | 0.90V | | 0.85V | | 0.72V | 0.90V | | 0.85V | | 0.72V | 0.90V | | 0.85V | | 0.72V | |
| | -3 | -2 | -1 | -2 | -1 | -3 | -2 | -1 | -2 | -1 | -3 | -2 | -1 | -2 | -1 | |
| LVTTL_S_16 | 1.164 | 1.164 | 1.223 | 1.164 | 1.223 | 2.714 | 2.714 | 3.024 | 3.106 | 3.407 | 2.028 | 2.028 | 2.232 | 2.383 | 2.383 | ns |
| LVTTL_S_4 | 1.164 | 1.164 | 1.223 | 1.164 | 1.223 | 2.999 | 2.999 | 3.340 | 3.391 | 3.723 | 2.320 | 2.320 | 2.610 | 2.675 | 2.675 | ns |
| LVTTL_S_8 | 1.164 | 1.164 | 1.223 | 1.164 | 1.223 | 2.929 | 2.929 | 3.260 | 3.321 | 3.643 | 2.260 | 2.260 | 2.532 | 2.615 | 2.616 | ns |
| SLVS_400_25 | 0.998 | 1.020 | 1.136 | 1.020 | 1.136 | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A | ns |
| SSTL12_F | 0.712 | 0.780 | 0.867 | 0.780 | 0.867 | 1.577 | 1.643 | 1.792 | 2.035 | 2.175 | 1.285 | 1.285 | 1.423 | 1.640 | 1.640 | ns |
| SSTL12_S | 0.712 | 0.780 | 0.867 | 0.780 | 0.867 | 1.726 | 1.784 | 1.948 | 2.176 | 2.331 | 1.567 | 1.567 | 1.706 | 1.922 | 1.922 | ns |
| SSTL135_F | 0.731 | 0.798 | 0.881 | 0.798 | 0.881 | 1.558 | 1.625 | 1.765 | 2.017 | 2.148 | 1.341 | 1.341 | 1.458 | 1.696 | 1.696 | ns |
| SSTL135_II_F | 0.731 | 0.798 | 0.881 | 0.798 | 0.881 | 1.574 | 1.623 | 1.770 | 2.015 | 2.153 | 1.325 | 1.325 | 1.470 | 1.680 | 1.689 | ns |
| SSTL135_II_S | 0.731 | 0.798 | 0.881 | 0.798 | 0.881 | 1.694 | 1.768 | 1.916 | 2.160 | 2.299 | 1.722 | 1.722 | 1.911 | 2.077 | 2.078 | ns |
| SSTL135_S | 0.731 | 0.798 | 0.881 | 0.798 | 0.881 | 1.796 | 1.869 | 2.025 | 2.261 | 2.408 | 1.814 | 1.814 | 1.976 | 2.169 | 2.169 | ns |
| SSTL15_F | 0.731 | 0.838 | 0.880 | 0.838 | 0.880 | 1.544 | 1.612 | 1.754 | 2.004 | 2.137 | 1.357 | 1.357 | 1.464 | 1.712 | 1.713 | ns |
| SSTL15_II_F | 0.731 | 0.838 | 0.880 | 0.838 | 0.880 | 1.588 | 1.622 | 1.778 | 2.014 | 2.161 | 1.356 | 1.356 | 1.442 | 1.711 | 1.712 | ns |
| SSTL15_II_S | 0.731 | 0.838 | 0.880 | 0.838 | 0.880 | 1.769 | 1.821 | 1.987 | 2.213 | 2.370 | 1.895 | 1.895 | 2.047 | 2.250 | 2.250 | ns |
| SSTL15_S | 0.731 | 0.838 | 0.880 | 0.838 | 0.880 | 1.752 | 1.824 | 1.977 | 2.216 | 2.360 | 1.743 | 1.743 | 1.907 | 2.098 | 2.098 | ns |
| SSTL18_II_F | 0.854 | 0.947 | 1.021 | 0.947 | 1.021 | 1.699 | 1.729 | 1.880 | 2.121 | 2.263 | 1.377 | 1.377 | 1.492 | 1.732 | 1.732 | ns |
| SSTL18_II_S | 0.854 | 0.947 | 1.021 | 0.947 | 1.021 | 1.748 | 1.796 | 1.965 | 2.188 | 2.348 | 1.616 | 1.616 | 1.800 | 1.971 | 1.972 | ns |
| SSTL18_I_F | 0.854 | 0.947 | 1.021 | 0.947 | 1.021 | 1.566 | 1.609 | 1.755 | 2.001 | 2.138 | 1.220 | 1.220 | 1.313 | 1.575 | 1.575 | ns |
| SSTL18_I_S | 0.854 | 0.947 | 1.021 | 0.947 | 1.021 | 1.745 | 1.786 | 1.942 | 2.178 | 2.325 | 1.677 | 1.677 | 1.836 | 2.032 | 2.033 | ns |
| SUB_LVDS | 0.871 | 1.002 | 1.036 | 1.002 | 1.036 | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A | ns |

IOB High Performance (HP) Switching Characteristics

Table 76: IOB High Performance (HP) Switching Characteristics

| I/O Standards | $T_{INBUF_DELAY_PAD_I}$ | | | | | $T_{OUTBUF_DELAY_O_PAD}$ | | | | | $T_{OUTBUF_DELAY_TD_PAD}$ | | | | | Units |
|----------------------|----------------------------|-------|-------|-------|-------|-----------------------------|-------|-------|-------|-------|------------------------------|-------|-------|-------|-------|-------|
| | 0.90V | | 0.85V | | 0.72V | 0.90V | | 0.85V | | 0.72V | 0.90V | | 0.85V | | 0.72V | |
| | -3 | -2 | -1 | -2 | -1 | -3 | -2 | -1 | -2 | -1 | -3 | -2 | -1 | -2 | -1 | |
| DIFF_HSTL_I_12_F | 0.288 | 0.394 | 0.402 | 0.394 | 0.402 | 0.410 | 0.423 | 0.443 | 0.423 | 0.443 | 0.514 | 0.553 | 0.582 | 0.553 | 0.582 | ns |
| DIFF_HSTL_I_12_M | 0.288 | 0.394 | 0.402 | 0.394 | 0.402 | 0.552 | 0.552 | 0.583 | 0.552 | 0.583 | 0.632 | 0.641 | 0.679 | 0.641 | 0.679 | ns |
| DIFF_HSTL_I_12_S | 0.288 | 0.394 | 0.402 | 0.394 | 0.402 | 0.752 | 0.752 | 0.800 | 0.752 | 0.800 | 0.813 | 0.813 | 0.868 | 0.813 | 0.868 | ns |
| DIFF_HSTL_I_18_F | 0.259 | 0.319 | 0.339 | 0.319 | 0.339 | 0.439 | 0.456 | 0.474 | 0.456 | 0.474 | 0.549 | 0.576 | 0.606 | 0.576 | 0.606 | ns |
| DIFF_HSTL_I_18_M | 0.259 | 0.319 | 0.339 | 0.319 | 0.339 | 0.563 | 0.570 | 0.603 | 0.570 | 0.603 | 0.636 | 0.653 | 0.692 | 0.653 | 0.692 | ns |
| DIFF_HSTL_I_18_S | 0.259 | 0.319 | 0.339 | 0.319 | 0.339 | 0.782 | 0.782 | 0.834 | 0.782 | 0.834 | 0.816 | 0.816 | 0.871 | 0.816 | 0.871 | ns |
| DIFF_HSTL_I_DCI_12_F | 0.288 | 0.394 | 0.402 | 0.394 | 0.402 | 0.393 | 0.406 | 0.429 | 0.406 | 0.429 | 0.502 | 0.534 | 0.564 | 0.534 | 0.564 | ns |
| DIFF_HSTL_I_DCI_12_M | 0.288 | 0.394 | 0.402 | 0.394 | 0.402 | 0.546 | 0.557 | 0.587 | 0.557 | 0.587 | 0.636 | 0.653 | 0.694 | 0.653 | 0.694 | ns |
| DIFF_HSTL_I_DCI_12_S | 0.288 | 0.394 | 0.402 | 0.394 | 0.402 | 0.755 | 0.755 | 0.806 | 0.755 | 0.806 | 0.842 | 0.842 | 0.907 | 0.842 | 0.907 | ns |
| DIFF_HSTL_I_DCI_18_F | 0.259 | 0.323 | 0.339 | 0.323 | 0.339 | 0.422 | 0.445 | 0.461 | 0.445 | 0.461 | 0.509 | 0.566 | 0.595 | 0.566 | 0.595 | ns |
| DIFF_HSTL_I_DCI_18_M | 0.259 | 0.323 | 0.339 | 0.323 | 0.339 | 0.546 | 0.555 | 0.586 | 0.555 | 0.586 | 0.626 | 0.643 | 0.684 | 0.643 | 0.684 | ns |
| DIFF_HSTL_I_DCI_18_S | 0.259 | 0.323 | 0.339 | 0.323 | 0.339 | 0.762 | 0.762 | 0.818 | 0.762 | 0.818 | 0.836 | 0.836 | 0.900 | 0.836 | 0.900 | ns |

Table 76: IOB High Performance (HP) Switching Characteristics (cont'd)

| I/O Standards | $T_{INBUF_DELAY_PAD_I}$ | | | | | $T_{OUTBUF_DELAY_O_PAD}$ | | | | | $T_{OUTBUF_DELAY_TD_PAD}$ | | | | | Units |
|--------------------|----------------------------|-------|-------|-------|-------|-----------------------------|-------|-------|-------|-------|------------------------------|-------|-------|-------|-------|-------|
| | 0.90V | | 0.85V | | 0.72V | 0.90V | | 0.85V | | 0.72V | 0.90V | | 0.85V | | 0.72V | |
| | -3 | -2 | -1 | -2 | -1 | -3 | -2 | -1 | -2 | -1 | -3 | -2 | -1 | -2 | -1 | |
| DIFF_HSTL_I_DCI_F | 0.335 | 0.397 | 0.417 | 0.397 | 0.417 | 0.407 | 0.431 | 0.445 | 0.431 | 0.445 | 0.517 | 0.555 | 0.575 | 0.555 | 0.575 | ns |
| DIFF_HSTL_I_DCI_M | 0.335 | 0.397 | 0.417 | 0.397 | 0.417 | 0.549 | 0.553 | 0.583 | 0.553 | 0.583 | 0.634 | 0.644 | 0.684 | 0.644 | 0.684 | ns |
| DIFF_HSTL_I_DCI_S | 0.335 | 0.397 | 0.417 | 0.397 | 0.417 | 0.767 | 0.767 | 0.823 | 0.767 | 0.823 | 0.848 | 0.848 | 0.912 | 0.848 | 0.912 | ns |
| DIFF_HSTL_I_F | 0.304 | 0.404 | 0.417 | 0.404 | 0.417 | 0.409 | 0.423 | 0.443 | 0.423 | 0.443 | 0.514 | 0.549 | 0.581 | 0.549 | 0.581 | ns |
| DIFF_HSTL_I_M | 0.304 | 0.404 | 0.417 | 0.404 | 0.417 | 0.549 | 0.555 | 0.586 | 0.555 | 0.586 | 0.624 | 0.640 | 0.677 | 0.640 | 0.677 | ns |
| DIFF_HSTL_I_S | 0.304 | 0.404 | 0.417 | 0.404 | 0.417 | 0.767 | 0.767 | 0.818 | 0.767 | 0.818 | 0.811 | 0.811 | 0.866 | 0.811 | 0.866 | ns |
| DIFF_HSUL_12_DCI_F | 0.320 | 0.381 | 0.400 | 0.381 | 0.400 | 0.411 | 0.425 | 0.443 | 0.425 | 0.443 | 0.520 | 0.558 | 0.586 | 0.558 | 0.586 | ns |
| DIFF_HSUL_12_DCI_M | 0.320 | 0.381 | 0.400 | 0.381 | 0.400 | 0.546 | 0.557 | 0.587 | 0.557 | 0.587 | 0.636 | 0.653 | 0.694 | 0.653 | 0.694 | ns |
| DIFF_HSUL_12_DCI_S | 0.320 | 0.381 | 0.400 | 0.381 | 0.400 | 0.737 | 0.737 | 0.787 | 0.737 | 0.787 | 0.822 | 0.822 | 0.885 | 0.822 | 0.885 | ns |
| DIFF_HSUL_12_F | 0.322 | 0.394 | 0.402 | 0.394 | 0.402 | 0.394 | 0.412 | 0.430 | 0.412 | 0.430 | 0.494 | 0.538 | 0.566 | 0.538 | 0.566 | ns |
| DIFF_HSUL_12_M | 0.322 | 0.394 | 0.402 | 0.394 | 0.402 | 0.552 | 0.552 | 0.583 | 0.552 | 0.583 | 0.632 | 0.641 | 0.679 | 0.641 | 0.679 | ns |
| DIFF_HSUL_12_S | 0.322 | 0.394 | 0.402 | 0.394 | 0.402 | 0.752 | 0.752 | 0.800 | 0.752 | 0.800 | 0.813 | 0.813 | 0.868 | 0.813 | 0.868 | ns |
| DIFF_POD10_DCI_F | 0.289 | 0.411 | 0.430 | 0.411 | 0.430 | 0.407 | 0.425 | 0.444 | 0.425 | 0.444 | 0.512 | 0.555 | 0.584 | 0.555 | 0.584 | ns |
| DIFF_POD10_DCI_M | 0.289 | 0.411 | 0.430 | 0.411 | 0.430 | 0.533 | 0.542 | 0.571 | 0.542 | 0.571 | 0.618 | 0.640 | 0.681 | 0.640 | 0.681 | ns |
| DIFF_POD10_DCI_S | 0.289 | 0.411 | 0.430 | 0.411 | 0.430 | 0.754 | 0.754 | 0.815 | 0.754 | 0.815 | 0.850 | 0.850 | 0.917 | 0.850 | 0.917 | ns |
| DIFF_POD10_F | 0.288 | 0.411 | 0.433 | 0.411 | 0.433 | 0.425 | 0.438 | 0.459 | 0.438 | 0.459 | 0.531 | 0.569 | 0.601 | 0.569 | 0.601 | ns |
| DIFF_POD10_M | 0.288 | 0.411 | 0.433 | 0.411 | 0.433 | 0.519 | 0.538 | 0.568 | 0.538 | 0.568 | 0.589 | 0.630 | 0.667 | 0.630 | 0.667 | ns |
| DIFF_POD10_S | 0.288 | 0.411 | 0.433 | 0.411 | 0.433 | 0.752 | 0.766 | 0.821 | 0.766 | 0.821 | 0.821 | 0.836 | 0.894 | 0.836 | 0.894 | ns |
| DIFF_POD12_DCI_F | 0.320 | 0.407 | 0.432 | 0.407 | 0.432 | 0.411 | 0.425 | 0.443 | 0.425 | 0.443 | 0.519 | 0.558 | 0.586 | 0.558 | 0.586 | ns |
| DIFF_POD12_DCI_M | 0.320 | 0.407 | 0.432 | 0.407 | 0.432 | 0.516 | 0.543 | 0.572 | 0.543 | 0.572 | 0.602 | 0.638 | 0.678 | 0.638 | 0.678 | ns |
| DIFF_POD12_DCI_S | 0.320 | 0.407 | 0.432 | 0.407 | 0.432 | 0.740 | 0.772 | 0.822 | 0.772 | 0.822 | 0.833 | 0.862 | 0.929 | 0.862 | 0.929 | ns |
| DIFF_POD12_F | 0.305 | 0.409 | 0.430 | 0.409 | 0.430 | 0.438 | 0.455 | 0.476 | 0.455 | 0.476 | 0.549 | 0.595 | 0.626 | 0.595 | 0.626 | ns |
| DIFF_POD12_M | 0.305 | 0.409 | 0.430 | 0.409 | 0.430 | 0.551 | 0.551 | 0.582 | 0.551 | 0.582 | 0.632 | 0.641 | 0.679 | 0.641 | 0.679 | ns |
| DIFF_POD12_S | 0.305 | 0.409 | 0.430 | 0.409 | 0.430 | 0.749 | 0.767 | 0.817 | 0.767 | 0.817 | 0.818 | 0.832 | 0.889 | 0.832 | 0.889 | ns |
| DIFF_SSTL12_DCI_F | 0.303 | 0.381 | 0.400 | 0.381 | 0.400 | 0.411 | 0.425 | 0.443 | 0.425 | 0.443 | 0.520 | 0.558 | 0.586 | 0.558 | 0.586 | ns |
| DIFF_SSTL12_DCI_M | 0.303 | 0.381 | 0.400 | 0.381 | 0.400 | 0.549 | 0.557 | 0.587 | 0.557 | 0.587 | 0.643 | 0.654 | 0.694 | 0.654 | 0.694 | ns |
| DIFF_SSTL12_DCI_S | 0.303 | 0.381 | 0.400 | 0.381 | 0.400 | 0.754 | 0.754 | 0.803 | 0.754 | 0.803 | 0.842 | 0.842 | 0.908 | 0.842 | 0.908 | ns |
| DIFF_SSTL12_F | 0.288 | 0.394 | 0.402 | 0.394 | 0.402 | 0.394 | 0.412 | 0.430 | 0.412 | 0.430 | 0.494 | 0.538 | 0.566 | 0.538 | 0.566 | ns |
| DIFF_SSTL12_M | 0.288 | 0.394 | 0.402 | 0.394 | 0.402 | 0.550 | 0.553 | 0.584 | 0.553 | 0.584 | 0.630 | 0.641 | 0.676 | 0.641 | 0.676 | ns |
| DIFF_SSTL12_S | 0.288 | 0.394 | 0.402 | 0.394 | 0.402 | 0.758 | 0.758 | 0.808 | 0.758 | 0.808 | 0.823 | 0.823 | 0.879 | 0.823 | 0.879 | ns |
| DIFF_SSTL135_DCI_F | 0.303 | 0.371 | 0.402 | 0.371 | 0.402 | 0.392 | 0.411 | 0.428 | 0.411 | 0.428 | 0.494 | 0.537 | 0.565 | 0.537 | 0.565 | ns |
| DIFF_SSTL135_DCI_M | 0.303 | 0.371 | 0.402 | 0.371 | 0.402 | 0.551 | 0.551 | 0.582 | 0.551 | 0.582 | 0.643 | 0.645 | 0.685 | 0.645 | 0.685 | ns |
| DIFF_SSTL135_DCI_S | 0.303 | 0.371 | 0.402 | 0.371 | 0.402 | 0.746 | 0.746 | 0.799 | 0.746 | 0.799 | 0.829 | 0.829 | 0.893 | 0.829 | 0.893 | ns |
| DIFF_SSTL135_F | 0.289 | 0.375 | 0.402 | 0.375 | 0.402 | 0.393 | 0.408 | 0.428 | 0.408 | 0.428 | 0.491 | 0.528 | 0.561 | 0.528 | 0.561 | ns |
| DIFF_SSTL135_M | 0.289 | 0.375 | 0.402 | 0.375 | 0.402 | 0.548 | 0.555 | 0.585 | 0.555 | 0.585 | 0.621 | 0.641 | 0.679 | 0.641 | 0.679 | ns |
| DIFF_SSTL135_S | 0.289 | 0.375 | 0.402 | 0.375 | 0.402 | 0.772 | 0.772 | 0.823 | 0.772 | 0.823 | 0.827 | 0.827 | 0.878 | 0.827 | 0.878 | ns |
| DIFF_SSTL15_DCI_F | 0.335 | 0.397 | 0.417 | 0.397 | 0.417 | 0.394 | 0.412 | 0.429 | 0.412 | 0.429 | 0.497 | 0.531 | 0.563 | 0.531 | 0.563 | ns |
| DIFF_SSTL15_DCI_M | 0.335 | 0.397 | 0.417 | 0.397 | 0.417 | 0.549 | 0.553 | 0.583 | 0.553 | 0.583 | 0.632 | 0.645 | 0.685 | 0.645 | 0.685 | ns |
| DIFF_SSTL15_DCI_S | 0.335 | 0.397 | 0.417 | 0.397 | 0.417 | 0.768 | 0.768 | 0.822 | 0.768 | 0.822 | 0.847 | 0.847 | 0.912 | 0.847 | 0.912 | ns |

Table 76: IOB High Performance (HP) Switching Characteristics (cont'd)

| I/O Standards | $T_{INBUF_DELAY_PAD_I}$ | | | | | $T_{OUTBUF_DELAY_O_PAD}$ | | | | | $T_{OUTBUF_DELAY_TD_PAD}$ | | | | | Units |
|---------------------|----------------------------|-------|-------|-------|-------|-----------------------------|-------|-------|-------|-------|------------------------------|-------|-------|-------|-------|-------|
| | 0.90V | | 0.85V | | 0.72V | 0.90V | | 0.85V | | 0.72V | 0.90V | | 0.85V | | 0.72V | |
| | -3 | -2 | -1 | -2 | -1 | -3 | -2 | -1 | -2 | -1 | -3 | -2 | -1 | -2 | -1 | |
| DIFF_SSTL15_F | 0.304 | 0.404 | 0.417 | 0.404 | 0.417 | 0.409 | 0.424 | 0.445 | 0.424 | 0.445 | 0.513 | 0.551 | 0.577 | 0.551 | 0.577 | ns |
| DIFF_SSTL15_M | 0.304 | 0.404 | 0.417 | 0.404 | 0.417 | 0.547 | 0.554 | 0.585 | 0.554 | 0.585 | 0.624 | 0.639 | 0.677 | 0.639 | 0.677 | ns |
| DIFF_SSTL15_S | 0.304 | 0.404 | 0.417 | 0.404 | 0.417 | 0.767 | 0.767 | 0.817 | 0.767 | 0.817 | 0.813 | 0.813 | 0.867 | 0.813 | 0.867 | ns |
| DIFF_SSTL18_I_DCI_F | 0.256 | 0.320 | 0.336 | 0.320 | 0.336 | 0.422 | 0.445 | 0.461 | 0.445 | 0.461 | 0.540 | 0.566 | 0.595 | 0.566 | 0.595 | ns |
| DIFF_SSTL18_I_DCI_M | 0.256 | 0.320 | 0.336 | 0.320 | 0.336 | 0.552 | 0.554 | 0.585 | 0.554 | 0.585 | 0.629 | 0.644 | 0.683 | 0.644 | 0.683 | ns |
| DIFF_SSTL18_I_DCI_S | 0.256 | 0.320 | 0.336 | 0.320 | 0.336 | 0.762 | 0.762 | 0.818 | 0.762 | 0.818 | 0.837 | 0.837 | 0.899 | 0.837 | 0.899 | ns |
| DIFF_SSTL18_I_F | 0.256 | 0.316 | 0.336 | 0.316 | 0.336 | 0.439 | 0.454 | 0.476 | 0.454 | 0.476 | 0.549 | 0.578 | 0.608 | 0.578 | 0.608 | ns |
| DIFF_SSTL18_I_M | 0.256 | 0.316 | 0.336 | 0.316 | 0.336 | 0.567 | 0.571 | 0.603 | 0.571 | 0.603 | 0.535 | 0.652 | 0.692 | 0.652 | 0.692 | ns |
| DIFF_SSTL18_I_S | 0.256 | 0.316 | 0.336 | 0.316 | 0.336 | 0.782 | 0.782 | 0.835 | 0.782 | 0.835 | 0.816 | 0.816 | 0.870 | 0.816 | 0.870 | ns |
| HSLVDCI_15_F | 0.336 | 0.393 | 0.415 | 0.393 | 0.415 | 0.407 | 0.425 | 0.443 | 0.425 | 0.443 | 0.513 | 0.548 | 0.579 | 0.548 | 0.579 | ns |
| HSLVDCI_15_M | 0.336 | 0.393 | 0.415 | 0.393 | 0.415 | 0.548 | 0.552 | 0.581 | 0.552 | 0.581 | 0.635 | 0.644 | 0.684 | 0.644 | 0.684 | ns |
| HSLVDCI_15_S | 0.336 | 0.393 | 0.415 | 0.393 | 0.415 | 0.748 | 0.748 | 0.802 | 0.748 | 0.802 | 0.827 | 0.827 | 0.890 | 0.827 | 0.890 | ns |
| HSLVDCI_18_F | 0.367 | 0.424 | 0.447 | 0.424 | 0.447 | 0.424 | 0.445 | 0.461 | 0.445 | 0.461 | 0.541 | 0.566 | 0.595 | 0.566 | 0.595 | ns |
| HSLVDCI_18_M | 0.367 | 0.424 | 0.447 | 0.424 | 0.447 | 0.563 | 0.567 | 0.598 | 0.567 | 0.598 | 0.647 | 0.658 | 0.699 | 0.658 | 0.699 | ns |
| HSLVDCI_18_S | 0.367 | 0.424 | 0.447 | 0.424 | 0.447 | 0.761 | 0.761 | 0.817 | 0.761 | 0.817 | 0.836 | 0.836 | 0.900 | 0.836 | 0.900 | ns |
| HSTL_I_12_F | 0.322 | 0.378 | 0.399 | 0.378 | 0.399 | 0.410 | 0.423 | 0.443 | 0.423 | 0.443 | 0.514 | 0.553 | 0.582 | 0.553 | 0.582 | ns |
| HSTL_I_12_M | 0.322 | 0.378 | 0.399 | 0.378 | 0.399 | 0.551 | 0.551 | 0.582 | 0.551 | 0.582 | 0.632 | 0.642 | 0.679 | 0.642 | 0.679 | ns |
| HSTL_I_12_S | 0.322 | 0.378 | 0.399 | 0.378 | 0.399 | 0.750 | 0.750 | 0.799 | 0.750 | 0.799 | 0.813 | 0.813 | 0.868 | 0.813 | 0.868 | ns |
| HSTL_I_18_F | 0.258 | 0.322 | 0.339 | 0.322 | 0.339 | 0.439 | 0.456 | 0.474 | 0.456 | 0.474 | 0.549 | 0.576 | 0.606 | 0.576 | 0.606 | ns |
| HSTL_I_18_M | 0.258 | 0.322 | 0.339 | 0.322 | 0.339 | 0.562 | 0.569 | 0.602 | 0.569 | 0.602 | 0.637 | 0.653 | 0.692 | 0.653 | 0.692 | ns |
| HSTL_I_18_S | 0.258 | 0.322 | 0.339 | 0.322 | 0.339 | 0.781 | 0.781 | 0.833 | 0.781 | 0.833 | 0.816 | 0.816 | 0.871 | 0.816 | 0.871 | ns |
| HSTL_I_DCI_12_F | 0.322 | 0.378 | 0.399 | 0.378 | 0.399 | 0.393 | 0.406 | 0.429 | 0.406 | 0.429 | 0.502 | 0.534 | 0.564 | 0.534 | 0.564 | ns |
| HSTL_I_DCI_12_M | 0.322 | 0.378 | 0.399 | 0.378 | 0.399 | 0.551 | 0.556 | 0.586 | 0.556 | 0.586 | 0.644 | 0.654 | 0.694 | 0.654 | 0.694 | ns |
| HSTL_I_DCI_12_S | 0.322 | 0.378 | 0.399 | 0.378 | 0.399 | 0.754 | 0.754 | 0.803 | 0.754 | 0.803 | 0.842 | 0.842 | 0.907 | 0.842 | 0.907 | ns |
| HSTL_I_DCI_18_F | 0.258 | 0.321 | 0.339 | 0.321 | 0.339 | 0.422 | 0.445 | 0.461 | 0.445 | 0.461 | 0.509 | 0.566 | 0.595 | 0.566 | 0.595 | ns |
| HSTL_I_DCI_18_M | 0.258 | 0.321 | 0.339 | 0.321 | 0.339 | 0.551 | 0.554 | 0.585 | 0.554 | 0.585 | 0.634 | 0.643 | 0.684 | 0.643 | 0.684 | ns |
| HSTL_I_DCI_18_S | 0.258 | 0.321 | 0.339 | 0.321 | 0.339 | 0.761 | 0.761 | 0.817 | 0.761 | 0.817 | 0.836 | 0.836 | 0.900 | 0.836 | 0.900 | ns |
| HSTL_I_DCI_F | 0.288 | 0.393 | 0.415 | 0.393 | 0.415 | 0.407 | 0.431 | 0.445 | 0.431 | 0.445 | 0.517 | 0.555 | 0.575 | 0.555 | 0.575 | ns |
| HSTL_I_DCI_M | 0.288 | 0.393 | 0.415 | 0.393 | 0.415 | 0.548 | 0.552 | 0.581 | 0.552 | 0.581 | 0.635 | 0.644 | 0.684 | 0.644 | 0.684 | ns |
| HSTL_I_DCI_S | 0.288 | 0.393 | 0.415 | 0.393 | 0.415 | 0.766 | 0.766 | 0.821 | 0.766 | 0.821 | 0.847 | 0.847 | 0.912 | 0.847 | 0.912 | ns |
| HSTL_I_F | 0.322 | 0.378 | 0.399 | 0.378 | 0.399 | 0.409 | 0.423 | 0.443 | 0.423 | 0.443 | 0.514 | 0.549 | 0.581 | 0.549 | 0.581 | ns |
| HSTL_I_M | 0.322 | 0.378 | 0.399 | 0.378 | 0.399 | 0.548 | 0.554 | 0.585 | 0.554 | 0.585 | 0.624 | 0.640 | 0.677 | 0.640 | 0.677 | ns |
| HSTL_I_S | 0.322 | 0.378 | 0.399 | 0.378 | 0.399 | 0.766 | 0.766 | 0.816 | 0.766 | 0.816 | 0.811 | 0.811 | 0.866 | 0.811 | 0.866 | ns |
| HSUL_12_DCI_F | 0.319 | 0.378 | 0.399 | 0.378 | 0.399 | 0.411 | 0.425 | 0.443 | 0.425 | 0.443 | 0.520 | 0.558 | 0.586 | 0.558 | 0.586 | ns |
| HSUL_12_DCI_M | 0.319 | 0.378 | 0.399 | 0.378 | 0.399 | 0.551 | 0.556 | 0.586 | 0.556 | 0.586 | 0.644 | 0.654 | 0.694 | 0.654 | 0.694 | ns |
| HSUL_12_DCI_S | 0.319 | 0.378 | 0.399 | 0.378 | 0.399 | 0.736 | 0.736 | 0.784 | 0.736 | 0.784 | 0.821 | 0.821 | 0.886 | 0.821 | 0.886 | ns |
| HSUL_12_F | 0.305 | 0.378 | 0.399 | 0.378 | 0.399 | 0.394 | 0.412 | 0.430 | 0.412 | 0.430 | 0.494 | 0.538 | 0.566 | 0.538 | 0.566 | ns |
| HSUL_12_M | 0.305 | 0.378 | 0.399 | 0.378 | 0.399 | 0.551 | 0.551 | 0.582 | 0.551 | 0.582 | 0.632 | 0.642 | 0.679 | 0.642 | 0.679 | ns |
| HSUL_12_S | 0.305 | 0.378 | 0.399 | 0.378 | 0.399 | 0.750 | 0.750 | 0.799 | 0.750 | 0.799 | 0.813 | 0.813 | 0.868 | 0.813 | 0.868 | ns |

Table 76: IOB High Performance (HP) Switching Characteristics (cont'd)

| I/O Standards | $T_{INBUF_DELAY_PAD_I}$ | | | | | $T_{OUTBUF_DELAY_O_PAD}$ | | | | | $T_{OUTBUF_DELAY_TD_PAD}$ | | | | | Units |
|----------------|----------------------------|-------|-------|-------|-------|-----------------------------|-------|-------|-------|-------|------------------------------|-------|-------|-------|-------|-------|
| | 0.90V | | 0.85V | | 0.72V | 0.90V | | 0.85V | | 0.72V | 0.90V | | 0.85V | | 0.72V | |
| | -3 | -2 | -1 | -2 | -1 | -3 | -2 | -1 | -2 | -1 | -3 | -2 | -1 | -2 | -1 | |
| LVC MOS12_F_2 | 0.443 | 0.512 | 0.555 | 0.512 | 0.555 | 0.657 | 0.672 | 0.692 | 0.672 | 0.692 | 0.862 | 0.898 | 0.922 | 0.898 | 0.922 | ns |
| LVC MOS12_F_4 | 0.443 | 0.512 | 0.555 | 0.512 | 0.555 | 0.486 | 0.504 | 0.521 | 0.504 | 0.521 | 0.645 | 0.664 | 0.693 | 0.664 | 0.693 | ns |
| LVC MOS12_F_6 | 0.443 | 0.512 | 0.555 | 0.512 | 0.555 | 0.469 | 0.485 | 0.507 | 0.485 | 0.507 | 0.585 | 0.634 | 0.669 | 0.634 | 0.669 | ns |
| LVC MOS12_F_8 | 0.443 | 0.512 | 0.555 | 0.512 | 0.555 | 0.457 | 0.465 | 0.489 | 0.465 | 0.489 | 0.592 | 0.611 | 0.666 | 0.611 | 0.666 | ns |
| LVC MOS12_M_2 | 0.443 | 0.512 | 0.555 | 0.512 | 0.555 | 0.687 | 0.708 | 0.727 | 0.708 | 0.727 | 0.889 | 0.916 | 0.945 | 0.916 | 0.945 | ns |
| LVC MOS12_M_4 | 0.443 | 0.512 | 0.555 | 0.512 | 0.555 | 0.533 | 0.550 | 0.573 | 0.550 | 0.573 | 0.629 | 0.664 | 0.690 | 0.664 | 0.690 | ns |
| LVC MOS12_M_6 | 0.443 | 0.512 | 0.555 | 0.512 | 0.555 | 0.520 | 0.527 | 0.554 | 0.527 | 0.554 | 0.608 | 0.622 | 0.652 | 0.622 | 0.652 | ns |
| LVC MOS12_M_8 | 0.443 | 0.512 | 0.555 | 0.512 | 0.555 | 0.532 | 0.540 | 0.571 | 0.540 | 0.571 | 0.606 | 0.614 | 0.649 | 0.614 | 0.649 | ns |
| LVC MOS12_S_2 | 0.443 | 0.512 | 0.555 | 0.512 | 0.555 | 0.767 | 0.767 | 0.803 | 0.767 | 0.803 | 0.981 | 0.990 | 1.024 | 0.990 | 1.024 | ns |
| LVC MOS12_S_4 | 0.443 | 0.512 | 0.555 | 0.512 | 0.555 | 0.666 | 0.666 | 0.704 | 0.666 | 0.704 | 0.803 | 0.803 | 0.848 | 0.803 | 0.848 | ns |
| LVC MOS12_S_6 | 0.443 | 0.512 | 0.555 | 0.512 | 0.555 | 0.657 | 0.657 | 0.695 | 0.657 | 0.695 | 0.732 | 0.732 | 0.774 | 0.732 | 0.774 | ns |
| LVC MOS12_S_8 | 0.443 | 0.512 | 0.555 | 0.512 | 0.555 | 0.708 | 0.708 | 0.761 | 0.708 | 0.761 | 0.745 | 0.745 | 0.790 | 0.745 | 0.790 | ns |
| LVC MOS15_F_12 | 0.368 | 0.414 | 0.445 | 0.414 | 0.445 | 0.485 | 0.500 | 0.522 | 0.500 | 0.522 | 0.584 | 0.647 | 0.682 | 0.647 | 0.682 | ns |
| LVC MOS15_F_2 | 0.368 | 0.414 | 0.445 | 0.414 | 0.445 | 0.686 | 0.702 | 0.722 | 0.702 | 0.722 | 0.893 | 0.919 | 0.940 | 0.919 | 0.940 | ns |
| LVC MOS15_F_4 | 0.368 | 0.414 | 0.445 | 0.414 | 0.445 | 0.567 | 0.579 | 0.601 | 0.579 | 0.601 | 0.727 | 0.755 | 0.781 | 0.755 | 0.781 | ns |
| LVC MOS15_F_6 | 0.368 | 0.414 | 0.445 | 0.414 | 0.445 | 0.533 | 0.547 | 0.569 | 0.547 | 0.569 | 0.684 | 0.711 | 0.742 | 0.711 | 0.742 | ns |
| LVC MOS15_F_8 | 0.368 | 0.414 | 0.445 | 0.414 | 0.445 | 0.500 | 0.518 | 0.538 | 0.518 | 0.538 | 0.635 | 0.686 | 0.703 | 0.686 | 0.703 | ns |
| LVC MOS15_M_12 | 0.368 | 0.414 | 0.445 | 0.414 | 0.445 | 0.607 | 0.607 | 0.644 | 0.607 | 0.644 | 0.637 | 0.637 | 0.676 | 0.637 | 0.676 | ns |
| LVC MOS15_M_2 | 0.368 | 0.414 | 0.445 | 0.414 | 0.445 | 0.736 | 0.741 | 0.770 | 0.741 | 0.770 | 0.929 | 0.938 | 0.962 | 0.938 | 0.962 | ns |
| LVC MOS15_M_4 | 0.368 | 0.414 | 0.445 | 0.414 | 0.445 | 0.610 | 0.625 | 0.651 | 0.625 | 0.651 | 0.733 | 0.754 | 0.786 | 0.754 | 0.786 | ns |
| LVC MOS15_M_6 | 0.368 | 0.414 | 0.445 | 0.414 | 0.445 | 0.564 | 0.576 | 0.604 | 0.576 | 0.604 | 0.655 | 0.674 | 0.710 | 0.674 | 0.710 | ns |
| LVC MOS15_M_8 | 0.368 | 0.414 | 0.445 | 0.414 | 0.445 | 0.565 | 0.568 | 0.601 | 0.568 | 0.601 | 0.634 | 0.639 | 0.681 | 0.639 | 0.681 | ns |
| LVC MOS15_S_12 | 0.368 | 0.414 | 0.445 | 0.414 | 0.445 | 0.788 | 0.788 | 0.855 | 0.788 | 0.855 | 0.695 | 0.695 | 0.733 | 0.695 | 0.733 | ns |
| LVC MOS15_S_2 | 0.368 | 0.414 | 0.445 | 0.414 | 0.445 | 0.829 | 0.829 | 0.864 | 0.829 | 0.864 | 1.038 | 1.039 | 1.079 | 1.039 | 1.079 | ns |
| LVC MOS15_S_4 | 0.368 | 0.414 | 0.445 | 0.414 | 0.445 | 0.687 | 0.687 | 0.725 | 0.687 | 0.725 | 0.813 | 0.813 | 0.851 | 0.813 | 0.851 | ns |
| LVC MOS15_S_6 | 0.368 | 0.414 | 0.445 | 0.414 | 0.445 | 0.671 | 0.671 | 0.710 | 0.671 | 0.710 | 0.726 | 0.726 | 0.763 | 0.726 | 0.763 | ns |
| LVC MOS15_S_8 | 0.368 | 0.414 | 0.445 | 0.414 | 0.445 | 0.704 | 0.704 | 0.755 | 0.704 | 0.755 | 0.721 | 0.721 | 0.758 | 0.721 | 0.758 | ns |
| LVC MOS18_F_12 | 0.352 | 0.418 | 0.445 | 0.418 | 0.445 | 0.564 | 0.573 | 0.601 | 0.573 | 0.601 | 0.696 | 0.731 | 0.769 | 0.731 | 0.769 | ns |
| LVC MOS18_F_2 | 0.352 | 0.418 | 0.445 | 0.418 | 0.445 | 0.723 | 0.739 | 0.760 | 0.739 | 0.760 | 0.918 | 0.945 | 0.971 | 0.945 | 0.971 | ns |
| LVC MOS18_F_4 | 0.352 | 0.418 | 0.445 | 0.418 | 0.445 | 0.598 | 0.609 | 0.630 | 0.609 | 0.630 | 0.749 | 0.778 | 0.802 | 0.778 | 0.802 | ns |
| LVC MOS18_F_6 | 0.352 | 0.418 | 0.445 | 0.418 | 0.445 | 0.598 | 0.603 | 0.633 | 0.603 | 0.633 | 0.781 | 0.781 | 0.808 | 0.781 | 0.808 | ns |
| LVC MOS18_F_8 | 0.352 | 0.418 | 0.445 | 0.418 | 0.445 | 0.567 | 0.573 | 0.600 | 0.573 | 0.600 | 0.712 | 0.733 | 0.767 | 0.733 | 0.767 | ns |
| LVC MOS18_M_12 | 0.352 | 0.418 | 0.445 | 0.418 | 0.445 | 0.640 | 0.640 | 0.678 | 0.640 | 0.678 | 0.670 | 0.670 | 0.709 | 0.670 | 0.709 | ns |
| LVC MOS18_M_2 | 0.352 | 0.418 | 0.445 | 0.418 | 0.445 | 0.785 | 0.798 | 0.822 | 0.798 | 0.822 | 0.986 | 0.991 | 1.016 | 0.991 | 1.016 | ns |
| LVC MOS18_M_4 | 0.352 | 0.418 | 0.445 | 0.418 | 0.445 | 0.658 | 0.664 | 0.693 | 0.664 | 0.693 | 0.786 | 0.798 | 0.836 | 0.798 | 0.836 | ns |
| LVC MOS18_M_6 | 0.352 | 0.418 | 0.445 | 0.418 | 0.445 | 0.625 | 0.629 | 0.663 | 0.629 | 0.663 | 0.727 | 0.735 | 0.775 | 0.735 | 0.775 | ns |
| LVC MOS18_M_8 | 0.352 | 0.418 | 0.445 | 0.418 | 0.445 | 0.626 | 0.626 | 0.661 | 0.626 | 0.661 | 0.705 | 0.705 | 0.746 | 0.705 | 0.746 | ns |
| LVC MOS18_S_12 | 0.352 | 0.418 | 0.445 | 0.418 | 0.445 | 0.795 | 0.795 | 0.861 | 0.795 | 0.861 | 0.683 | 0.683 | 0.721 | 0.683 | 0.721 | ns |
| LVC MOS18_S_2 | 0.352 | 0.418 | 0.445 | 0.418 | 0.445 | 0.861 | 0.862 | 0.897 | 0.862 | 0.897 | 1.061 | 1.076 | 1.098 | 1.076 | 1.098 | ns |

Table 76: IOB High Performance (HP) Switching Characteristics (cont'd)

| I/O Standards | $T_{INBUF_DELAY_PAD_I}$ | | | | | $T_{OUTBUF_DELAY_O_PAD}$ | | | | | $T_{OUTBUF_DELAY_TD_PAD}$ | | | | | Units |
|------------------|----------------------------|-------|-------|-------|-------|-----------------------------|-------|-------|-------|-------|------------------------------|-------|-------|-------|-------|-------|
| | 0.90V | | 0.85V | | 0.72V | 0.90V | | 0.85V | | 0.72V | 0.90V | | 0.85V | | 0.72V | |
| | -3 | -2 | -1 | -2 | -1 | -3 | -2 | -1 | -2 | -1 | -3 | -2 | -1 | -2 | -1 | |
| LVC MOS18_S_4 | 0.352 | 0.418 | 0.445 | 0.418 | 0.445 | 0.716 | 0.716 | 0.758 | 0.716 | 0.758 | 0.829 | 0.829 | 0.872 | 0.829 | 0.872 | ns |
| LVC MOS18_S_6 | 0.352 | 0.418 | 0.445 | 0.418 | 0.445 | 0.682 | 0.682 | 0.724 | 0.682 | 0.724 | 0.724 | 0.724 | 0.762 | 0.724 | 0.762 | ns |
| LVC MOS18_S_8 | 0.352 | 0.418 | 0.445 | 0.418 | 0.445 | 0.707 | 0.707 | 0.760 | 0.707 | 0.760 | 0.709 | 0.709 | 0.745 | 0.709 | 0.745 | ns |
| LVDCI_15_F | 0.369 | 0.425 | 0.462 | 0.425 | 0.462 | 0.407 | 0.426 | 0.443 | 0.426 | 0.443 | 0.514 | 0.548 | 0.581 | 0.548 | 0.581 | ns |
| LVDCI_15_M | 0.369 | 0.425 | 0.462 | 0.425 | 0.462 | 0.549 | 0.553 | 0.582 | 0.553 | 0.582 | 0.632 | 0.645 | 0.685 | 0.645 | 0.685 | ns |
| LVDCI_15_S | 0.369 | 0.425 | 0.462 | 0.425 | 0.462 | 0.749 | 0.749 | 0.803 | 0.749 | 0.803 | 0.821 | 0.821 | 0.890 | 0.821 | 0.890 | ns |
| LVDCI_18_F | 0.367 | 0.414 | 0.447 | 0.414 | 0.447 | 0.422 | 0.441 | 0.459 | 0.441 | 0.459 | 0.541 | 0.560 | 0.589 | 0.560 | 0.589 | ns |
| LVDCI_18_M | 0.367 | 0.414 | 0.447 | 0.414 | 0.447 | 0.546 | 0.554 | 0.585 | 0.554 | 0.585 | 0.622 | 0.644 | 0.683 | 0.644 | 0.683 | ns |
| LVDCI_18_S | 0.367 | 0.414 | 0.447 | 0.414 | 0.447 | 0.760 | 0.760 | 0.818 | 0.760 | 0.818 | 0.837 | 0.837 | 0.899 | 0.837 | 0.899 | ns |
| LVDS | 0.508 | 0.539 | 0.620 | 0.539 | 0.620 | 0.626 | 0.626 | 0.662 | 0.626 | 0.662 | 960.447 | | | | | ns |
| MIPI_DPHY_DCI_HS | 0.305 | 0.386 | 0.415 | 0.386 | 0.415 | 0.489 | 0.502 | 0.522 | 0.502 | 0.522 | N/A | N/A | N/A | N/A | N/A | ns |
| MIPI_DPHY_DCI_LP | 8.438 | 8.438 | 8.792 | 8.438 | 8.792 | 0.895 | 0.914 | 0.937 | 0.914 | 0.937 | N/A | N/A | N/A | N/A | N/A | ns |
| POD10_DCI_F | 0.336 | 0.408 | 0.430 | 0.408 | 0.430 | 0.407 | 0.425 | 0.444 | 0.425 | 0.444 | 0.512 | 0.555 | 0.584 | 0.555 | 0.584 | ns |
| POD10_DCI_M | 0.336 | 0.408 | 0.430 | 0.408 | 0.430 | 0.533 | 0.542 | 0.571 | 0.542 | 0.571 | 0.618 | 0.640 | 0.681 | 0.640 | 0.681 | ns |
| POD10_DCI_S | 0.336 | 0.408 | 0.430 | 0.408 | 0.430 | 0.724 | 0.754 | 0.815 | 0.754 | 0.815 | 0.815 | 0.850 | 0.917 | 0.850 | 0.917 | ns |
| POD10_F | 0.336 | 0.407 | 0.430 | 0.407 | 0.430 | 0.425 | 0.438 | 0.459 | 0.438 | 0.459 | 0.531 | 0.569 | 0.601 | 0.569 | 0.601 | ns |
| POD10_M | 0.336 | 0.407 | 0.430 | 0.407 | 0.430 | 0.519 | 0.538 | 0.568 | 0.538 | 0.568 | 0.589 | 0.630 | 0.667 | 0.630 | 0.667 | ns |
| POD10_S | 0.336 | 0.407 | 0.430 | 0.407 | 0.430 | 0.752 | 0.766 | 0.821 | 0.766 | 0.821 | 0.821 | 0.836 | 0.894 | 0.836 | 0.894 | ns |
| POD12_DCI_F | 0.336 | 0.409 | 0.431 | 0.409 | 0.431 | 0.411 | 0.425 | 0.443 | 0.425 | 0.443 | 0.519 | 0.558 | 0.586 | 0.558 | 0.586 | ns |
| POD12_DCI_M | 0.336 | 0.409 | 0.431 | 0.409 | 0.431 | 0.516 | 0.543 | 0.572 | 0.543 | 0.572 | 0.602 | 0.638 | 0.678 | 0.638 | 0.678 | ns |
| POD12_DCI_S | 0.336 | 0.409 | 0.431 | 0.409 | 0.431 | 0.740 | 0.772 | 0.822 | 0.772 | 0.822 | 0.833 | 0.862 | 0.929 | 0.862 | 0.929 | ns |
| POD12_F | 0.336 | 0.409 | 0.431 | 0.409 | 0.431 | 0.438 | 0.455 | 0.476 | 0.455 | 0.476 | 0.549 | 0.595 | 0.626 | 0.595 | 0.626 | ns |
| POD12_M | 0.336 | 0.409 | 0.431 | 0.409 | 0.431 | 0.551 | 0.551 | 0.582 | 0.551 | 0.582 | 0.632 | 0.641 | 0.679 | 0.641 | 0.679 | ns |
| POD12_S | 0.336 | 0.409 | 0.431 | 0.409 | 0.431 | 0.749 | 0.767 | 0.817 | 0.767 | 0.817 | 0.818 | 0.832 | 0.889 | 0.832 | 0.889 | ns |
| SLVS_400_18 | 0.492 | 0.539 | 0.620 | 0.539 | 0.620 | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A | ns |
| SSTL12_DCI_F | 0.331 | 0.381 | 0.399 | 0.381 | 0.399 | 0.411 | 0.425 | 0.443 | 0.425 | 0.443 | 0.520 | 0.558 | 0.586 | 0.558 | 0.586 | ns |
| SSTL12_DCI_M | 0.331 | 0.381 | 0.399 | 0.381 | 0.399 | 0.549 | 0.557 | 0.587 | 0.557 | 0.587 | 0.643 | 0.654 | 0.694 | 0.654 | 0.694 | ns |
| SSTL12_DCI_S | 0.331 | 0.381 | 0.399 | 0.381 | 0.399 | 0.754 | 0.754 | 0.803 | 0.754 | 0.803 | 0.842 | 0.842 | 0.908 | 0.842 | 0.908 | ns |
| SSTL12_F | 0.320 | 0.403 | 0.403 | 0.403 | 0.403 | 0.394 | 0.412 | 0.430 | 0.412 | 0.430 | 0.494 | 0.538 | 0.566 | 0.538 | 0.566 | ns |
| SSTL12_M | 0.320 | 0.403 | 0.403 | 0.403 | 0.403 | 0.550 | 0.553 | 0.584 | 0.553 | 0.584 | 0.630 | 0.641 | 0.676 | 0.641 | 0.676 | ns |
| SSTL12_S | 0.320 | 0.403 | 0.403 | 0.403 | 0.403 | 0.758 | 0.758 | 0.808 | 0.758 | 0.808 | 0.823 | 0.823 | 0.879 | 0.823 | 0.879 | ns |
| SSTL135_DCI_F | 0.341 | 0.366 | 0.399 | 0.366 | 0.399 | 0.392 | 0.411 | 0.428 | 0.411 | 0.428 | 0.494 | 0.537 | 0.565 | 0.537 | 0.565 | ns |
| SSTL135_DCI_M | 0.341 | 0.366 | 0.399 | 0.366 | 0.399 | 0.551 | 0.551 | 0.582 | 0.551 | 0.582 | 0.643 | 0.645 | 0.685 | 0.645 | 0.685 | ns |
| SSTL135_DCI_S | 0.341 | 0.366 | 0.399 | 0.366 | 0.399 | 0.746 | 0.746 | 0.799 | 0.746 | 0.799 | 0.829 | 0.829 | 0.893 | 0.829 | 0.893 | ns |
| SSTL135_F | 0.321 | 0.378 | 0.399 | 0.378 | 0.399 | 0.393 | 0.408 | 0.428 | 0.408 | 0.428 | 0.491 | 0.528 | 0.561 | 0.528 | 0.561 | ns |
| SSTL135_M | 0.321 | 0.378 | 0.399 | 0.378 | 0.399 | 0.548 | 0.555 | 0.585 | 0.555 | 0.585 | 0.621 | 0.641 | 0.679 | 0.641 | 0.679 | ns |
| SSTL135_S | 0.321 | 0.378 | 0.399 | 0.378 | 0.399 | 0.772 | 0.772 | 0.823 | 0.772 | 0.823 | 0.827 | 0.827 | 0.878 | 0.827 | 0.878 | ns |
| SSTL15_DCI_F | 0.319 | 0.402 | 0.417 | 0.402 | 0.417 | 0.394 | 0.412 | 0.429 | 0.412 | 0.429 | 0.497 | 0.531 | 0.563 | 0.531 | 0.563 | ns |
| SSTL15_DCI_M | 0.319 | 0.402 | 0.417 | 0.402 | 0.417 | 0.549 | 0.553 | 0.583 | 0.553 | 0.583 | 0.632 | 0.645 | 0.685 | 0.645 | 0.685 | ns |

Table 76: IOB High Performance (HP) Switching Characteristics (cont'd)

| I/O Standards | $T_{\text{INBUF_DELAY_PAD_I}}$ | | | | | $T_{\text{OUTBUF_DELAY_O_PAD}}$ | | | | | $T_{\text{OUTBUF_DELAY_TD_PAD}}$ | | | | | Units |
|----------------|-----------------------------------|-------|-------|-------|-------|------------------------------------|-------|-------|-------|-------|-------------------------------------|---------|-------|-------|-------|-------|
| | 0.90V | | 0.85V | | 0.72V | 0.90V | | 0.85V | | 0.72V | 0.90V | | 0.85V | | 0.72V | |
| | -3 | -2 | -1 | -2 | -1 | -3 | -2 | -1 | -2 | -1 | -3 | -2 | -1 | -2 | -1 | |
| SSTL15_DCI_S | 0.319 | 0.402 | 0.417 | 0.402 | 0.417 | 0.768 | 0.768 | 0.822 | 0.768 | 0.822 | 0.847 | 0.847 | 0.912 | 0.847 | 0.912 | ns |
| SSTL15_F | 0.320 | 0.371 | 0.400 | 0.371 | 0.400 | 0.393 | 0.408 | 0.428 | 0.408 | 0.428 | 0.494 | 0.530 | 0.556 | 0.530 | 0.556 | ns |
| SSTL15_M | 0.320 | 0.371 | 0.400 | 0.371 | 0.400 | 0.547 | 0.554 | 0.585 | 0.554 | 0.585 | 0.624 | 0.639 | 0.677 | 0.639 | 0.677 | ns |
| SSTL15_S | 0.320 | 0.371 | 0.400 | 0.371 | 0.400 | 0.767 | 0.767 | 0.817 | 0.767 | 0.817 | 0.813 | 0.813 | 0.867 | 0.813 | 0.867 | ns |
| SSTL18_I_DCI_F | 0.256 | 0.329 | 0.336 | 0.329 | 0.336 | 0.422 | 0.445 | 0.461 | 0.445 | 0.461 | 0.540 | 0.566 | 0.595 | 0.566 | 0.595 | ns |
| SSTL18_I_DCI_M | 0.256 | 0.329 | 0.336 | 0.329 | 0.336 | 0.552 | 0.554 | 0.585 | 0.554 | 0.585 | 0.629 | 0.644 | 0.683 | 0.644 | 0.683 | ns |
| SSTL18_I_DCI_S | 0.256 | 0.329 | 0.336 | 0.329 | 0.336 | 0.762 | 0.762 | 0.818 | 0.762 | 0.818 | 0.837 | 0.837 | 0.899 | 0.837 | 0.899 | ns |
| SSTL18_I_F | 0.259 | 0.316 | 0.337 | 0.316 | 0.337 | 0.439 | 0.454 | 0.476 | 0.454 | 0.476 | 0.549 | 0.578 | 0.608 | 0.578 | 0.608 | ns |
| SSTL18_I_M | 0.259 | 0.316 | 0.337 | 0.316 | 0.337 | 0.567 | 0.571 | 0.603 | 0.571 | 0.603 | 0.535 | 0.652 | 0.692 | 0.652 | 0.692 | ns |
| SSTL18_I_S | 0.259 | 0.316 | 0.337 | 0.316 | 0.337 | 0.782 | 0.782 | 0.835 | 0.782 | 0.835 | 0.816 | 0.816 | 0.870 | 0.816 | 0.870 | ns |
| SUB_LVDS | 0.508 | 0.539 | 0.620 | 0.539 | 0.620 | 0.658 | 0.660 | 0.692 | 0.660 | 0.692 | 907.4 | 969.863 | | | | ns |

IOB 3-state Output Switching Characteristics

Table 77 specifies the values of $T_{\text{OUTBUF_DELAY_TE_PAD}}$ and $T_{\text{INBUF_DELAY_IBUFDIS_O}}$.

- $T_{\text{OUTBUF_DELAY_TE_PAD}}$ is the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state).
- $T_{\text{INBUF_DELAY_IBUFDIS_O}}$ is the IOB delay from IBUFDISABLE to O output.
- In HP I/O banks, the internal DCI termination turn-off time is always faster than $T_{\text{OUTBUF_DELAY_TE_PAD}}$ when the DCITERMDISABLE pin is used.
- In HD I/O banks, the internal IN_TERM termination turn-off time is always faster than $T_{\text{OUTBUF_DELAY_TE_PAD}}$ when the INTERMDISABLE pin is used.

Table 77: IOB 3-state Output Switching Characteristics

| Symbol | Description | Speed Grade and V_{CCINT} Operating Voltages | | | | | Units |
|---------------------------------------|---|---|-------|-------|-------|-------|-------|
| | | 0.90V | | 0.85V | | 0.72V | |
| | | -3 | -2 | -1 | -2 | -1 | |
| $T_{\text{OUTBUF_DELAY_TE_PAD}}$ | T input to pad high-impedance for HD I/O banks | 6.167 | 6.318 | 6.369 | 6.699 | 6.752 | ns |
| | T input to pad high-impedance for HP I/O banks | 5.330 | 5.330 | 5.341 | 5.330 | 5.341 | ns |
| $T_{\text{INBUF_DELAY_IBUFDIS_O}}$ | IBUF turn-on time from IBUFDISABLE to O output for HD I/O banks | 2.266 | 2.266 | 2.430 | 2.266 | 2.430 | ns |
| | IBUF turn-on time from IBUFDISABLE to O output for HP I/O banks | 0.873 | 0.936 | 1.037 | 0.936 | 1.037 | ns |

Input Delay Measurement Methodology

The following table shows the test setup parameters used for measuring input delay.

Table 78: Input Delay Measurement Methodology

| Description | I/O Standard Attribute | $V_L^{1,2}$ | $V_H^{1,2}$ | $V_{MEAS}^{1,4}$ | $V_{REF}^{1,3,5}$ |
|--|---------------------------------|--------------------|--------------------|------------------|-------------------|
| LVC MOS, 1.2V | LVC MOS12 | 0.1 | 1.1 | 0.6 | – |
| LVC MOS, LVDCI, HSLVDCI, 1.5V | LVC MOS15, LVDCI_15, HSLVDCI_15 | 0.1 | 1.4 | 0.75 | – |
| LVC MOS, LVDCI, HSLVDCI, 1.8V | LVC MOS18, LVDCI_18, HSLVDCI_18 | 0.1 | 1.7 | 0.9 | – |
| LVC MOS, 2.5V | LVC MOS25 | 0.1 | 2.4 | 1.25 | – |
| LVC MOS, 3.3V | LVC MOS33 | 0.1 | 3.2 | 1.65 | – |
| LV TTL, 3.3V | LV TTL | 0.1 | 3.2 | 1.65 | – |
| HSTL (high-speed transceiver logic), class I, 1.2V | HSTL_I_12 | $V_{REF} - 0.25$ | $V_{REF} + 0.25$ | V_{REF} | 0.6 |
| HSTL, class I, 1.5V | HSTL_I | $V_{REF} - 0.325$ | $V_{REF} + 0.325$ | V_{REF} | 0.75 |
| HSTL, class I, 1.8V | HSTL_I_18 | $V_{REF} - 0.4$ | $V_{REF} + 0.4$ | V_{REF} | 0.9 |
| HSUL (high-speed unterminated logic), 1.2V | HSUL_12 | $V_{REF} - 0.25$ | $V_{REF} + 0.25$ | V_{REF} | 0.6 |
| SSTL12 (stub series terminated logic), 1.2V | SSTL12 | $V_{REF} - 0.25$ | $V_{REF} + 0.25$ | V_{REF} | 0.6 |
| SSTL135 and SSTL135 class II, 1.35V | SSTL135, SSTL135_II | $V_{REF} - 0.2875$ | $V_{REF} + 0.2875$ | V_{REF} | 0.675 |
| SSTL15 and SSTL15 class II, 1.5V | SSTL15, SSTL15_II | $V_{REF} - 0.325$ | $V_{REF} + 0.325$ | V_{REF} | 0.75 |
| SSTL18, class I and II, 1.8V | SSTL18_I, SSTL18_II | $V_{REF} - 0.4$ | $V_{REF} + 0.4$ | V_{REF} | 0.9 |
| POD10, 1.0V | POD10 | $V_{REF} - 0.2$ | $V_{REF} + 0.2$ | V_{REF} | 0.7 |
| POD12, 1.2V | POD12 | $V_{REF} - 0.24$ | $V_{REF} + 0.24$ | V_{REF} | 0.84 |
| DIFF_HSTL, class I, 1.2V | DIFF_HSTL_I_12 | $0.6 - 0.25$ | $0.6 + 0.25$ | 0^6 | – |
| DIFF_HSTL, class I, 1.5V | DIFF_HSTL_I | $0.75 - 0.325$ | $0.75 + 0.325$ | 0^6 | – |
| DIFF_HSTL, class I, 1.8V | DIFF_HSTL_I_18 | $0.9 - 0.4$ | $0.9 + 0.4$ | 0^6 | – |
| DIFF_HSUL, 1.2V | DIFF_HSUL_12 | $0.6 - 0.25$ | $0.6 + 0.25$ | 0^6 | – |
| DIFF_SSTL, 1.2V | DIFF_SSTL12 | $0.6 - 0.25$ | $0.6 + 0.25$ | 0^6 | – |
| DIFF_SSTL135 and DIFF_SSTL135 class II, 1.35V | DIFF_SSTL135, DIFF_SSTL135_II | $0.675 - 0.2875$ | $0.675 + 0.2875$ | 0^6 | – |
| DIFF_SSTL15 and DIFF_SSTL15 class II, 1.5V | DIFF_SSTL15, DIFF_SSTL15_II | $0.75 - 0.325$ | $0.75 + 0.325$ | 0^6 | – |
| DIFF_SSTL18_I, DIFF_SSTL18_II, 1.8V | DIFF_SSTL18_I, DIFF_SSTL18_II | $0.9 - 0.4$ | $0.9 + 0.4$ | 0^6 | – |
| DIFF_POD10, 1.0V | DIFF_POD10 | $0.5 - 0.2$ | $0.5 + 0.2$ | 0^6 | – |
| DIFF_POD12, 1.2V | DIFF_POD12 | $0.6 - 0.25$ | $0.6 + 0.25$ | 0^6 | – |
| LVDS (low-voltage differential signaling), 1.8V | LVDS | $0.9 - 0.125$ | $0.9 + 0.125$ | 0^6 | – |
| LVDS_25, 2.5V | LVDS_25 | $1.25 - 0.125$ | $1.25 + 0.125$ | 0^6 | – |
| SUB_LVDS, 1.8V | SUB_LVDS | $0.9 - 0.125$ | $0.9 + 0.125$ | 0^6 | – |
| SLVS, 1.8V | SLVS_400_18 | $0.9 - 0.125$ | $0.9 + 0.125$ | 0^6 | – |
| SLVS, 2.5V | SLVS_400_25 | $1.25 - 0.125$ | $1.25 + 0.125$ | 0^6 | – |
| LVPECL, 2.5V | LVPECL | $1.25 - 0.125$ | $1.25 + 0.125$ | 0^6 | – |
| MIPI D-PHY (high speed) 1.2V | MIPI_DPHY_DCI_HS | $0.2 - 0.125$ | $0.2 + 0.125$ | 0^6 | – |

Table 78: Input Delay Measurement Methodology (cont'd)

| Description | I/O Standard Attribute | $V_L^{1,2}$ | $V_H^{1,2}$ | $V_{MEAS}^{1,4}$ | $V_{REF}^{1,3,5}$ |
|-----------------------------|------------------------|-------------|-------------|------------------|-------------------|
| MIPI D-PHY (low power) 1.2V | MIPI_DPHY_DCI_LP | 0.715 - 0.2 | 0.715 + 0.2 | 0 ⁶ | - |

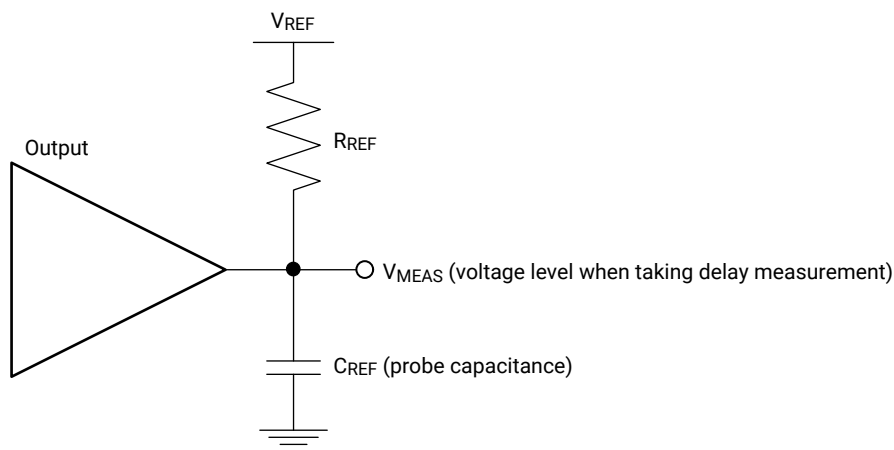
Notes:

1. The input delay measurement methodology parameters for LVDCI/HSLVDCI are the same for LVCMOS standards of the same voltage. Parameters for all other DCI standards are the same for the corresponding non-DCI standards.
2. Input waveform switches between V_L and V_H .
3. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst case of these measurements. V_{REF} values listed are typical.
4. Input voltage level from which measurement starts.
5. This is an input voltage reference that bears no relation to the V_{REF}/V_{MEAS} parameters found in IBIS models and/or noted in Figure 1.
6. The value given is the differential input voltage.

Output Delay Measurement Methodology

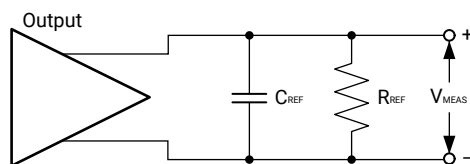
Output delays are measured with short output traces. Standard termination was used for all testing. The propagation delay of the trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setups shown in Figure 1 and Figure 2.

Figure 1: Single-Ended Test Setup



X16654-072117

Figure 2: Differential Test Setup



X16640-072117

Parameters V_{REF} , R_{REF} , C_{REF} , and V_{MEAS} fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using this method:

1. Simulate the output driver of choice into the generalized test setup using values from Table 79.

2. Record the time to V_{MEAS} .
3. Simulate the output driver of choice into the actual PCB trace and load using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS} .
5. Compare the results of step 2 and step 4. The increase or decrease in delay yields the actual propagation delay of the PCB trace.

Table 79: Output Delay Measurement Methodology

| Description | I/O Standard Attribute | R_{REF} (Ω) | C_{REF} ¹ (pF) | V_{MEAS} (V) | V_{REF} (V) |
|--|-------------------------------|---------------------------|--------------------------------|-------------------|------------------|
| LVC MOS, 1.2V | LVC MOS12 | 1M | 0 | 0.6 | 0 |
| LVC MOS, 1.5V | LVC MOS15 | 1M | 0 | 0.75 | 0 |
| LVC MOS, 1.8V | LVC MOS18 | 1M | 0 | 0.9 | 0 |
| LVC MOS, 2.5V | LVC MOS25 | 1M | 0 | 1.25 | 0 |
| LVC MOS, 3.3V | LVC MOS33 | 1M | 0 | 1.65 | 0 |
| LV TTL, 3.3V | LV TTL | 1M | 0 | 1.65 | 0 |
| LVDCI, HSLVDCI, 1.5V | LVDCI_15, HSLVDCI_15 | 50 | 0 | V_{REF} | 0.75 |
| LVDCI, HSLVDCI, 1.8V | LVDCI_15, HSLVDCI_18 | 50 | 0 | V_{REF} | 0.9 |
| HSTL (high-speed transceiver logic), class I, 1.2V | HSTL_I_12 | 50 | 0 | V_{REF} | 0.6 |
| HSTL, class I, 1.5V | HSTL_I | 50 | 0 | V_{REF} | 0.75 |
| HSTL, class I, 1.8V | HSTL_I_18 | 50 | 0 | V_{REF} | 0.9 |
| HSUL (high-speed unterminated logic), 1.2V | HSUL_12 | 50 | 0 | V_{REF} | 0.6 |
| SSTL12 (stub series terminated logic), 1.2V | SSTL12 | 50 | 0 | V_{REF} | 0.6 |
| SSTL135 and SSTL135 class II, 1.35V | SSTL135, SSTL135_II | 50 | 0 | V_{REF} | 0.675 |
| SSTL15 and SSTL15 class II, 1.5V | SSTL15, SSTL15_II | 50 | 0 | V_{REF} | 0.75 |
| SSTL18, class I and class II, 1.8V | SSTL18_I, SSTL18_II | 50 | 0 | V_{REF} | 0.9 |
| POD10, 1.0V | POD10 | 50 | 0 | V_{REF} | 1.0 |
| POD12, 1.2V | POD12 | 50 | 0 | V_{REF} | 1.2 |
| DIFF_HSTL, class I, 1.2V | DIFF_HSTL_I_12 | 50 | 0 | V_{REF} | 0.6 |
| DIFF_HSTL, class I, 1.5V | DIFF_HSTL_I | 50 | 0 | V_{REF} | 0.75 |
| DIFF_HSTL, class I, 1.8V | DIFF_HSTL_I_18 | 50 | 0 | V_{REF} | 0.9 |
| DIFF_HSUL, 1.2V | DIFF_HSUL_12 | 50 | 0 | V_{REF} | 0.6 |
| DIFF_SSTL12, 1.2V | DIFF_SSTL12 | 50 | 0 | V_{REF} | 0.6 |
| DIFF_SSTL135 and DIFF_SSTL135 class II, 1.35V | DIFF_SSTL135, DIFF_SSTL135_II | 50 | 0 | V_{REF} | 0.675 |
| DIFF_SSTL15 and DIFF_SSTL15 class II, 1.5V | DIFF_SSTL15, DIFF_SSTL15_II | 50 | 0 | V_{REF} | 0.75 |
| DIFF_SSTL18, class I and II, 1.8V | DIFF_SSTL18_I, DIFF_SSTL18_II | 50 | 0 | V_{REF} | 0.9 |
| DIFF_POD10, 1.0V | DIFF_POD10 | 50 | 0 | V_{REF} | 1.0 |
| DIFF_POD12, 1.2V | DIFF_POD12 | 50 | 0 | V_{REF} | 1.2 |
| LVDS (low-voltage differential signaling), 1.8V | LVDS | 100 | 0 | 0 ² | 0 |
| SUB_LVDS, 1.8V | SUB_LVDS | 100 | 0 | 0 ² | 0 |
| MIPI D-PHY (high speed) 1.2V | MIPI_DPHY_DCI_HS | 100 | 0 | 0 ² | 0 |

Table 79: Output Delay Measurement Methodology (cont'd)

| Description | I/O Standard Attribute | R _{REF} (Ω) | C _{REF} ¹ (pF) | V _{MEAS} (V) | V _{REF} (V) |
|-----------------------------|------------------------|----------------------------------|---------------------------------------|--------------------------|-------------------------|
| MIPI D-PHY (low power) 1.2V | MIPI_DPHY_DCI_LP | 1M | 0 | 0.6 | 0 |

Notes:

1. C_{REF} is the capacitance of the probe, nominally 0 pF.
2. The value given is the differential output voltage.

Block RAM and FIFO Switching Characteristics

Table 80: Block RAM and FIFO Switching Characteristics

| Symbol | Description | Speed Grade and V _{CCINT} Operating Voltages | | | | | Units |
|---|--|---|------|-------|------|-------|---------|
| | | 0.90V | | 0.85V | | 0.72V | |
| | | -3 | -2 | -1 | -2 | -1 | |
| Maximum Frequency | | | | | | | |
| F _{MAX_WF_NC} | Block RAM (WRITE_FIRST and NO_CHANGE modes) | 825 | 738 | 645 | 585 | 516 | MHz |
| F _{MAX_RF} | Block RAM (READ_FIRST mode) | 718 | 637 | 575 | 510 | 460 | MHz |
| F _{MAX_FIFO} | FIFO in all modes without ECC | 825 | 738 | 645 | 585 | 516 | MHz |
| F _{MAX_ECC} | Block RAM and FIFO in ECC configuration without PIPELINE | 718 | 637 | 575 | 510 | 460 | MHz |
| | Block RAM and FIFO in ECC configuration with PIPELINE and Block RAM in WRITE_FIRST or NO_CHANGE mode | 825 | 738 | 645 | 585 | 516 | MHz |
| T _{PW} ¹ | Minimum pulse width | 495 | 542 | 543 | 577 | 578 | ps |
| Block RAM and FIFO Clock-to-Out Delays | | | | | | | |
| T _{RCKO_DO} | Clock CLK to DOUT output (without output register) | 0.91 | 1.02 | 1.11 | 1.46 | 1.53 | ns, Max |
| T _{RCKO_DO_REG} | Clock CLK to DOUT output (with output register) | 0.27 | 0.29 | 0.30 | 0.42 | 0.44 | ns, Max |

Notes:

1. The MMCM and PLL DUTY_CYCLE attribute should be set to 50% to meet the pulse-width requirements at the higher frequencies.

UltraRAM Switching Characteristics

The *UltraScale Architecture and Product Data Sheet: Overview* (DS890) lists the Zynq UltraScale+ MPSoCs that include this memory.

Table 81: UltraRAM Switching Characteristics

| Symbol | Description | Speed Grade and V _{CCINT} Operating Voltages | | | | | Units |
|---------------------------------|--|---|-------|-----|-------|-----|-------|
| | | 0.90V | 0.85V | | 0.72V | | |
| | | -3 | -2 | -1 | -2 | -1 | |
| Maximum Frequency | | | | | | | |
| F _{MAX} | UltraRAM maximum frequency with OREG_B = True | 650 | 600 | 575 | 500 | 481 | MHz |
| F _{MAX_ECC_NOPIPELINE} | UltraRAM maximum frequency with OREG_B = False and EN_ECC_RD_B = True | 435 | 400 | 386 | 312 | 303 | MHz |
| F _{MAX_NOPIPELINE} | UltraRAM maximum frequency with OREG_B = False and EN_ECC_RD_B = False | 528 | 500 | 478 | 404 | 389 | MHz |
| T _{PW} ¹ | Minimum pulse width | 650 | 700 | 730 | 800 | 832 | ps |
| T _{RSTPW} | Asynchronous reset minimum pulse width. One cycle required | 1 clock cycle | | | | | |

Notes:

- The MMCM and PLL DUTY_CYCLE attribute should be set to 50% to meet the pulse-width requirements at the higher frequencies.

Input/Output Delay Switching Characteristics

Table 82: Input/Output Delay Switching Characteristics

| Symbol | Description | Speed Grade and V _{CCINT} Operating Voltages | | | | | Units |
|--|---|---|----------------|-------------|-------------|-------------|-------|
| | | 0.90V | 0.85V | | 0.72V | | |
| | | -3 | -2 | -1 | -2 | -1 | |
| F _{REFCLK} | Reference clock frequency for IDELAYCTRL (component mode) | 300 to 800 | | | | | MHz |
| | Reference clock frequency when using BITSlice_CONTROL with REFCLK (in native mode (for RX_BITSlice only)) | 300 to 800 | | | | | MHz |
| | Reference clock frequency for BITSlice_CONTROL with PLL_CLK (in native mode) ¹ | 300 to 2666.67 | 300 to 2666.67 | 300 to 2400 | 300 to 2400 | 300 to 2133 | MHz |
| T _{MINPER_CLK} | Minimum period for IODELAY clock | 3.195 | 3.195 | 3.195 | 3.195 | 3.195 | ns |
| T _{MINPER_RST} | Minimum reset pulse width | 52.00 | | | | | ns |
| T _{IDELAY_RESOLUTION} / T _{ODELAY_RESOLUTION} | IDELAY/ODELAY chain resolution | 2.1 to 12 | | | | | ps |

Notes:

- PLL settings could restrict the minimum allowable data rate. For example, when using a PLL with CLKOUTPHY_MODE = VCO_HALF, the minimum frequency is PLL_F_{VCOMIN}/2.

DSP48 Slice Switching Characteristics

Table 83: DSP48 Slice Switching Characteristics

| Symbol | Description | Speed Grade and V _{CCINT} Operating Voltages | | | | | Units |
|---------------------------------------|--|---|-------|-----|--------------------|-----|-------|
| | | 0.90V | 0.85V | | 0.72V ¹ | | |
| | | -3 | -2 | -1 | -2 | -1 | |
| Maximum Frequency | | | | | | | |
| F _{MAX} | With all registers used | 891 | 775 | 645 | 644 | 600 | MHz |
| F _{MAX_PATDET} | With pattern detector | 794 | 687 | 571 | 562 | 524 | MHz |
| F _{MAX_MULT_NOMREG} | Two register multiply without MREG | 635 | 544 | 456 | 440 | 413 | MHz |
| F _{MAX_MULT_NOMREG_PATDET} | Two register multiply without MREG with pattern detect | 577 | 492 | 410 | 395 | 371 | MHz |
| F _{MAX_PREADD_NOADREG} | Without ADREG | 655 | 565 | 468 | 453 | 423 | MHz |
| F _{MAX_NOPIPELINEREG} | Without pipeline registers (MREG, ADREG) | 483 | 410 | 338 | 323 | 304 | MHz |
| F _{MAX_NOPIPELINEREG_PATDET} | Without pipeline registers (MREG, ADREG) with pattern detect | 448 | 379 | 314 | 299 | 280 | MHz |

Notes:

- For devices operating at the lower power V_{CCINT} = 0.72V voltages, DSP cascades that cross the clock region center might operate below the specified F_{MAX}.

Clock Buffers and Networks

Table 84: Clock Buffers Switching Characteristics

| Symbol | Description | Speed Grade and V _{CCINT} Operating Voltages | | | | | Units |
|--|--|---|-------|-----|-------|-----|-------|
| | | 0.90V | 0.85V | | 0.72V | | |
| | | -3 | -2 | -1 | -2 | -1 | |
| Global Clock Switching Characteristics (Including BUFGCTRL) | | | | | | | |
| F _{MAX} | Maximum frequency of a global clock tree (BUFG) | 891 | 775 | 667 | 725 | 667 | MHz |
| Global Clock Buffer with Input Divide Capability (BUFGCE_DIV) | | | | | | | |
| F _{MAX} | Maximum frequency of a global clock buffer with input divide capability (BUFGCE_DIV) | 891 | 775 | 667 | 725 | 667 | MHz |
| Global Clock Buffer with Clock Enable (BUFGCE) | | | | | | | |
| F _{MAX} | Maximum frequency of a global clock buffer with clock enable (BUFGCE) | 891 | 775 | 667 | 725 | 667 | MHz |
| Leaf Clock Buffer with Clock Enable (BUFCE_LEAF) | | | | | | | |
| F _{MAX} | Maximum frequency of a leaf clock buffer with clock enable (BUFCE_LEAF) | 891 | 775 | 667 | 725 | 667 | MHz |
| GTH or GTY Clock Buffer with Clock Enable and Clock Input Divide Capability (BUFG_GT) | | | | | | | |
| F _{MAX} | Maximum frequency of a serial transceiver clock buffer with clock enable and clock input divide capability | 512 | 512 | 512 | 512 | 512 | MHz |

MMCM Switching Characteristics

Table 85: MMCM Specification

| Symbol | Description | Speed Grade and V _{CCINT} Operating Voltages | | | | | Units |
|---------------------------------|--|---|-------|------|-------|------|-------|
| | | 0.90V | 0.85V | | 0.72V | | |
| | | -3 | -2 | -1 | -2 | -1 | |
| MMCM_F _{INMAX} | Maximum input clock frequency | 1066 | 933 | 800 | 933 | 800 | MHz |
| MMCM_F _{INMIN} | Minimum input clock frequency | 10 | 10 | 10 | 10 | 10 | MHz |
| MMCM_F _{INJITTER} | Maximum input clock period jitter | < 20% of clock input period or 1 ns Max | | | | | |
| MMCM_F _{INDUTY} | Input duty cycle range: 10–49 MHz | 25–75 | | | | | % |
| | Input duty cycle range: 50–199 MHz | 30–70 | | | | | % |
| | Input duty cycle range: 200–399 MHz | 35–65 | | | | | % |
| | Input duty cycle range: 400–499 MHz | 40–60 | | | | | % |
| | Input duty cycle range: >500 MHz | 45–55 | | | | | % |
| MMCM_F _{MIN_PSCLK} | Minimum dynamic phase shift clock frequency | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | MHz |
| MMCM_F _{MAX_PSCLK} | Maximum dynamic phase shift clock frequency | 550 | 500 | 450 | 500 | 450 | MHz |
| MMCM_F _{VCOMIN} | Minimum MMCM VCO frequency | 800 | 800 | 800 | 800 | 800 | MHz |
| MMCM_F _{VCOMAX} | Maximum MMCM VCO frequency | 1600 | 1600 | 1600 | 1600 | 1600 | MHz |
| MMCM_F _{BANDWIDTH} | Low MMCM bandwidth at typical ¹ | 1.00 | 1.00 | 1.00 | 1.00 | 1.00 | MHz |
| | High MMCM bandwidth at typical ¹ | 4.00 | 4.00 | 4.00 | 4.00 | 4.00 | MHz |
| MMCM_T _{STATPHAOFFSET} | Static phase offset of the MMCM outputs ² | 0.12 | 0.12 | 0.12 | 0.12 | 0.12 | ns |
| MMCM_T _{OUTJITTER} | MMCM output jitter. | Note 3 | | | | | |
| MMCM_T _{OUTDUTY} | MMCM output clock duty cycle precision ⁴ | 0.165 | 0.20 | 0.20 | 0.20 | 0.20 | ns |
| MMCM_T _{LOCKMAX} | MMCM maximum lock time for MMCM_F _{PFDMIN} | 100 | 100 | 100 | 100 | 100 | μs |
| MMCM_F _{OUTMAX} | MMCM maximum output frequency | 891 | 775 | 667 | 725 | 667 | MHz |
| MMCM_F _{OUTMIN} | MMCM minimum output frequency ^{4, 5} | 6.25 | 6.25 | 6.25 | 6.25 | 6.25 | MHz |
| MMCM_T _{EXTFDVAR} | External clock feedback variation | < 20% of clock input period or 1 ns Max | | | | | |
| MMCM_RST _{MINPULSE} | Minimum reset pulse width | 5.00 | 5.00 | 5.00 | 5.00 | 5.00 | ns |
| MMCM_F _{PFDMAX} | Maximum frequency at the phase frequency detector | 550 | 500 | 450 | 500 | 450 | MHz |
| MMCM_F _{PFDMIN} | Minimum frequency at the phase frequency detector | 10 | 10 | 10 | 10 | 10 | MHz |
| MMCM_T _{FBDelay} | Maximum delay in the feedback path | 5 ns Max or one clock cycle | | | | | |
| MMCM_F _{DPRCLK_MAX} | Maximum DRP clock frequency | 250 | 250 | 250 | 250 | 250 | MHz |

Notes:

1. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any MMCM outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard.
4. Includes global clock buffer.
5. Calculated as F_{VCO}/128 assuming output duty cycle is 50%.

PLL Switching Characteristics

Table 86: PLL Specification

| Symbol | Description ¹ | Speed Grade and V _{CCINT} Operating Voltages | | | | | Units |
|--------------------------------|---|--|-------|-------|-------|-------|-------|
| | | 0.90V | 0.85V | | 0.72V | | |
| | | -3 | -2 | -1 | -2 | -1 | |
| PLL_F _{INMAX} | Maximum input clock frequency | 1066 | 933 | 800 | 933 | 800 | MHz |
| PLL_F _{INMIN} | Minimum input clock frequency | 70 | 70 | 70 | 70 | 70 | MHz |
| PLL_F _{INJITTER} | Maximum input clock period jitter | < 20% of clock input period or 1 ns Max | | | | | |
| PLL_F _{INDUTY} | Input duty cycle range: 70–399 MHz | 35–65 | | | | | % |
| | Input duty cycle range: 400–499 MHz | 40–60 | | | | | % |
| | Input duty cycle range: >500 MHz | 45–55 | | | | | % |
| PLL_F _{VCOMIN} | Minimum PLL VCO frequency | 750 | 750 | 750 | 750 | 750 | MHz |
| PLL_F _{VCOMAX} | Maximum PLL VCO frequency | 1500 | 1500 | 1500 | 1500 | 1500 | MHz |
| PLL_T _{STATPHAOFFSET} | Static phase offset of the PLL outputs ² | 0.12 | 0.12 | 0.12 | 0.12 | 0.12 | ns |
| PLL_T _{OUTJITTER} | PLL output jitter. | Note 3 | | | | | |
| PLL_T _{OUTDUTY} | PLL CLKOUT0, CLKOUT0B, CLKOUT1, CLKOUT1B duty-cycle precision ⁴ | 0.165 | 0.20 | 0.20 | 0.20 | 0.20 | ns |
| PLL_T _{LOCKMAX} | PLL maximum lock time | 100 | | | | | µs |
| PLL_F _{OUTMAX} | PLL maximum output frequency at CLKOUT0, CLKOUT0B, CLKOUT1, CLKOUT1B | 891 | 775 | 667 | 725 | 667 | MHz |
| | PLL maximum output frequency at CLKOUTPHY | 2667 | 2667 | 2400 | 2400 | 2133 | MHz |
| PLL_F _{OUTMIN} | PLL minimum output frequency at CLKOUT0, CLKOUT0B, CLKOUT1, CLKOUT1B ⁵ | 5.86 | 5.86 | 5.86 | 5.86 | 5.86 | MHz |
| | PLL minimum output frequency at CLKOUTPHY | 2 x VCO mode: 1500, 1 x VCO mode: 750, 0.5 x VCO mode: 375 | | | | | MHz |
| PLL_R _{STMINPULSE} | Minimum reset pulse width | 5.00 | 5.00 | 5.00 | 5.00 | 5.00 | ns |
| PLL_F _{PFDMAX} | Maximum frequency at the phase frequency detector | 667.5 | 667.5 | 667.5 | 667.5 | 667.5 | MHz |
| PLL_F _{PFDMIN} | Minimum frequency at the phase frequency detector | 70 | 70 | 70 | 70 | 70 | MHz |
| PLL_F _{BANDWIDTH} | PLL bandwidth at typical | 14 | 14 | 14 | 14 | 14 | MHz |
| PLL_F _{DRPCLK_MAX} | Maximum DRP clock frequency | 250 | 250 | 250 | 250 | 250 | MHz |

Notes:

1. The PLL does not filter typical spread-spectrum input clocks because they are usually far below the loop filter frequencies.
2. The static offset is measured between any PLL outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard.
4. Includes global clock buffer.
5. Calculated as F_{VCO}/128 assuming output duty cycle is 50%.

Device Pin-to-Pin Output Parameter Guidelines

The pin-to-pin numbers in the following tables are based on the clock root placement in the center of the device. The actual pin-to-pin values will vary if the root placement selected is different. Consult the Vivado Design Suite timing report for the actual pin-to-pin values.

Table 87: Global Clock Input to Output Delay Without MMCM (Near Clock Region)

| Symbol | Description ¹ | Device | Speed Grade and V _{CCINT} Operating Voltages | | | | | Units |
|--|---|--------|---|------|-------|------|-------|-------|
| | | | 0.90V | | 0.85V | | 0.72V | |
| | | | -3 | -2 | -1 | -2 | -1 | |
| SSTL15 Global Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>without</i> MMCM | | | | | | | | |
| T _{ICKOF} | Global clock input and output flip-flop <i>without</i> MMCM (near clock region) | XCZU2 | N/A | 4.90 | 5.28 | 6.08 | 6.51 | ns |
| | | XCZU3 | N/A | 4.90 | 5.28 | 6.08 | 6.51 | ns |
| | | XCZU4 | 5.05 | 5.53 | 5.95 | 6.90 | 7.49 | ns |
| | | XCZU5 | 5.05 | 5.53 | 5.95 | 6.90 | 7.49 | ns |
| | | XCZU6 | 5.42 | 5.91 | 6.35 | 7.48 | 8.03 | ns |
| | | XCZU7 | 5.96 | 6.54 | 7.01 | 8.17 | 8.76 | ns |
| | | XCZU9 | 5.42 | 5.91 | 6.35 | 7.48 | 8.03 | ns |
| | | XCZU11 | 5.92 | 6.49 | 6.96 | 8.16 | 8.91 | ns |
| | | XCZU15 | 5.58 | 6.09 | 6.55 | 7.75 | 8.33 | ns |
| | | XCZU17 | 6.29 | 6.90 | 7.40 | 8.68 | 9.32 | ns |
| | | XCZU19 | 6.29 | 6.90 | 7.40 | 8.68 | 9.32 | ns |
| | | XAZU2 | N/A | N/A | 5.28 | N/A | 6.51 | ns |
| | | XAZU3 | N/A | N/A | 5.28 | N/A | 6.51 | ns |
| | | XAZU4 | N/A | N/A | 5.95 | N/A | 7.49 | ns |
| | | XAZU5 | N/A | N/A | 5.95 | N/A | 7.49 | ns |
| | | XAZU7 | N/A | N/A | 7.01 | N/A | N/A | ns |
| | | XAZU11 | N/A | N/A | 6.96 | N/A | N/A | ns |
| | | XQZU3 | N/A | 4.90 | 5.28 | N/A | 6.51 | ns |
| | | XQZU5 | N/A | 5.53 | 5.95 | N/A | 7.49 | ns |
| | | XQZU7 | N/A | 6.54 | 7.01 | N/A | 8.76 | ns |
| XQZU9 | N/A | 5.91 | 6.35 | N/A | 8.03 | ns | | |
| XQZU11 | N/A | 6.49 | 6.96 | N/A | 8.91 | ns | | |
| XQZU15 | N/A | 6.09 | 6.55 | N/A | 8.33 | ns | | |
| XQZU19 | N/A | 6.90 | 7.40 | N/A | 9.32 | ns | | |

Notes:

- This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net.

Table 88: Global Clock Input to Output Delay Without MMCM (Far Clock Region)

| Symbol | Description ¹ | Device | Speed Grade and V _{CCINT} Operating Voltages | | | | | Units |
|--|--|--------|---|-------|-------|-------|-------|-------|
| | | | 0.90V | 0.85V | | 0.72V | | |
| | | | -3 | -2 | -1 | -2 | -1 | |
| SSTL15 Global Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>without</i> MMCM | | | | | | | | |
| T _{ICKOF_FAR} | Global clock input and output flip-flop <i>without</i> MMCM (far clock region) | XCZU2 | N/A | 5.27 | 5.68 | 6.59 | 7.06 | ns |
| | | XCZU3 | N/A | 5.27 | 5.68 | 6.59 | 7.06 | ns |
| | | XCZU4 | 5.24 | 5.73 | 6.17 | 7.17 | 7.79 | ns |
| | | XCZU5 | 5.24 | 5.73 | 6.17 | 7.17 | 7.79 | ns |
| | | XCZU6 | 5.91 | 6.49 | 6.97 | 8.16 | 8.76 | ns |
| | | XCZU7 | 5.96 | 6.54 | 7.01 | 8.17 | 8.76 | ns |
| | | XCZU9 | 5.91 | 6.49 | 6.97 | 8.16 | 8.76 | ns |
| | | XCZU11 | 6.29 | 6.91 | 7.41 | 8.72 | 9.52 | ns |
| | | XCZU15 | 5.90 | 6.49 | 6.96 | 8.16 | 8.77 | ns |
| | | XCZU17 | 6.84 | 7.53 | 8.07 | 9.52 | 10.23 | ns |
| | | XCZU19 | 6.84 | 7.53 | 8.07 | 9.52 | 10.23 | ns |
| | | XAZU2 | N/A | N/A | 5.68 | N/A | 7.06 | ns |
| | | XAZU3 | N/A | N/A | 5.68 | N/A | 7.06 | ns |
| | | XAZU4 | N/A | N/A | 6.17 | N/A | 7.79 | ns |
| | | XAZU5 | N/A | N/A | 6.17 | N/A | 7.79 | ns |
| | | XAZU7 | N/A | N/A | 7.01 | N/A | N/A | ns |
| | | XAZU11 | N/A | N/A | 7.41 | N/A | N/A | ns |
| | | XQZU3 | N/A | 5.27 | 5.68 | N/A | 7.06 | ns |
| | | XQZU5 | N/A | 5.73 | 6.17 | N/A | 7.79 | ns |
| | | XQZU7 | N/A | 6.54 | 7.01 | N/A | 8.76 | ns |
| | | XQZU9 | N/A | 6.49 | 6.97 | N/A | 8.76 | ns |
| XQZU11 | N/A | 6.91 | 7.41 | N/A | 9.52 | ns | | |
| XQZU15 | N/A | 6.49 | 6.96 | N/A | 8.77 | ns | | |
| XQZU19 | N/A | 7.53 | 8.07 | N/A | 10.23 | ns | | |

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net.

Table 89: Global Clock Input to Output Delay With MMCM

| Symbol | Description ^{1, 2} | Device | Speed Grade and V _{CCINT} Operating Voltages | | | | | Units |
|--|---|--------|---|------|-------|------|-------|-------|
| | | | 0.90V | | 0.85V | | 0.72V | |
| | | | -3 | -2 | -1 | -2 | -1 | |
| SSTL15 Global Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, with MMCM | | | | | | | | |
| T _{ICKOFMMCMCC} | Global clock input and output flip-flop with MMCM | XCZU2 | N/A | 2.22 | 2.43 | 2.87 | 3.00 | ns |
| | | XCZU3 | N/A | 2.22 | 2.43 | 2.87 | 3.00 | ns |
| | | XCZU4 | 1.90 | 2.24 | 2.47 | 2.90 | 3.08 | ns |
| | | XCZU5 | 1.90 | 2.24 | 2.47 | 2.90 | 3.08 | ns |
| | | XCZU6 | 1.83 | 2.15 | 2.36 | 2.80 | 2.95 | ns |
| | | XCZU7 | 1.98 | 2.32 | 2.55 | 3.00 | 3.15 | ns |
| | | XCZU9 | 1.83 | 2.15 | 2.36 | 2.80 | 2.95 | ns |
| | | XCZU11 | 1.96 | 2.30 | 2.51 | 2.99 | 3.20 | ns |
| | | XCZU15 | 1.85 | 2.18 | 2.38 | 2.82 | 2.98 | ns |
| | | XCZU17 | 2.08 | 2.44 | 2.66 | 3.15 | 3.33 | ns |
| | | XCZU19 | 2.08 | 2.44 | 2.66 | 3.15 | 3.33 | ns |
| | | XAZU2 | N/A | N/A | 2.43 | N/A | 3.00 | ns |
| | | XAZU3 | N/A | N/A | 2.43 | N/A | 3.00 | ns |
| | | XAZU4 | N/A | N/A | 2.47 | N/A | 3.08 | ns |
| | | XAZU5 | N/A | N/A | 2.47 | N/A | 3.08 | ns |
| | | XAZU7 | N/A | N/A | 2.55 | N/A | N/A | ns |
| | | XAZU11 | N/A | N/A | 2.51 | N/A | N/A | ns |
| | | XQZU3 | N/A | 2.22 | 2.43 | N/A | 3.00 | ns |
| | | XQZU5 | N/A | 2.24 | 2.47 | N/A | 3.08 | ns |
| | | XQZU7 | N/A | 2.32 | 2.55 | N/A | 3.15 | ns |
| XQZU9 | N/A | 2.15 | 2.36 | N/A | 2.95 | ns | | |
| XQZU11 | N/A | 2.30 | 2.51 | N/A | 3.20 | ns | | |
| XQZU15 | N/A | 2.18 | 2.38 | N/A | 2.98 | ns | | |
| XQZU19 | N/A | 2.44 | 2.66 | N/A | 3.33 | ns | | |

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

Table 90: Source Synchronous Output Characteristics (Component Mode)

| Description | Speed Grade and V _{CCINT} Operating Voltages | | | | | Units |
|--|---|----|-------|----|-------|-------|
| | 0.90V | | 0.85V | | 0.72V | |
| | -3 | -2 | -1 | -2 | -1 | |
| T _{OUTPUT_LOGIC_DELAY_VARIATION} ¹ | 80 | | | | | ps |

Notes:

1. Delay mismatch across a transmit bus when using component mode output logic (ODDRE1, OSERDESE3) within a bank.

Device Pin-to-Pin Input Parameter Guidelines

The pin-to-pin numbers in the following tables are based on the clock root placement in the center of the device. The actual pin-to-pin values will vary if the root placement selected is different. Consult the Vivado Design Suite timing report for the actual pin-to-pin values.

Table 91: Global Clock Input Setup and Hold With 3.3V HD I/O Without MMCM

| Symbol | Description | Device | Speed Grade and V _{CCINT} Operating Voltages | | | | | Units | |
|---|---|--------|---|-------|-------|-------|-------|-------|----|
| | | | 0.90V | 0.85V | | 0.72V | | | |
| | | | -3 | -2 | -1 | -2 | -1 | | |
| Input Setup and Hold Time Relative to Global Clock Input Signal using SSTL15 Standard.^{1, 2, 3} | | | | | | | | | |
| T _{PSFD_ZU2} | Global clock input and input flip-flop (or latch) <i>without</i> MMCM | Setup | XCZU2 | N/A | 2.27 | 2.37 | 3.54 | 3.82 | ns |
| T _{PHFD_ZU2} | | Hold | | | -0.36 | -0.36 | -1.03 | -1.03 | ns |
| T _{PSFD_ZU3} | | Setup | XCZU3 | N/A | 2.27 | 2.37 | 3.54 | 3.82 | ns |
| T _{PHFD_ZU3} | | Hold | | | -0.36 | -0.36 | -1.03 | -1.03 | ns |
| T _{PSFD_ZU4} | | Setup | XCZU4 | 2.00 | 2.30 | 2.39 | 3.56 | 3.81 | ns |
| T _{PHFD_ZU4} | | Hold | | -0.37 | -0.37 | -0.37 | -1.05 | -1.05 | ns |
| T _{PSFD_ZU5} | | Setup | XCZU5 | 2.00 | 2.30 | 2.39 | 3.56 | 3.81 | ns |
| T _{PHFD_ZU5} | | Hold | | -0.37 | -0.37 | -0.37 | -1.05 | -1.05 | ns |
| T _{PSFD_ZU6} | | Setup | XCZU6 | 1.51 | 1.79 | 1.86 | 2.85 | 3.06 | ns |
| T _{PHFD_ZU6} | | Hold | | -0.05 | -0.05 | -0.05 | -0.60 | -0.60 | ns |
| T _{PSFD_ZU7} | | Setup | XCZU7 | 2.02 | 2.32 | 2.42 | 3.59 | 3.87 | ns |
| T _{PHFD_ZU7} | | Hold | | -0.40 | -0.40 | -0.40 | -1.10 | -1.10 | ns |
| T _{PSFD_ZU9} | | Setup | XCZU9 | 1.51 | 1.79 | 1.86 | 2.85 | 3.06 | ns |
| T _{PHFD_ZU9} | | Hold | | -0.05 | -0.05 | -0.05 | -0.60 | -0.60 | ns |
| T _{PSFD_ZU11} | | Setup | XCZU11 | 1.99 | 2.28 | 2.38 | 3.54 | 3.79 | ns |
| T _{PHFD_ZU11} | | Hold | | -0.38 | -0.38 | -0.38 | -1.05 | -1.05 | ns |
| T _{PSFD_ZU15} | | Setup | XCZU15 | 1.51 | 1.79 | 1.85 | 2.84 | 3.05 | ns |
| T _{PHFD_ZU15} | | Hold | | -0.04 | -0.04 | -0.04 | -0.60 | -0.60 | ns |
| T _{PSFD_ZU17} | | Setup | XCZU17 | 2.00 | 2.29 | 2.38 | 3.56 | 3.83 | ns |
| T _{PHFD_ZU17} | | Hold | | -0.38 | -0.38 | -0.38 | -1.08 | -1.08 | ns |
| T _{PSFD_ZU19} | | Setup | XCZU19 | 2.00 | 2.29 | 2.38 | 3.56 | 3.83 | ns |
| T _{PHFD_ZU19} | | Hold | | -0.38 | -0.38 | -0.38 | -1.08 | -1.08 | ns |
| T _{PSFD_XAZU2} | | Setup | XAZU2 | N/A | N/A | 2.37 | N/A | 3.82 | ns |
| T _{PHFD_XAZU2} | | Hold | | N/A | N/A | -0.36 | N/A | -1.03 | ns |
| T _{PSFD_XAZU3} | | Setup | XAZU3 | N/A | N/A | 2.37 | N/A | 3.82 | ns |
| T _{PHFD_XAZU3} | | Hold | | N/A | N/A | -0.36 | N/A | -1.03 | ns |
| T _{PSFD_XAZU4} | | Setup | XAZU4 | N/A | N/A | 2.39 | N/A | 3.81 | ns |
| T _{PHFD_XAZU4} | | Hold | | N/A | N/A | -0.37 | N/A | -1.05 | ns |
| T _{PSFD_XAZU5} | | Setup | XAZU5 | N/A | N/A | 2.39 | N/A | 3.81 | ns |
| T _{PHFD_XAZU5} | | Hold | | N/A | N/A | -0.37 | N/A | -1.05 | ns |

Table 91: Global Clock Input Setup and Hold With 3.3V HD I/O Without MMCM (cont'd)

| Symbol | Description | Device | Speed Grade and V _{CCINT} Operating Voltages | | | | | Units | |
|--------------------------|---|--------|---|-------|-------|-------|-----|-------|----|
| | | | 0.90V | 0.85V | | 0.72V | | | |
| | | | -3 | -2 | -1 | -2 | -1 | | |
| T _{PSFD_XAZU7} | Global clock input and input flip-flop (or latch) <i>without</i> MMCM | Setup | XAZU7 | N/A | N/A | 2.42 | N/A | N/A | ns |
| T _{PHFD_XAZU7} | | Hold | | N/A | N/A | -0.40 | N/A | N/A | ns |
| T _{PSFD_XAZU11} | | Setup | XAZU11 | N/A | N/A | 2.38 | N/A | N/A | ns |
| T _{PHFD_XAZU11} | | Hold | | N/A | N/A | -0.38 | N/A | N/A | ns |
| T _{PSFD_XQZU3} | | Setup | XQZU3 | N/A | 2.27 | 2.37 | N/A | 3.82 | ns |
| T _{PHFD_XQZU3} | | Hold | | N/A | -0.36 | -0.36 | N/A | -1.03 | ns |
| T _{PSFD_XQZU5} | | Setup | XQZU5 | N/A | 2.30 | 2.39 | N/A | 3.81 | ns |
| T _{PHFD_XQZU5} | | Hold | | N/A | -0.37 | -0.37 | N/A | -1.05 | ns |
| T _{PSFD_XQZU7} | | Setup | XQZU7 | N/A | 2.32 | 2.42 | N/A | 3.87 | ns |
| T _{PHFD_XQZU7} | | Hold | | N/A | -0.40 | -0.40 | N/A | -1.10 | ns |
| T _{PSFD_XQZU9} | | Setup | XQZU9 | N/A | 1.79 | 1.86 | N/A | 3.06 | ns |
| T _{PHFD_XQZU9} | | Hold | | N/A | -0.05 | -0.05 | N/A | -0.60 | ns |
| T _{PSFD_XQZU11} | | Setup | XQZU11 | N/A | 2.28 | 2.38 | N/A | 3.79 | ns |
| T _{PHFD_XQZU11} | | Hold | | N/A | -0.38 | -0.38 | N/A | -1.05 | ns |
| T _{PSFD_XQZU15} | | Setup | XQZU15 | N/A | 1.79 | 1.85 | N/A | 3.05 | ns |
| T _{PHFD_XQZU15} | | Hold | | N/A | -0.04 | -0.04 | N/A | -0.60 | ns |
| T _{PSFD_XQZU19} | | Setup | XQZU19 | N/A | 2.29 | 2.38 | N/A | 3.83 | ns |
| T _{PHFD_XQZU19} | | Hold | | N/A | -0.38 | -0.38 | N/A | -1.08 | ns |

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, slowest temperature, and slowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, fastest temperature, and fastest voltage.
2. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net.
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 92: Global Clock Input Setup and Hold With MMCM

| Symbol | Description | Device | Speed Grade and V _{CCINT} Operating Voltages | | | | | Units | | |
|--|---|--------|---|-------|-------|-------|-------|-------|-------|----|
| | | | 0.90V | 0.85V | | 0.72V | | | | |
| | | | -3 | -2 | -1 | -2 | -1 | | | |
| Input Setup and Hold Time Relative to Global Clock Input Signal using SSTL15 Standard. ^{1, 2, 3} | | | | | | | | | | |
| T _{PSMMCMCC_ZU2} | Global clock input and input flip-flop (or latch) with MMCM | Setup | XCZU2 | N/A | 1.83 | 1.96 | 1.83 | 1.96 | ns | |
| T _{PHMMCMCC_ZU2} | | Hold | | | -0.19 | -0.19 | -0.24 | -0.24 | ns | |
| T _{PSMMCMCC_ZU3} | | Setup | XCZU3 | N/A | 1.83 | 1.96 | 1.83 | 1.96 | ns | |
| T _{PHMMCMCC_ZU3} | | Hold | | | -0.19 | -0.19 | -0.24 | -0.24 | ns | |
| T _{PSMMCMCC_ZU4} | | Setup | XCZU4 | | 1.82 | 1.82 | 1.94 | 1.82 | 1.94 | ns |
| T _{PHMMCMCC_ZU4} | | Hold | | | -0.16 | -0.16 | -0.16 | -0.25 | -0.25 | ns |
| T _{PSMMCMCC_ZU5} | | Setup | XCZU5 | | 1.82 | 1.82 | 1.94 | 1.82 | 1.94 | ns |
| T _{PHMMCMCC_ZU5} | | Hold | | | -0.16 | -0.16 | -0.16 | -0.25 | -0.25 | ns |
| T _{PSMMCMCC_ZU6} | | Setup | XCZU6 | | 2.00 | 2.00 | 2.12 | 2.00 | 2.12 | ns |
| T _{PHMMCMCC_ZU6} | | Hold | | | -0.11 | -0.11 | -0.11 | -0.18 | -0.18 | ns |
| T _{PSMMCMCC_ZU7} | | Setup | XCZU7 | | 1.89 | 1.91 | 2.02 | 1.91 | 2.02 | ns |
| T _{PHMMCMCC_ZU7} | | Hold | | | -0.14 | -0.14 | -0.14 | -0.18 | -0.18 | ns |
| T _{PSMMCMCC_ZU9} | | Setup | XCZU9 | | 2.00 | 2.00 | 2.12 | 2.00 | 2.12 | ns |
| T _{PHMMCMCC_ZU9} | | Hold | | | -0.11 | -0.11 | -0.11 | -0.18 | -0.18 | ns |
| T _{PSMMCMCC_ZU11} | | Setup | XCZU11 | | 1.89 | 1.89 | 2.02 | 1.89 | 2.02 | ns |
| T _{PHMMCMCC_ZU11} | | Hold | | | -0.20 | -0.20 | -0.20 | -0.25 | -0.25 | ns |
| T _{PSMMCMCC_ZU15} | | Setup | XCZU15 | | 1.99 | 1.99 | 2.12 | 1.99 | 2.12 | ns |
| T _{PHMMCMCC_ZU15} | | Hold | | | -0.10 | -0.10 | -0.10 | -0.16 | -0.16 | ns |
| T _{PSMMCMCC_ZU17} | | Setup | XCZU17 | | 1.89 | 1.89 | 2.03 | 1.89 | 2.03 | ns |
| T _{PHMMCMCC_ZU17} | | Hold | | | -0.16 | -0.16 | -0.16 | -0.23 | -0.23 | ns |
| T _{PSMMCMCC_ZU19} | | Setup | XCZU19 | | 1.89 | 1.89 | 2.03 | 1.89 | 2.03 | ns |
| T _{PHMMCMCC_ZU19} | | Hold | | | -0.16 | -0.16 | -0.16 | -0.23 | -0.23 | ns |
| T _{PSMMCMCC_XAZU2} | | Setup | XAZU2 | | N/A | N/A | 1.96 | N/A | 1.96 | ns |
| T _{PHMMCMCC_XAZU2} | | Hold | | | N/A | N/A | -0.19 | N/A | -0.24 | ns |
| T _{PSMMCMCC_XAZU3} | | Setup | XAZU3 | | N/A | N/A | 1.96 | N/A | 1.96 | ns |
| T _{PHMMCMCC_XAZU3} | | Hold | | | N/A | N/A | -0.19 | N/A | -0.24 | ns |
| T _{PSMMCMCC_XAZU4} | | Setup | XAZU4 | | N/A | N/A | 1.94 | N/A | 1.94 | ns |
| T _{PHMMCMCC_XAZU4} | | Hold | | | N/A | N/A | -0.16 | N/A | -0.25 | ns |
| T _{PSMMCMCC_XAZU5} | | Setup | XAZU5 | | N/A | N/A | 1.94 | N/A | 1.94 | ns |
| T _{PHMMCMCC_XAZU5} | | Hold | | | N/A | N/A | -0.16 | N/A | -0.25 | ns |

Table 92: Global Clock Input Setup and Hold With MMCM (cont'd)

| Symbol | Description | Device | Speed Grade and V _{CCINT} Operating Voltages | | | | | Units | |
|------------------------------|---|--------|---|-------|-------|-------|-----|-------|----|
| | | | 0.90V | 0.85V | | 0.72V | | | |
| | | | -3 | -2 | -1 | -2 | -1 | | |
| T _{PSMMCMCC_XAZU7} | Global clock input and input flip-flop (or latch) with MMCM | Setup | XAZU7 | N/A | N/A | 2.02 | N/A | N/A | ns |
| T _{PHMMCMCC_XAZU7} | | Hold | | N/A | N/A | -0.14 | N/A | N/A | ns |
| T _{PSMMCMCC_XAZU11} | | Setup | XAZU11 | N/A | N/A | 2.02 | N/A | N/A | ns |
| T _{PHMMCMCC_XAZU11} | | Hold | | N/A | N/A | -0.20 | N/A | N/A | ns |
| T _{PSMMCMCC_XQZU3} | | Setup | XQZU3 | N/A | 1.83 | 1.96 | N/A | 1.96 | ns |
| T _{PHMMCMCC_XQZU3} | | Hold | | N/A | -0.19 | -0.19 | N/A | -0.24 | ns |
| T _{PSMMCMCC_XQZU5} | | Setup | XQZU5 | N/A | 1.82 | 1.94 | N/A | 1.94 | ns |
| T _{PHMMCMCC_XQZU5} | | Hold | | N/A | -0.16 | -0.16 | N/A | -0.25 | ns |
| T _{PSMMCMCC_XQZU7} | | Setup | XQZU7 | N/A | 1.91 | 2.02 | N/A | 2.02 | ns |
| T _{PHMMCMCC_XQZU7} | | Hold | | N/A | -0.14 | -0.14 | N/A | -0.18 | ns |
| T _{PSMMCMCC_XQZU9} | | Setup | XQZU9 | N/A | 2.00 | 2.12 | N/A | 2.12 | ns |
| T _{PHMMCMCC_XQZU9} | | Hold | | N/A | -0.11 | -0.11 | N/A | -0.18 | ns |
| T _{PSMMCMCC_XQZU11} | | Setup | XQZU11 | N/A | 1.89 | 2.02 | N/A | 2.02 | ns |
| T _{PHMMCMCC_XQZU11} | | Hold | | -0.20 | -0.20 | -0.20 | N/A | -0.25 | ns |
| T _{PSMMCMCC_XQZU15} | | Setup | XQZU15 | N/A | 1.99 | 2.12 | N/A | 2.12 | ns |
| T _{PHMMCMCC_XQZU15} | | Hold | | N/A | -0.10 | -0.10 | N/A | -0.16 | ns |
| T _{PSMMCMCC_XQZU19} | | Setup | XQZU19 | N/A | 1.89 | 2.03 | N/A | 2.03 | ns |
| T _{PHMMCMCC_XQZU19} | | Hold | | N/A | -0.16 | -0.16 | N/A | -0.23 | ns |

Notes:

- Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, slowest temperature, and slowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, fastest temperature, and fastest voltage.
- This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net.
- Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 93: Sampling Window

| Description | Speed Grade and V _{CCINT} Operating Voltages | | | | | Units |
|--|---|-------|-----|-------|-----|-------|
| | 0.90V | 0.85V | | 0.72V | | |
| | -3 | -2 | -1 | -2 | -1 | |
| T _{SAMP_BUFG} ¹ | 510 | 610 | 610 | 610 | 610 | ps |
| T _{SAMP_NATIVE_DPA} ² | 100 | 100 | 125 | 125 | 150 | ps |
| T _{SAMP_NATIVE_BISC} ³ | 60 | 60 | 85 | 85 | 110 | ps |

Notes:

- This parameter indicates the total sampling error of the Zynq UltraScale+ MPSoC DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include: CLK0 MMCM jitter, MMCM accuracy (phase offset), and MMCM phase shift resolution. These measurements do not include package or clock tree skew.
- This parameter is the receive sampling error for RX_BITSLICE when using dynamic phase alignment.
- This parameter is the receive sampling error for RX_BITSLICE when using built-in self-calibration (BISC).

Table 94: Input Logic Characteristics for Dynamic Phase Aligned Applications (Component Mode)

| Description | Speed Grade and V _{CCINT} Operating Voltages | | | | | Units |
|---|---|-------|----|-------|----|-------|
| | 0.90V | 0.85V | | 0.72V | | |
| | -3 | -2 | -1 | -2 | -1 | |
| T _{INPUT_LOGIC_UNCERTAINTY} ¹ | 40 | | | | | ps |
| T _{CAL_ERROR} ² | 24 | | | | | ps |

Notes:

1. Input_logic_uncertainty accounts for the setup/hold and any pattern dependent jitter for the input logic (input register, IDDRE1, or ISERDESE3).
2. Calibration error associated with quantization effects based on the IDELAY resolution. Calibration must be performed for each input pin to ensure optimal performance.

Package Parameter Guidelines

The parameters in this section provide the necessary values for calculating timing budgets for clock transmitter and receiver data-valid windows.

Table 95: Package Skew

| Symbol | Description | Device | Package | Value | Units |
|----------|------------------------------|--------|----------|-------|-------|
| PKGSKEW | Package Skew ^{1, 2} | XCZU2 | SBVA484 | 105 | ps |
| | | | SFVA625 | 108 | ps |
| | | | SFVC784 | 93 | ps |
| | | XCZU3 | SBVA484 | 105 | ps |
| | | | SFVA625 | 108 | ps |
| | | | SFVC784 | 93 | ps |
| | | XCZU4 | SFVC784 | 133 | ps |
| | | | FBVB900 | 159 | ps |
| | | XCZU5 | SFVC784 | 133 | ps |
| | | | FBVB900 | 159 | ps |
| | | XCZU6 | FFVC900 | 119 | ps |
| | | | FFVB1156 | 134 | ps |
| | | XCZU7 | FBVB900 | 141 | ps |
| | | | FFVC1156 | 175 | ps |
| | | | FFVF1517 | 305 | ps |
| | | XCZU9 | FFVC900 | 119 | ps |
| | | | FFVB1156 | 134 | ps |
| | | XCZU11 | FFVC1156 | 170 | ps |
| | | | FFVB1517 | 176 | ps |
| | | | FFVF1517 | 186 | ps |
| | | | FFVC1760 | 215 | ps |
| | | XCZU15 | FFVC900 | 118 | ps |
| | | | FFVB1156 | 132 | ps |
| | | XCZU17 | FFVB1517 | 221 | ps |
| | | | FFVC1760 | 226 | ps |
| | | | FFVD1760 | 178 | ps |
| | | | FFVE1924 | 174 | ps |
| | | XCZU19 | FFVB1517 | 221 | ps |
| FFVC1760 | 226 | | ps | | |
| FFVD1760 | 178 | | ps | | |
| FFVE1924 | 174 | | ps | | |

Table 95: Package Skew (cont'd)

| Symbol | Description | Device | Package | Value | Units |
|----------|------------------------------|----------|----------|-------|-------|
| PKGSKEW | Package Skew ^{1, 2} | XAZU2EG | SBVA484 | 105 | ps |
| | | | SFVA625 | 108 | ps |
| | | | SFVC784 | 93 | ps |
| | | XAZU3EG | SBVA484 | 105 | ps |
| | | | SFVA625 | 108 | ps |
| | | | SFVC784 | 93 | ps |
| | | XAZU4EV | SFVC784 | 133 | ps |
| | | XAZU5EV | SFVC784 | 133 | ps |
| | | XAZU7EV | FBVB900 | 141 | ps |
| | | XAZU11EG | FFVF1517 | 186 | ps |
| | | XQZU3EG | SFRA484 | 106 | ps |
| | | | SFRC784 | 93 | ps |
| | | XQZU5EV | SFRC784 | 133 | ps |
| | | | FFRB900 | 155 | ps |
| | | XQZU7EV | FFRB900 | 141 | ps |
| | | | FFRC1156 | 176 | ps |
| | | XQZU9EG | FFRC900 | 119 | ps |
| | | | FFRB1156 | 135 | ps |
| | | XQZU11EG | FFRC1156 | 170 | ps |
| | | | FFRC1760 | 214 | ps |
| | | XQZU15EG | FFRC900 | 119 | ps |
| FFRB1156 | 127 | | ps | | |
| XQZU19EG | FFRB1517 | 211 | ps | | |
| | FFRC1760 | 228 | ps | | |

Notes:

1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from die pad to ball.
2. Package delay information is available for these device/package combinations. This information can be used to deskew the package.

GTH Transceiver Specifications

The *UltraScale Architecture and Product Data Sheet: Overview (DS890)* lists the Zynq UltraScale+ MPSoCs that include the GTH transceivers.

GTH Transceiver DC Input and Output Levels

The following table summarizes the DC specifications of the GTH transceivers in Zynq UltraScale+ MPSoCs. Consult the *UltraScale Architecture GTH Transceivers User Guide (UG576)* for further details.

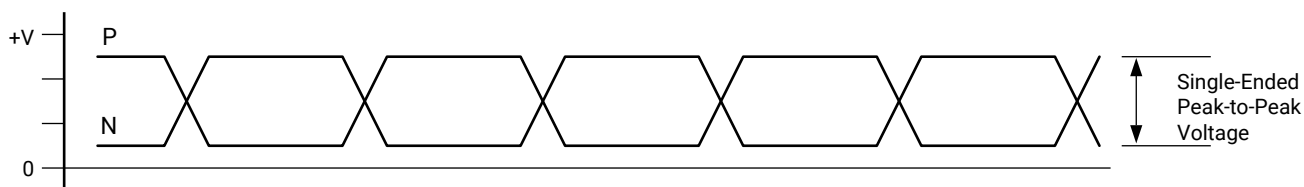
Table 96: GTH Transceiver DC Specifications

| Symbol | DC Parameter | Conditions | Min | Typ | Max | Units |
|----------------------|---|---|--|--------------------------|----------------------|-------|
| DV _{PPIN} | Differential peak-to-peak input voltage (external AC coupled) | >10.3125 Gb/s | 150 | - | 1250 | mV |
| | | 6.6 Gb/s to 10.3125 Gb/s | 150 | - | 1250 | mV |
| | | ≤ 6.6 Gb/s | 150 | - | 2000 | mV |
| V _{IN} | Single-ended input voltage. Voltage measured at the pin referenced to GND | DC coupled V _{MGTAVTT} = 1.2V | -400 | - | V _{MGTAVTT} | mV |
| V _{CMIN} | Common mode input voltage | DC coupled V _{MGTAVTT} = 1.2V | - | 2/3 V _{MGTAVTT} | - | mV |
| DV _{PPOUT} | Differential peak-to-peak output voltage ¹ | Transmitter output swing is set to 11111 | 800 | - | - | mV |
| V _{CMOUTDC} | Common mode output voltage: DC coupled (equation based) | When remote RX is terminated to GND | $V_{MGTAVTT}/2 - D_{VPPOUT}/4$ | | | mV |
| | | When remote RX termination is floating | $V_{MGTAVTT} - D_{VPPOUT}/2$ | | | mV |
| | | When remote RX is terminated to V _{RX_TERM} ² | $V_{MGTAVTT} - \frac{D_{VPPOUT}}{4} - \left(\frac{V_{MGTAVTT} - V_{RX_TERM}}{2} \right)$ | | | mV |
| V _{CMOUTAC} | Common mode output voltage: AC coupled (equation based) | | $V_{MGTAVTT} - D_{VPPOUT}/2$ | | | mV |
| R _{IN} | Differential input resistance | | - | 100 | - | Ω |
| R _{OUT} | Differential output resistance | | - | 100 | - | Ω |
| T _{OSKEW} | Transmitter output pair (TXP and TXN) intra-pair skew (all packages) | | - | - | 10 | ps |
| C _{EXT} | Recommended external AC coupling capacitor ³ | | - | 100 | - | nF |

Notes:

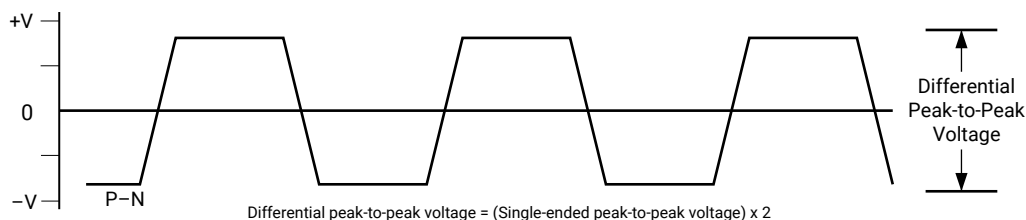
- The output swing and pre-emphasis levels are programmable using the attributes discussed in the *UltraScale Architecture GTH Transceivers User Guide (UG576)*, and can result in values lower than reported in this table.
- V_{RX_TERM} is the remote RX termination voltage.
- Other values can be used as appropriate to conform to specific protocols and standards.

Figure 3: Single-Ended Peak-to-Peak Voltage



X16653-072117

Figure 4: Differential Peak-to-Peak Voltage



X16639-072117

Table 97 and Table 98 summarize the DC specifications of the GTH transceivers input and output clocks in Zynq UltraScale+ MPSoCs. Consult the *UltraScale Architecture GTH Transceivers User Guide* (UG576) for further details.

Table 97: GTH Transceiver Clock Input Level Specification

| Symbol | DC Parameter | Min | Typ | Max | Units |
|--------------------|---|-----|-----|------|-------|
| V _{IDIFF} | Differential peak-to-peak input voltage | 250 | - | 2000 | mV |
| R _{IN} | Differential input resistance | - | 100 | - | Ω |
| C _{EXT} | Required external AC coupling capacitor | - | 10 | - | nF |

Table 98: GTH Transceiver Clock Output Level Specification

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|--------------------|---|--|-----|-----|-----|-------|
| V _{OL} | Output Low voltage for P and N | R _T = 100Ω across P and N signals | 100 | - | 330 | mV |
| V _{OH} | Output High voltage for P and N | R _T = 100Ω across P and N signals | 500 | - | 700 | mV |
| V _{DDOUT} | Differential output voltage (P-N), P = High (N-P), N = High | R _T = 100Ω across P and N signals | 300 | - | 430 | mV |
| V _{CMOUT} | Common mode voltage | R _T = 100Ω across P and N signals | 300 | - | 500 | mV |

GTH Transceiver Switching Characteristics

Consult the *UltraScale Architecture GTH Transceivers User Guide* (UG576) for further information.

Table 99: GTH Transceiver Performance

| Symbol | Description | Output Divider | Speed Grade and V _{CCINT} Operating Voltages | | | | | | | | | | Units |
|-------------------------|------------------------------------|----------------|---|--------|---------------------|--------|--------|--------|--------|--------|--------|---------|-------|
| | | | 0.90V | | 0.85V | | | | 0.72V | | | | |
| | | | -3 | -2 | -1 | -2 | -1 | -2 | -1 | | | | |
| F _{GTHMAX} | GTH maximum line rate | | 16.375 ¹ | | 16.375 ¹ | | | | 12.5 | | | | Gb/s |
| F _{GTHMIN} | GTH minimum line rate | | 0.5 | | 0.5 | | | | 0.5 | | | | Gb/s |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| F _{GTHCRANGE} | CPLL line rate range ² | 1 | 4 | 12.5 | 4 | 12.5 | 4 | 8.5 | 4 | 8.5 | 4 | 8.5 | Gb/s |
| | | 2 | 2 | 6.25 | 2 | 6.25 | 2 | 4.25 | 2 | 4.25 | 2 | 4.25 | Gb/s |
| | | 4 | 1 | 3.125 | 1 | 3.125 | 1 | 2.125 | 1 | 2.125 | 1 | 2.125 | Gb/s |
| | | 8 | 0.5 | 1.5625 | 0.5 | 1.5625 | 0.5 | 1.0625 | 0.5 | 1.0625 | 0.5 | 1.0625 | Gb/s |
| | | 16 | N/A | | | | | | | | | | Gb/s |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| F _{GTHQRANGE1} | QPLL0 line rate range ³ | 1 | 9.8 | 16.375 | 9.8 | 16.375 | 9.8 | 12.5 | 9.8 | 12.5 | 9.8 | 10.3125 | Gb/s |
| | | 2 | 4.9 | 8.1875 | 4.9 | 8.1875 | 4.9 | 8.15 | 4.9 | 8.1875 | 4.9 | 8.15 | Gb/s |
| | | 4 | 2.45 | 4.0938 | 2.45 | 4.0938 | 2.45 | 4.075 | 2.45 | 4.0938 | 2.45 | 4.075 | Gb/s |
| | | 8 | 1.225 | 2.0469 | 1.225 | 2.0469 | 1.225 | 2.0375 | 1.225 | 2.0469 | 1.225 | 2.0375 | Gb/s |
| | | 16 | 0.6125 | 1.0234 | 0.6125 | 1.0234 | 0.6125 | 1.0188 | 0.6125 | 1.0234 | 0.6125 | 1.0188 | Gb/s |

Table 99: GTH Transceiver Performance (cont'd)

| Symbol | Description | Output Divider | Speed Grade and V _{CCINT} Operating Voltages | | | | | | | | | | Units |
|--------------------------|------------------------------------|----------------|---|--------|--------|--------|--------|--------|--------|--------|--------|---------|-------|
| | | | 0.90V | | 0.85V | | | | 0.72V | | | | |
| | | | -3 | | -2 | | -1 | | -2 | | -1 | | |
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | | |
| F _{GTHQRANGE2} | QPLL1 line rate range ⁴ | 1 | 8.0 | 13.0 | 8.0 | 13.0 | 8.0 | 12.5 | 8.0 | 12.5 | 8.0 | 10.3125 | Gb/s |
| | | 2 | 4.0 | 6.5 | 4.0 | 6.5 | 4.0 | 6.5 | 4.0 | 6.5 | 4.0 | 6.5 | Gb/s |
| | | 4 | 2.0 | 3.25 | 2.0 | 3.25 | 2.0 | 3.25 | 2.0 | 3.25 | 2.0 | 3.25 | Gb/s |
| | | 8 | 1.0 | 1.625 | 1.0 | 1.625 | 1.0 | 1.625 | 1.0 | 1.625 | 1.0 | 1.625 | Gb/s |
| | | 16 | 0.5 | 0.8125 | 0.5 | 0.8125 | 0.5 | 0.8125 | 0.5 | 0.8125 | 0.5 | 0.8125 | Gb/s |
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | | |
| F _{CPLL} RANGE | CPLL frequency range | 2 | 6.25 | 2 | 6.25 | 2 | 4.25 | 2 | 4.25 | 2 | 4.25 | GHz | |
| F _{QPLL0} RANGE | QPLL0 frequency range | 9.8 | 16.375 | 9.8 | 16.375 | 9.8 | 16.375 | 9.8 | 16.375 | 9.8 | 16.375 | GHz | |
| F _{QPLL1} RANGE | QPLL1 frequency range | 8 | 13 | 8 | 13 | 8 | 13 | 8 | 13 | 8 | 13 | GHz | |

Notes:

1. GTH transceiver line rates in the SFVC784 and SFRC784 packages support data rates up to 12.5 Gb/s.
2. The values listed are the rounded results of the calculated equation $(2 \times \text{CPLL_Frequency}) / \text{Output_Divider}$.
3. The values listed are the rounded results of the calculated equation $(\text{QPLL0_Frequency}) / \text{Output_Divider}$.
4. The values listed are the rounded results of the calculated equation $(\text{QPLL1_Frequency}) / \text{Output_Divider}$.

Table 100: GTH Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics

| Symbol | Description | All Speed Grades | Units |
|------------------------|-----------------------------|------------------|-------|
| F _{GTHDRPCLK} | GTHDRPCLK maximum frequency | 250 | MHz |

Table 101: GTH Transceiver Reference Clock Switching Characteristics

| Symbol | Description | Conditions | All Speed Grades | | | Units |
|-------------------|---------------------------------|----------------------|------------------|-----|-----|-------|
| | | | Min | Typ | Max | |
| F _{GCLK} | Reference clock frequency range | | 60 | - | 820 | MHz |
| T _{RCLK} | Reference clock rise time | 20% - 80% | - | 200 | - | ps |
| T _{FCLK} | Reference clock fall time | 80% - 20% | - | 200 | - | ps |
| T _{DREF} | Reference clock duty cycle | Transceiver PLL only | 40 | 50 | 60 | % |

Table 102: GTH Transceiver Reference Clock Oscillator Selection Phase Noise Mask

| Symbol | Description | Offset Frequency | Min | Typ | Max | Units |
|--|---|------------------|-----|-----|------|--------|
| QPLL _{REFCLK} MASK ^{1,2} | QPLL0/QPLL1 reference clock select phase noise mask at REFCLK frequency = 312.5 MHz | 10 kHz | - | - | -105 | dBc/Hz |
| | | 100 kHz | - | - | -124 | |
| | | 1 MHz | - | - | -130 | |
| CPLL _{REFCLK} MASK ^{1,2} | CPLL reference clock select phase noise mask at REFCLK frequency = 312.5 MHz | 10 kHz | - | - | -105 | dBc/Hz |
| | | 100 kHz | - | - | -124 | |
| | | 1 MHz | - | - | -130 | |
| | | 50 MHz | - | - | -140 | |

Notes:

- For reference clock frequencies other than 312.5 MHz, adjust the phase-noise mask values by $20 \times \log(N/312.5)$ where N is the new reference clock frequency in MHz.
- This reference clock phase-noise mask is superseded by any reference clock phase-noise mask that is specified in a supported protocol, e.g., PCIe.

Table 103: GTH Transceiver PLL/Lock Time Adaptation

| Symbol | Description | Conditions | All Speed Grades | | | Units |
|--------------------|--|---|------------------|--------|-----------------------|-------|
| | | | Min | Typ | Max | |
| T _{LOCK} | Initial PLL lock | | - | - | 1 | ms |
| T _{DLOCK} | Clock recovery phase acquisition and adaptation time for decision feedback equalizer (DFE) | After the PLL is locked to the reference clock, this is the time it takes to lock the clock data recovery (CDR) to the data present at the input. | - | 50,000 | 37 x 10 ⁶ | UI |
| | Clock recovery phase acquisition and adaptation time for low-power mode (LPM) when the DFE is disabled | | - | 50,000 | 2.3 x 10 ⁶ | UI |

Table 104: GTH Transceiver User Clock Switching Characteristics

| Symbol | Description ¹ | Data Width Conditions (Bit) | | Speed Grade and V _{CCINT} Operating Voltages | | | | | Units |
|---------------------------|--|-----------------------------|--------------------|---|-------------------|-------------------|-----------------|-----------------|-------|
| | | Internal Logic | Interconnect Logic | 0.90V | 0.85V | | 0.72V | | |
| | | | | -3 ² | -2 ^{2,3} | -1 ^{4,5} | -2 ³ | -1 ⁵ | |
| F _{TXOUTPMA} | TXOUTCLK maximum frequency sourced from OUTCLKPMA | | | 511.719 | 511.719 | 390.625 | 390.625 | 322.266 | MHz |
| F _{RXOUTPMA} | RXOUTCLK maximum frequency sourced from OUTCLKPMA | | | 511.719 | 511.719 | 390.625 | 390.625 | 322.266 | MHz |
| F _{TXOUTPROGDIV} | TXOUTCLK maximum frequency sourced from TXPROGDIVCLK | | | 511.719 | 511.719 | 511.719 | 511.719 | 511.719 | MHz |
| F _{RXOUTPROGDIV} | RXOUTCLK maximum frequency sourced from RXPROGDIVCLK | | | 511.719 | 511.719 | 511.719 | 511.719 | 511.719 | MHz |
| F _{TXIN} | TXUSRCLK ⁶ maximum frequency | 16 | 16, 32 | 511.719 | 511.719 | 390.625 | 390.625 | 322.266 | MHz |
| | | 32 | 32, 64 | 511.719 | 511.719 | 390.625 | 390.625 | 322.266 | MHz |
| | | 20 | 20, 40 | 409.375 | 409.375 | 312.500 | 312.500 | 257.813 | MHz |
| | | 40 | 40, 80 | 409.375 | 409.375 | 312.500 | 312.500 | 257.813 | MHz |

Table 104: GTH Transceiver User Clock Switching Characteristics (cont'd)

| Symbol | Description ¹ | Data Width Conditions (Bit) | | Speed Grade and V _{CCINT} Operating Voltages | | | | | Units |
|--------------------|---|-----------------------------|--------------------|---|-------------------|-------------------|-----------------|-----------------|-------|
| | | | | 0.90V | 0.85V | | 0.72V | | |
| | | Internal Logic | Interconnect Logic | -3 ² | -2 ^{2,3} | -1 ^{4,5} | -2 ³ | -1 ⁵ | |
| F _{RXIN} | RXUSRCLK ⁶ maximum frequency | 16 | 16, 32 | 511.719 | 511.719 | 390.625 | 390.625 | 322.266 | MHz |
| | | 32 | 32, 64 | 511.719 | 511.719 | 390.625 | 390.625 | 322.266 | MHz |
| | | 20 | 20, 40 | 409.375 | 409.375 | 312.500 | 312.500 | 257.813 | MHz |
| | | 40 | 40, 80 | 409.375 | 409.375 | 312.500 | 312.500 | 257.813 | MHz |
| F _{TXIN2} | TXUSRCLK2 ⁶ maximum frequency | 16 | 16 | 511.719 | 511.719 | 390.625 | 390.625 | 322.266 | MHz |
| | | 16 | 32 | 255.859 | 255.859 | 195.313 | 195.313 | 161.133 | MHz |
| | | 32 | 32 | 511.719 | 511.719 | 390.625 | 390.625 | 322.266 | MHz |
| | | 32 | 64 | 255.859 | 255.859 | 195.313 | 195.313 | 161.133 | MHz |
| | | 20 | 20 | 409.375 | 409.375 | 312.500 | 312.500 | 257.813 | MHz |
| | | 20 | 40 | 204.688 | 204.688 | 156.250 | 156.250 | 128.906 | MHz |
| | | 40 | 40 | 409.375 | 409.375 | 312.500 | 312.500 | 257.813 | MHz |
| | | 40 | 80 | 204.688 | 204.688 | 156.250 | 156.250 | 128.906 | MHz |
| F _{RXIN2} | RXUSRCLK2 ⁶ maximum frequency | 16 | 16 | 511.719 | 511.719 | 390.625 | 390.625 | 322.266 | MHz |
| | | 16 | 32 | 255.859 | 255.859 | 195.313 | 195.313 | 161.133 | MHz |
| | | 32 | 32 | 511.719 | 511.719 | 390.625 | 390.625 | 322.266 | MHz |
| | | 32 | 64 | 255.859 | 255.859 | 195.313 | 195.313 | 161.133 | MHz |
| | | 20 | 20 | 409.375 | 409.375 | 312.500 | 312.500 | 257.813 | MHz |
| | | 20 | 40 | 204.688 | 204.688 | 156.250 | 156.250 | 128.906 | MHz |
| | | 40 | 40 | 409.375 | 409.375 | 312.500 | 312.500 | 257.813 | MHz |
| | | 40 | 80 | 204.688 | 204.688 | 156.250 | 156.250 | 128.906 | MHz |

Notes:

1. Clocking must be implemented as described in *UltraScale Architecture GTH Transceivers User Guide (UG576)*.
2. For speed grades -3E, -2E, and -2I, a 16-bit and 20-bit internal data path can only be used for line rates less than 8.1875 Gb/s.
3. For speed grade -2LE, a 16-bit and 20-bit internal data path can only be used for line rates less than 8.1875 Gb/s when V_{CCINT} = 0.85V or 6.25 Gb/s when V_{CCINT} = 0.72V.
4. For speed grades -1E, -1I, -1Q, and -1M, a 16-bit and 20-bit internal data path can only be used for line rates less than 6.25 Gb/s.
5. For speed grade -1LI, a 16-bit and 20-bit internal data path can only be used for line rates less than 6.25 Gb/s when V_{CCINT} = 0.85V or 5.15625 Gb/s when V_{CCINT} = 0.72V.
6. When the gearbox is used, these maximums refer to the XCLK. For more information, see the *UltraScale Architecture GTH Transceivers User Guide (UG576)*.

Table 105: GTH Transceiver Transmitter Switching Characteristics

| Symbol | Description | Condition | Min | Typ | Max | Units |
|----------------------|-------------------------------------|-------------|-------|-----|---------------------|-------|
| F _{GTHTX} | Serial data rate range | | 0.500 | - | F _{GTHMAX} | Gb/s |
| T _{RTX} | TX rise time | 20%–80% | - | 21 | - | ps |
| T _{FTX} | TX fall time | 80%–20% | - | 21 | - | ps |
| T _{LLSKEW} | TX lane-to-lane skew ¹ | | - | - | 500.00 | ps |
| T _{J16.375} | Total jitter ^{2,4} | 16.375 Gb/s | - | - | 0.28 | UI |
| D _{J16.375} | Deterministic jitter ^{2,4} | | - | - | 0.17 | UI |

Table 105: GTH Transceiver Transmitter Switching Characteristics (cont'd)

| Symbol | Description | Condition | Min | Typ | Max | Units |
|----------------------------|-------------------------------------|------------------------|-----|-----|------|-------|
| T _{J15.0} | Total jitter ^{2,4} | 15.0 Gb/s | - | - | 0.28 | UI |
| D _{J15.0} | Deterministic jitter ^{2,4} | | - | - | 0.17 | UI |
| T _{J14.1} | Total jitter ^{2,4} | 14.1 Gb/s | - | - | 0.28 | UI |
| D _{J14.1} | Deterministic jitter ^{2,4} | | - | - | 0.17 | UI |
| T _{J14.1} | Total jitter ^{2,4} | 14.025 Gb/s | - | - | 0.28 | UI |
| D _{J14.1} | Deterministic jitter ^{2,4} | | - | - | 0.17 | UI |
| T _{J13.1} | Total jitter ^{2,4} | 13.1 Gb/s | - | - | 0.28 | UI |
| D _{J13.1} | Deterministic jitter ^{2,4} | | - | - | 0.17 | UI |
| T _{J12.5_QPLL} | Total jitter ^{2,4} | 12.5 Gb/s | - | - | 0.28 | UI |
| D _{J12.5_QPLL} | Deterministic jitter ^{2,4} | | - | - | 0.17 | UI |
| T _{J12.5_CPLL} | Total jitter ^{3,4} | 12.5 Gb/s | - | - | 0.33 | UI |
| D _{J12.5_CPLL} | Deterministic jitter ^{3,4} | | - | - | 0.17 | UI |
| T _{J11.3_QPLL} | Total jitter ^{2,4} | 11.3 Gb/s | - | - | 0.28 | UI |
| D _{J11.3_QPLL} | Deterministic jitter ^{2,4} | | - | - | 0.17 | UI |
| T _{J10.3125_QPLL} | Total jitter ^{2,4} | 10.3125 Gb/s | - | - | 0.28 | UI |
| D _{J10.3125_QPLL} | Deterministic jitter ^{2,4} | | - | - | 0.17 | UI |
| T _{J10.3125_CPLL} | Total jitter ^{3,4} | 10.3125 Gb/s | - | - | 0.33 | UI |
| D _{J10.3125_CPLL} | Deterministic jitter ^{3,4} | | - | - | 0.17 | UI |
| T _{J9.953_QPLL} | Total jitter ^{2,4} | 9.953 Gb/s | - | - | 0.28 | UI |
| D _{J9.953_QPLL} | Deterministic jitter ^{2,4} | | - | - | 0.17 | UI |
| T _{J9.953_CPLL} | Total jitter ^{3,4} | 9.953 Gb/s | - | - | 0.33 | UI |
| D _{J9.953_CPLL} | Deterministic jitter ^{3,4} | | - | - | 0.17 | UI |
| T _{J8.0} | Total jitter ^{3,4} | 8.0 Gb/s | - | - | 0.32 | UI |
| D _{J8.0} | Deterministic jitter ^{3,4} | | - | - | 0.17 | UI |
| T _{J6.6} | Total jitter ^{3,4} | 6.6 Gb/s | - | - | 0.30 | UI |
| D _{J6.6} | Deterministic jitter ^{3,4} | | - | - | 0.15 | UI |
| T _{J5.0} | Total jitter ^{3,4} | 5.0 Gb/s | - | - | 0.30 | UI |
| D _{J5.0} | Deterministic jitter ^{3,4} | | - | - | 0.15 | UI |
| T _{J4.25} | Total jitter ^{3,4} | 4.25 Gb/s | - | - | 0.30 | UI |
| D _{J4.25} | Deterministic jitter ^{3,4} | | - | - | 0.15 | UI |
| T _{J4.0} | Total jitter ^{3,4} | 4.0 Gb/s | - | - | 0.32 | UI |
| D _{J4.0} | Deterministic jitter ^{3,4} | | - | - | 0.16 | UI |
| T _{J3.20} | Total jitter ^{3,4} | 3.20 Gb/s ⁵ | - | - | 0.20 | UI |
| D _{J3.20} | Deterministic jitter ^{3,4} | | - | - | 0.10 | UI |
| T _{J2.5} | Total jitter ^{3,4} | 2.5 Gb/s ⁶ | - | - | 0.20 | UI |
| D _{J2.5} | Deterministic jitter ^{3,4} | | - | - | 0.10 | UI |
| T _{J1.25} | Total jitter ^{3,4} | 1.25 Gb/s ⁷ | - | - | 0.15 | UI |
| D _{J1.25} | Deterministic jitter ^{3,4} | | - | - | 0.06 | UI |

Table 105: GTH Transceiver Transmitter Switching Characteristics (cont'd)

| Symbol | Description | Condition | Min | Typ | Max | Units |
|-------------------|--------------------------------------|-----------------------|-----|-----|------|-------|
| T _{J500} | Total jitter ^{3, 4} | 500 Mb/s ⁸ | - | - | 0.10 | UI |
| D _{J500} | Deterministic jitter ^{3, 4} | | - | - | 0.03 | UI |

Notes:

- Using same REFCLK input with TX phase alignment enabled for up to four consecutive transmitters (one fully populated GTH Quad) at the maximum line rate.
- Using QPLL_FBDIV = 40, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
- Using CPLL_FBDIV = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
- All jitter values are based on a bit-error ratio of 10⁻¹².
- CPLL frequency at 3.2 GHz and TXOUT_DIV = 2.
- CPLL frequency at 2.5 GHz and TXOUT_DIV = 2.
- CPLL frequency at 2.5 GHz and TXOUT_DIV = 4.
- CPLL frequency at 2.0 GHz and TXOUT_DIV = 8.

Table 106: GTH Transceiver Receiver Switching Characteristics

| Symbol | Description | Condition | Min | Typ | Max | Units |
|--|--|-------------------------------------|-------|-----|---------------------|-------|
| F _{GTHRX} | Serial data rate | | 0.500 | - | F _{GTHMAX} | Gb/s |
| R _{XSSST} | Receiver spread-spectrum tracking ¹ | Modulated at 33 kHz | -5000 | - | 0 | ppm |
| R _{XRLL} | Run length (CID) | | - | - | 256 | UI |
| R _{XPMTOL} | Data/REFCLK PPM offset tolerance | Bit rates ≤ 6.6 Gb/s | -1250 | - | 1250 | ppm |
| | | Bit rates > 6.6 Gb/s and ≤ 8.0 Gb/s | -700 | - | 700 | ppm |
| | | Bit rates > 8.0 Gb/s | -200 | - | 200 | ppm |
| SJ Jitter Tolerance² | | | | | | |
| J _{T_SJ16.375} | Sinusoidal jitter (QPLL) ³ | 16.375 Gb/s | 0.30 | - | - | UI |
| J _{T_SJ15.0} | Sinusoidal jitter (QPLL) ³ | 15.0 Gb/s | 0.30 | - | - | UI |
| J _{T_SJ14.1} | Sinusoidal jitter (QPLL) ³ | 14.1 Gb/s | 0.30 | - | - | UI |
| J _{T_SJ13.1} | Sinusoidal jitter (QPLL) ³ | 13.1 Gb/s | 0.30 | - | - | UI |
| J _{T_SJ12.5} | Sinusoidal jitter (QPLL) ³ | 12.5 Gb/s | 0.30 | - | - | UI |
| J _{T_SJ11.3} | Sinusoidal jitter (QPLL) ³ | 11.3 Gb/s | 0.30 | - | - | UI |
| J _{T_SJ10.32_QPLL} | Sinusoidal jitter (QPLL) ³ | 10.32 Gb/s | 0.30 | - | - | UI |
| J _{T_SJ10.32_CPLL} | Sinusoidal jitter (CPLL) ³ | 10.32 Gb/s | 0.30 | - | - | UI |
| J _{T_SJ9.953_QPLL} | Sinusoidal jitter (QPLL) ³ | 9.953 Gb/s | 0.30 | - | - | UI |
| J _{T_SJ9.953_CPLL} | Sinusoidal jitter (CPLL) ³ | 9.953 Gb/s | 0.30 | - | - | UI |
| J _{T_SJ8.0} | Sinusoidal jitter (QPLL) ³ | 8.0 Gb/s | 0.42 | - | - | UI |
| J _{T_SJ6.6_CPLL} | Sinusoidal jitter (CPLL) ³ | 6.6 Gb/s | 0.44 | - | - | UI |
| J _{T_SJ5.0} | Sinusoidal jitter (CPLL) ³ | 5.0 Gb/s | 0.44 | - | - | UI |
| J _{T_SJ4.25} | Sinusoidal jitter (CPLL) ³ | 4.25 Gb/s | 0.44 | - | - | UI |
| J _{T_SJ3.2} | Sinusoidal jitter (CPLL) ³ | 3.2 Gb/s ⁴ | 0.45 | - | - | UI |
| J _{T_SJ2.5} | Sinusoidal jitter (CPLL) ³ | 2.5 Gb/s ⁵ | 0.30 | - | - | UI |
| J _{T_SJ1.25} | Sinusoidal jitter (CPLL) ³ | 1.25 Gb/s ⁶ | 0.30 | - | - | UI |
| J _{T_SJ500} | Sinusoidal jitter (CPLL) ³ | 500 Mb/s ⁷ | 0.30 | - | - | UI |

Table 106: GTH Transceiver Receiver Switching Characteristics (cont'd)

| Symbol | Description | Condition | Min | Typ | Max | Units |
|--|--|-----------|------|-----|-----|-------|
| SJ Jitter Tolerance with Stressed Eye² | | | | | | |
| J _{T_TJSE3.2} | Total jitter with stressed eye ⁸ | 3.2 Gb/s | 0.70 | - | - | UI |
| J _{T_TJSE6.6} | | 6.6 Gb/s | 0.70 | - | - | UI |
| J _{T_SJSE3.2} | Sinusoidal jitter with stressed eye ⁸ | 3.2 Gb/s | 0.10 | - | - | UI |
| J _{T_SJSE6.6} | | 6.6 Gb/s | 0.10 | - | - | UI |

Notes:

- Using RXOUT_DIV = 1, 2, and 4.
- All jitter values are based on a bit error ratio of 10⁻¹².
- The frequency of the injected sinusoidal jitter is 80 MHz.
- CPLL frequency at 3.2 GHz and RXOUT_DIV = 2.
- CPLL frequency at 2.5 GHz and RXOUT_DIV = 2.
- CPLL frequency at 2.5 GHz and RXOUT_DIV = 4.
- CPLL frequency at 2.0 GHz and RXOUT_DIV = 8.
- Composite jitter with RX equalizer enabled. DFE disabled.

GTH Transceiver Electrical Compliance

The *UltraScale Architecture GTH Transceivers User Guide (UG576)* contains recommended use modes that ensure compliance for the protocols listed in the following table. The transceiver wizard provides the recommended settings for those use cases and for protocol specific characteristics.

Table 107: GTH Transceiver Protocol List

| Protocol | Specification | Serial Rate (Gb/s) | Electrical Compliance |
|-------------------------|----------------------------|--------------------|-----------------------|
| CAUI-10 | IEEE 802.3-2012 | 10.3125 | Compliant |
| nPPI | IEEE 802.3-2012 | 10.3125 | Compliant |
| 10GBASE-KR ¹ | IEEE 802.3-2012 | 10.3125 | Compliant |
| 40GBASE-KR | IEEE 802.3-2012 | 10.3125 | Compliant |
| SFP+ | SFF-8431 (SR and LR) | 9.95328–11.10 | Compliant |
| XFP | INF-8077i, revision 4.5 | 10.3125 | Compliant |
| RXAUI | CEI-6G-SR | 6.25 | Compliant |
| XAUI | IEEE 802.3-2012 | 3.125 | Compliant |
| 1000BASE-X | IEEE 802.3-2012 | 1.25 | Compliant |
| 5.0G Ethernet | IEEE 802.3bx (PAR) | 5 | Compliant |
| 2.5G Ethernet | IEEE 802.3bx (PAR) | 2.5 | Compliant |
| HiGig, HiGig+, HiGig2 | IEEE 802.3-2012 | 3.74, 6.6 | Compliant |
| OTU2 | ITU G.8251 | 10.709225 | Compliant |
| OTU4 (OTL4.10) | OIF-CEI-11G-SR | 11.180997 | Compliant |
| OC-3/12/48/192 | GR-253-CORE | 0.1555–9.956 | Compliant |
| TFI-5 | OIF-TFI5-0.1.0 | 2.488 | Compliant |
| Interlaken | OIF-CEI-6G, OIF-CEI-11G-SR | 4.25–12.5 | Compliant |
| PCIe Gen1, 2, 3 | PCI Express base 3.0 | 2.5, 5.0, and 8.0 | Compliant |
| SDI ² | SMPTE 424M-2006 | 0.27–2.97 | Compliant |

Table 107: GTH Transceiver Protocol List (cont'd)

| Protocol | Specification | Serial Rate (Gb/s) | Electrical Compliance |
|-------------------------------|--|--------------------|-----------------------|
| UHD-SDI ² | SMPTE ST-2081 6G, SMPTE ST-2082 12G | 6 and 12 | Compliant |
| Hybrid memory cube (HMC) | HMC-15G-SR | 10, 12.5, and 15.0 | Compliant |
| MoSys Bandwidth Engine | CEI-11-SR and CEI-11-SR (overclocked) | 10.3125, 15.5 | Compliant |
| CPRI | CPRI_v_6_1_2014-07-01 | 0.6144–12.165 | Compliant |
| HDMI ² | HDMI 2.0 | All | Compliant |
| Passive optical network (PON) | 10G-EPON, 1G-EPON, NG-PON2, XG-PON, and 2.5G-PON | 0.155–10.3125 | Compliant |
| JESD204a/b | OIF-CEI-6G, OIF-CEI-11G | 3.125–12.5 | Compliant |
| Serial RapidIO | RapidIO specification 3.1 | 1.25–10.3125 | Compliant |
| DisplayPort ² | DP 1.2B CTS | 1.62–5.4 | Compliant |
| Fibre channel | FC-PI-4 | 1.0625–14.025 | Compliant |
| SATA Gen1, 2, 3 | Serial ATA revision 3.0 specification | 1.5, 3.0, and 6.0 | Compliant |
| SAS Gen1, 2, 3 | T10/BSR INCITS 519 | 3.0, 6.0, and 12.0 | Compliant |
| SFI-5 | OIF-SFI5-01.0 | 0.625–12.5 | Compliant |
| Aurora | CEI-6G, CEI-11G-LR | up to 11.180997 | Compliant |

Notes:

1. The transition time of the transmitter is faster than the IEEE Std 802.3-2012 specification.
2. This protocol requires external circuitry to achieve compliance.

GTy Transceiver Specifications

The *UltraScale Architecture and Product Data Sheet: Overview (DS890)* lists the Zynq UltraScale+ MPSoCs that include the GTy transceivers.

GTy Transceiver DC Input and Output Levels

Table 108 summarizes the DC specifications of the GTy transceivers in Zynq UltraScale+ MPSoCs. Consult the *UltraScale Architecture GTy Transceivers User Guide (UG578)* for further details.

Table 108: GTy Transceiver DC Specifications

| Symbol | DC Parameter | Conditions | Min | Typ | Max | Units |
|---------------------|--|--|------|--------------------------|----------------------|-------|
| DV _{PPIN} | Differential peak-to-peak input voltage (external AC coupled) | >10.3125 Gb/s | 150 | – | 1250 | mV |
| | | 6.6 Gb/s to 10.3125 Gb/s | 150 | – | 1250 | mV |
| | | ≤ 6.6 Gb/s | 150 | – | 2000 | mV |
| V _{IN} | Single-ended input voltage. Voltage measured at the pin referenced to GND. | DC coupled V _{MGTAVTT} = 1.2V | –400 | – | V _{MGTAVTT} | mV |
| V _{CMIN} | Common mode input voltage | DC coupled V _{MGTAVTT} = 1.2V | – | 2/3 V _{MGTAVTT} | – | mV |
| DV _{PPOUT} | Differential peak-to-peak output voltage ¹ | Transmitter output swing is set to 11111 | 800 | – | – | mV |

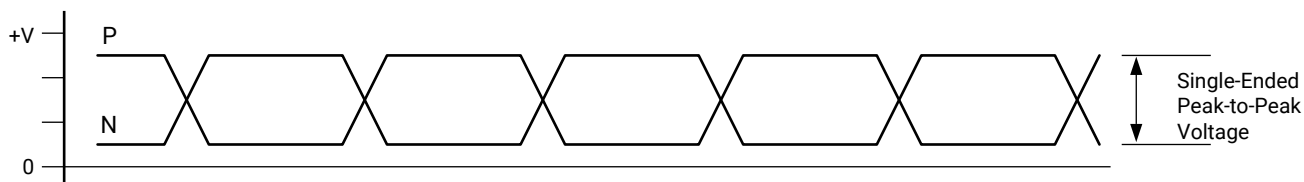
Table 108: GTY Transceiver DC Specifications (cont'd)

| Symbol | DC Parameter | Conditions | Min | Typ | Max | Units |
|----------------------|---|---|--|-----|-----|-------|
| V _{CMOUTDC} | Common mode output voltage: DC coupled (equation based) | When remote RX is terminated to GND | $V_{MGTAVTT}/2 - D_{VPPOUT}/4$ | | | mV |
| | | When remote RX termination is floating | $V_{MGTAVTT} - D_{VPPOUT}/2$ | | | mV |
| | | When remote RX is terminated to V _{RX_TERM} ² | $V_{MGTAVTT} - \frac{D_{VPPOUT}}{4} - \left(\frac{V_{MGTAVTT} - V_{RX_TERM}}{2} \right)$ | | | mV |
| V _{CMOUTAC} | Common mode output voltage: AC coupled | Equation based | $V_{MGTAVTT} - D_{VPPOUT}/2$ | | | mV |
| R _{IN} | Differential input resistance | | - | 100 | - | Ω |
| R _{OUT} | Differential output resistance | | - | 100 | - | Ω |
| T _{OSKEW} | Transmitter output pair (TXP and TXN) intra-pair skew | | - | - | 10 | ps |
| C _{EXT} | Recommended external AC coupling capacitor ³ | | - | 100 | - | nF |

Notes:

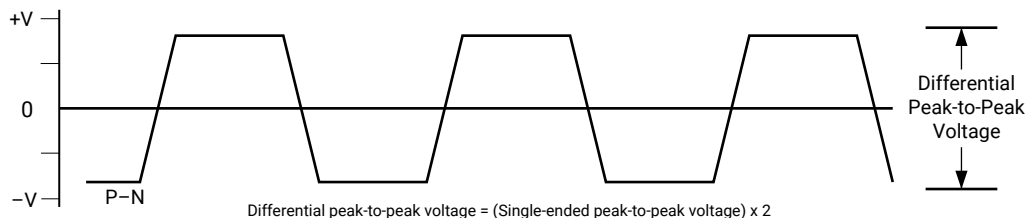
1. The output swing and pre-emphasis levels are programmable using the GTY transceiver attributes discussed in the *UltraScale Architecture GTY Transceivers User Guide (UG578)* and can result in values lower than reported in this table.
2. V_{RX_TERM} is the remote RX termination voltage.
3. Other values can be used as appropriate to conform to specific protocols and standards.

Figure 5: Single-Ended Peak-to-Peak Voltage



X16653-072117

Figure 6: Differential Peak-to-Peak Voltage



X16639-072117

The following tables summarize the DC specifications of the clock input/output levels of the GTY transceivers in Zynq UltraScale+ MPSoCs. Consult the *UltraScale Architecture GTY Transceivers User Guide (UG578)* for further details.

Table 109: GTY Transceiver Clock DC Input Level Specification

| Symbol | DC Parameter | Min | Typ | Max | Units |
|--------------------|---|-----|-----|------|-------|
| V _{IDIFF} | Differential peak-to-peak input voltage | 250 | - | 2000 | mV |
| R _{IN} | Differential input resistance | - | 100 | - | Ω |
| C _{EXT} | Required external AC coupling capacitor | - | 10 | - | nF |

Table 110: GTY Transceiver Clock Output Level Specification

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|--------------------|---|--|-----|-----|-----|-------|
| V _{OL} | Output Low voltage for P and N | R _T = 100Ω across P and N signals | 100 | - | 330 | mV |
| V _{OH} | Output High voltage for P and N | R _T = 100Ω across P and N signals | 500 | - | 700 | mV |
| V _{DDOUT} | Differential output voltage (P-N), P = High (N-P), N = High | R _T = 100Ω across P and N signals | 300 | - | 430 | mV |
| V _{CMOUT} | Common mode voltage | R _T = 100Ω across P and N signals | 300 | - | 500 | mV |

GTY Transceiver Switching Characteristics

Consult the *UltraScale Architecture GTY Transceivers User Guide (UG578)* for further information.

Table 111: GTY Transceiver Performance

| Symbol | Description | Output Divider | Speed Grade and V _{CCINT} Operating Voltages | | | | | | | | | | Units | | | | |
|------------------------|------------------------------------|----------------|---|--------|--------|--------|--------|--------|--------|--------|--------|--------|-------|-----|------|--|------|
| | | | 0.90V | | 0.85V | | | | 0.72V | | | | | | | | |
| | | | -3 | -2 | -1 | -2 | -1 | -2 | -1 | -2 | -1 | | | | | | |
| F _{GTMAX} | GTY maximum line rate | | 32.75 | | 28.21 | | | | 25.785 | | | | 28.21 | | 12.5 | | Gb/s |
| F _{GTMIN} | GTY minimum line rate | | 0.5 | | 0.5 | | | | 0.5 | | | | 0.5 | | 0.5 | | Gb/s |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | | | |
| F _{GTQRANGE} | CPLL line rate range ¹ | 1 | 4.0 | 12.5 | 4.0 | 12.5 | 4.0 | 8.5 | 4.0 | 12.5 | 4.0 | 8.5 | Gb/s | | | | |
| | | 2 | 2.0 | 6.25 | 2.0 | 6.25 | 2.0 | 4.25 | 2.0 | 6.25 | 2.0 | 4.25 | Gb/s | | | | |
| | | 4 | 1.0 | 3.125 | 1.0 | 3.125 | 1.0 | 2.125 | 1.0 | 3.125 | 1.0 | 2.125 | Gb/s | | | | |
| | | 8 | 0.5 | 1.5625 | 0.5 | 1.5625 | 0.5 | 1.0625 | 0.5 | 1.5625 | 0.5 | 1.0625 | Gb/s | | | | |
| | | 16 | N/A | | | | | | | | | | Gb/s | | | | |
| | | 32 | N/A | | | | | | | | | | Gb/s | | | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | | | | | |
| F _{GTQRANGE1} | QPLL0 line rate range ² | 1 | 19.6 | 32.75 | 19.6 | 28.21 | 19.6 | 25.785 | 19.6 | 28.21 | N/A | | Gb/s | | | | |
| | | 1 | 9.8 | 16.375 | 9.8 | 16.375 | 9.8 | 16.375 | 9.8 | 16.375 | 9.8 | 12.5 | Gb/s | | | | |
| | | 2 | 4.9 | 8.1875 | 4.9 | 8.1875 | 4.9 | 8.1875 | 4.9 | 8.1875 | 4.9 | 8.1875 | Gb/s | | | | |
| | | 4 | 2.45 | 4.0938 | 2.45 | 4.0938 | 2.45 | 4.0938 | 2.45 | 4.0938 | 2.45 | 4.0938 | Gb/s | | | | |
| | | 8 | 1.225 | 2.0469 | 1.225 | 2.0469 | 1.225 | 2.0469 | 1.225 | 2.0469 | 1.225 | 2.0469 | Gb/s | | | | |
| | | 16 | 0.6125 | 1.0234 | 0.6125 | 1.0234 | 0.6125 | 1.0234 | 0.6125 | 1.0234 | 0.6125 | 1.0234 | Gb/s | | | | |

Table 111: GTY Transceiver Performance (cont'd)

| Symbol | Description | Output Divider | Speed Grade and V _{CCINT} Operating Voltages | | | | | | | | | | Units |
|--------------------------|------------------------------------|----------------|---|--------|-------|--------|------|--------|-------|--------|-----|--------|-------|
| | | | 0.90V | | 0.85V | | | | 0.72V | | | | |
| | | | -3 | | -2 | | -1 | | -2 | | -1 | | |
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | | |
| F _{GTYQRANGE2} | QPLL1 line rate range ³ | 1 | 16.0 | 26.0 | 16.0 | 26.0 | 16.0 | 25.785 | 16.0 | 26.0 | N/A | | Gb/s |
| | | 1 | 8.0 | 13.0 | 8.0 | 13.0 | 8.0 | 12.5 | 8.0 | 13.0 | 8.0 | 12.5 | Gb/s |
| | | 2 | 4.0 | 6.5 | 4.0 | 6.5 | 4.0 | 6.5 | 4.0 | 6.5 | 4.0 | 6.5 | Gb/s |
| | | 4 | 2.0 | 3.25 | 2.0 | 3.25 | 2.0 | 3.25 | 2.0 | 3.25 | 2.0 | 3.25 | Gb/s |
| | | 8 | 1.0 | 1.625 | 1.0 | 1.625 | 1.0 | 1.625 | 1.0 | 1.625 | 1.0 | 1.625 | Gb/s |
| | | 16 | 0.5 | 0.8125 | 0.5 | 0.8125 | 0.5 | 0.8125 | 0.5 | 0.8125 | 0.5 | 0.8125 | Gb/s |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| F _{CPLL} RANGE | CPLL frequency range | | 2.0 | 6.25 | 2.0 | 6.25 | 2.0 | 4.25 | 2.0 | 6.25 | 2.0 | 4.25 | GHz |
| F _{QPLL0} RANGE | QPLL0 frequency range | | 9.8 | 16.375 | 9.8 | 16.375 | 9.8 | 16.375 | 9.8 | 16.375 | 9.8 | 16.375 | GHz |
| F _{QPLL1} RANGE | QPLL1 frequency range | | 8.0 | 13.0 | 8.0 | 13.0 | 8.0 | 13.0 | 8.0 | 13.0 | 8.0 | 13.0 | GHz |

Notes:

- The values listed are the rounded results of the calculated equation $(2 \times \text{CPLL_Frequency}) / \text{Output_Divider}$.
- The values listed are the rounded results of the calculated equation $(\text{QPLL0_Frequency} \times \text{RATE}) / \text{Output_Divider}$ where RATE is 1 when QPLL0_CLKOUT_RATE is set to HALF and 2 if QPLL0_CLKOUT_RATE is set to FULL.
- The values listed are the rounded results of the calculated equation $(\text{QPLL1_Frequency} \times \text{RATE}) / \text{Output_Divider}$ where RATE is 1 when QPLL1_CLKOUT_RATE is set to HALF and 2 if QPLL1_CLKOUT_RATE is set to FULL.

Table 112: GTY Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics

| Symbol | Description | All Speed Grades | Units |
|------------------------|-----------------------------|------------------|-------|
| F _{GTYDRPCLK} | GTYDRPCLK maximum frequency | 250 | MHz |

Table 113: GTY Transceiver Reference Clock Switching Characteristics

| Symbol | Description | Conditions | All Speed Grades | | | Units |
|--------------------|---------------------------------|----------------------|------------------|-----|-----|-------|
| | | | Min | Typ | Max | |
| F _{GCLK} | Reference clock frequency range | | 60 | - | 820 | MHz |
| T _{RCLK} | Reference clock rise time | 20% - 80% | - | 200 | - | ps |
| T _{FCLK} | Reference clock fall time | 80% - 20% | - | 200 | - | ps |
| T _{DCREP} | Reference clock duty cycle | Transceiver PLL only | 40 | 50 | 60 | % |

Table 114: GTY Transceiver Reference Clock Oscillator Selection Phase Noise Mask

| Symbol | Description ^{1, 2} | Offset Frequency | Min | Typ | Max | Units |
|-----------------------------|--|------------------|-----|-----|------|--------|
| QPLL _{REFCLK} MASK | QPLL0/QPLL1 reference clock select phase noise mask at REFCLK frequency = 156.25 MHz | 10 kHz | - | - | -112 | dBc/Hz |
| | | 100 kHz | - | - | -128 | |
| | | 1 MHz | - | - | -145 | |
| | QPLL0/QPLL1 reference clock select phase noise mask at REFCLK frequency = 312.5 MHz | 10 kHz | - | - | -103 | dBc/Hz |
| | | 100 kHz | - | - | -123 | |
| | | 1 MHz | - | - | -143 | |
| | QPLL0/QPLL1 reference clock select phase noise mask at REFCLK frequency = 625 MHz | 10 kHz | - | - | -98 | dBc/Hz |
| | | 100 kHz | - | - | -117 | |
| | | 1 MHz | - | - | -140 | |
| CPLL _{REFCLK} MASK | CPLL reference clock select phase noise mask at REFCLK frequency = 156.25 MHz | 10 kHz | - | - | -112 | dBc/Hz |
| | | 100 kHz | - | - | -128 | |
| | | 1 MHz | - | - | -145 | |
| | | 50 MHz | - | - | -145 | |
| | CPLL reference clock select phase noise mask at REFCLK frequency = 312.5 MHz | 10 kHz | - | - | -103 | dBc/Hz |
| | | 100 kHz | - | - | -123 | |
| | | 1 MHz | - | - | -143 | |
| | | 50 MHz | - | - | -145 | |
| | CPLL reference clock select phase noise mask at REFCLK frequency = 625 MHz | 10 kHz | - | - | -98 | dBc/Hz |
| | | 100 kHz | - | - | -117 | |
| | | 1 MHz | - | - | -140 | |
| | | 50 MHz | - | - | -144 | |

Notes:

- For reference clock frequencies not in this table, use the phase-noise mask for the nearest reference clock frequency.
- This reference clock phase-noise mask is superseded by any reference clock phase-noise mask that is specified in a supported protocol, e.g., PCIe.

Table 115: GTY Transceiver PLL/Lock Time Adaptation

| Symbol | Description | Conditions | All Speed Grades | | | Units |
|--------------------|--|---|------------------|--------|-----------------------|-------|
| | | | Min | Typ | Max | |
| T _{LOCK} | Initial PLL lock. | | - | - | 1 | ms |
| T _{DLOCK} | Clock recovery phase acquisition and adaptation time for decision feedback equalizer (DFE) | After the PLL is locked to the reference clock, this is the time it takes to lock the clock data recovery (CDR) to the data present at the input. | - | 50,000 | 37 x 10 ⁶ | UI |
| | Clock recovery phase acquisition and adaptation time for low-power mode (LPM) when the DFE is disabled | | - | 50,000 | 2.3 x 10 ⁶ | UI |

Table 116: GTY Transceiver User Clock Switching Characteristics

| Symbol | Description ¹ | Data Width Conditions (Bit) | | Speed Grade and V _{CCINT} Operating Voltages | | | | | Units |
|---------------------------|--|-----------------------------|--------------------|---|-------------------|---------------------|-----------------|-----------------|-------|
| | | | | 0.90V | 0.85V | | 0.72V | | |
| | | Internal Logic | Interconnect Logic | -3 ² | -2 ^{2,3} | -1 ^{4,5,6} | -2 ³ | -1 ⁵ | |
| F _{TXOUTPMA} | TXOUTCLK maximum frequency sourced from OUTCLKPMA | | | 511.719 | 511.719 | 402.891 | 402.832 | 322.266 | MHz |
| F _{RXOUTPMA} | RXOUTCLK maximum frequency sourced from OUTCLKPMA | | | 511.719 | 511.719 | 402.891 | 402.832 | 322.266 | MHz |
| F _{TXOUTPROGDIV} | TXOUTCLK maximum frequency sourced from TXPROGDIVCLK | | | 511.719 | 511.719 | 511.719 | 511.719 | 511.719 | MHz |
| F _{RXOUTPROGDIV} | RXOUTCLK maximum frequency sourced from RXPROGDIVCLK | | | 511.719 | 511.719 | 511.719 | 511.719 | 511.719 | MHz |
| F _{TXIN} | TXUSRCLK ⁷ maximum frequency | 16 | 16, 32 | 511.719 | 511.719 | 390.625 | 390.625 | 322.266 | MHz |
| | | 32 | 32, 64 | 511.719 | 511.719 | 390.625 | 390.625 | 322.266 | MHz |
| | | 64 | 64, 128 | 511.719 | 440.781 | 402.891 | 402.832 | 195.313 | MHz |
| | | 20 | 20, 40 | 409.375 | 409.375 | 312.500 | 312.500 | 257.813 | MHz |
| | | 40 | 40, 80 | 409.375 | 409.375 | 312.500 | 350.000 | 257.813 | MHz |
| | | 80 | 80, 160 | 409.375 | 352.625 | 322.313 | 352.625 | 156.250 | MHz |
| F _{RXIN} | RXUSRCLK ⁷ maximum frequency | 16 | 16, 32 | 511.719 | 511.719 | 390.625 | 390.625 | 322.266 | MHz |
| | | 32 | 32, 64 | 511.719 | 511.719 | 390.625 | 390.625 | 322.266 | MHz |
| | | 64 | 64, 128 | 511.719 | 440.781 | 402.891 | 402.832 | 195.313 | MHz |
| | | 20 | 20, 40 | 409.375 | 409.375 | 312.500 | 312.500 | 257.813 | MHz |
| | | 40 | 40, 80 | 409.375 | 409.375 | 312.500 | 350.000 | 257.813 | MHz |
| | | 80 | 80, 160 | 409.375 | 352.625 | 322.313 | 352.625 | 156.250 | MHz |
| F _{TXIN2} | TXUSRCLK ^{2,7} maximum frequency | 16 | 16 | 511.719 | 511.719 | 390.625 | 390.625 | 322.266 | MHz |
| | | 16 | 32 | 255.859 | 255.859 | 195.313 | 195.313 | 161.133 | MHz |
| | | 32 | 32 | 511.719 | 511.719 | 390.625 | 390.625 | 322.266 | MHz |
| | | 32 | 64 | 255.859 | 255.859 | 195.313 | 195.313 | 161.133 | MHz |
| | | 64 | 64 | 511.719 | 440.781 | 402.891 | 402.832 | 195.313 | MHz |
| | | 64 | 128 | 255.859 | 220.391 | 201.445 | 201.416 | 97.656 | MHz |
| | | 20 | 20 | 409.375 | 409.375 | 312.500 | 312.500 | 257.813 | MHz |
| | | 20 | 40 | 204.688 | 204.688 | 156.250 | 156.250 | 128.906 | MHz |
| | | 40 | 40 | 409.375 | 409.375 | 312.500 | 350.000 | 257.813 | MHz |
| | | 40 | 80 | 204.688 | 204.688 | 156.250 | 175.000 | 128.906 | MHz |
| | | 80 | 80 | 409.375 | 352.625 | 322.313 | 352.625 | 156.250 | MHz |
| | | 80 | 160 | 204.688 | 176.313 | 161.156 | 176.313 | 78.125 | MHz |

Table 116: GTY Transceiver User Clock Switching Characteristics (cont'd)

| Symbol | Description ¹ | Data Width Conditions (Bit) | | Speed Grade and V _{CCINT} Operating Voltages | | | | | Units |
|--------------------|--|-----------------------------|--------------------|---|-------------------|---------------------|-----------------|-----------------|-------|
| | | | | 0.90V | 0.85V | | 0.72V | | |
| | | Internal Logic | Interconnect Logic | -3 ² | -2 ^{2,3} | -1 ^{4,5,6} | -2 ³ | -1 ⁵ | |
| F _{RXIN2} | RXUSRCLK2 ⁷ maximum frequency | 16 | 16 | 511.719 | 511.719 | 390.625 | 390.625 | 322.266 | MHz |
| | | 16 | 32 | 255.859 | 255.859 | 195.313 | 195.313 | 161.133 | MHz |
| | | 32 | 32 | 511.719 | 511.719 | 390.625 | 390.625 | 322.266 | MHz |
| | | 32 | 64 | 255.859 | 255.859 | 195.313 | 195.313 | 161.133 | MHz |
| | | 64 | 64 | 511.719 | 440.781 | 402.891 | 402.832 | 195.313 | MHz |
| | | 64 | 128 | 255.859 | 220.391 | 201.445 | 201.416 | 97.656 | MHz |
| | | 20 | 20 | 409.375 | 409.375 | 312.500 | 312.500 | 257.813 | MHz |
| | | 20 | 40 | 204.688 | 204.688 | 156.250 | 156.250 | 128.906 | MHz |
| | | 40 | 40 | 409.375 | 409.375 | 312.500 | 350.000 | 257.813 | MHz |
| | | 40 | 80 | 204.688 | 204.688 | 156.250 | 175.000 | 128.906 | MHz |
| | | 80 | 80 | 409.375 | 352.625 | 322.313 | 352.625 | 156.250 | MHz |
| 80 | 160 | 204.688 | 176.313 | 161.156 | 176.313 | 78.125 | MHz | | |

Notes:

1. Clocking must be implemented as described in the *UltraScale Architecture GTY Transceivers User Guide (UG578)*.
2. For speed grades -3E, -2E, and -2I, a 16-bit and 20-bit internal data path can only be used for line rates less than 8.1875 Gb/s.
3. For speed grade -2LE, a 16-bit and 20-bit internal data path can only be used for line rates less than 8.1875 Gb/s when V_{CCINT} = 0.85V or 6.25 Gb/s when V_{CCINT} = 0.72V.
4. For speed grades -1E, -1I, -1Q, and -1M, a 16-bit and 20-bit internal data path can only be used for line rates less than 6.25 Gb/s.
5. For speed grade -1LI, a 16-bit and 20-bit internal data path can only be used for line rates less than 6.25 Gb/s when V_{CCINT} = 0.85V or 5.15625 Gb/s when V_{CCINT} = 0.72V.
6. For the speed grades -1E, -1I, -1Q, and -1M, only a 64- or 80-bit internal data path can be used for line rates above 12.5 Gb/s.
7. When the gearbox is used, these maximums refer to the XCLK. For more information, see the Valid Data Width Combinations for TX Asynchronous Gearbox table in the *UltraScale Architecture GTY Transceivers User Guide (UG578)*.

Table 117: GTY Transceiver Transmitter Switching Characteristics

| Symbol | Description | Condition | Min | Typ | Max | Units |
|----------------------|-------------------------------------|-------------|-------|-----|---------------------|-------|
| F _{GTYTX} | Serial data rate range | | 0.500 | - | F _{GTYMAX} | Gb/s |
| T _{RTX} | TX rise time | 20%–80% | - | 21 | - | ps |
| T _{FTX} | TX fall time | 80%–20% | - | 21 | - | ps |
| T _{LLSKEW} | TX lane-to-lane skew ¹ | | - | - | 500.00 | ps |
| T _{J32.75} | Total jitter ^{2,4} | 32.75 Gb/s | - | - | 0.35 | UI |
| D _{J32.75} | Deterministic jitter ^{2,4} | | - | - | 0.19 | UI |
| T _{J28.21} | Total jitter ^{2,4} | 28.21 Gb/s | - | - | 0.28 | UI |
| D _{J28.21} | Deterministic jitter ^{2,4} | | - | - | 0.17 | UI |
| T _{J16.375} | Total jitter ^{2,4} | 16.375 Gb/s | - | - | 0.28 | UI |
| D _{J16.375} | Deterministic jitter ^{2,4} | | - | - | 0.17 | UI |
| T _{J15.0} | Total jitter ^{2,4} | 15.0 Gb/s | - | - | 0.28 | UI |
| D _{J15.0} | Deterministic jitter ^{2,4} | | - | - | 0.17 | UI |

Table 117: GTY Transceiver Transmitter Switching Characteristics (cont'd)

| Symbol | Description | Condition | Min | Typ | Max | Units |
|----------------------------|-------------------------------------|------------------------|-----|-----|------|-------|
| T _{J14.1} | Total jitter ^{2,4} | 14.1 Gb/s | - | - | 0.28 | UI |
| D _{J14.1} | Deterministic jitter ^{2,4} | | - | - | 0.17 | UI |
| T _{J14.1} | Total jitter ^{2,4} | 14.025 Gb/s | - | - | 0.28 | UI |
| D _{J14.1} | Deterministic jitter ^{2,4} | | - | - | 0.17 | UI |
| T _{J13.1} | Total jitter ^{2,4} | 13.1 Gb/s | - | - | 0.28 | UI |
| D _{J13.1} | Deterministic jitter ^{2,4} | | - | - | 0.17 | UI |
| T _{J12.5_QPLL} | Total jitter ^{2,4} | 12.5 Gb/s | - | - | 0.28 | UI |
| D _{J12.5_QPLL} | Deterministic jitter ^{2,4} | | - | - | 0.17 | UI |
| T _{J12.5_CPLL} | Total jitter ^{3,4} | 12.5 Gb/s | - | - | 0.33 | UI |
| D _{J12.5_CPLL} | Deterministic jitter ^{3,4} | | - | - | 0.17 | UI |
| T _{J11.3_QPLL} | Total jitter ^{2,4} | 11.3 Gb/s | - | - | 0.28 | UI |
| D _{J11.3_QPLL} | Deterministic jitter ^{2,4} | | - | - | 0.17 | UI |
| T _{J10.3125_QPLL} | Total jitter ^{2,4} | 10.3125 Gb/s | - | - | 0.28 | UI |
| D _{J10.3125_QPLL} | Deterministic jitter ^{2,4} | | - | - | 0.17 | UI |
| T _{J10.3125_CPLL} | Total jitter ^{3,4} | 10.3125 Gb/s | - | - | 0.33 | UI |
| D _{J10.3125_CPLL} | Deterministic jitter ^{3,4} | | - | - | 0.17 | UI |
| T _{J9.953_QPLL} | Total jitter ^{2,4} | 9.953 Gb/s | - | - | 0.28 | UI |
| D _{J9.953_QPLL} | Deterministic jitter ^{2,4} | | - | - | 0.17 | UI |
| T _{J9.953_CPLL} | Total jitter ^{3,4} | 9.953 Gb/s | - | - | 0.33 | UI |
| D _{J9.953_CPLL} | Deterministic jitter ^{3,4} | | - | - | 0.17 | UI |
| T _{J8.0} | Total jitter ^{3,4} | 8.0 Gb/s | - | - | 0.32 | UI |
| D _{J8.0} | Deterministic jitter ^{3,4} | | - | - | 0.17 | UI |
| T _{J6.6} | Total jitter ^{3,4} | 6.6 Gb/s | - | - | 0.30 | UI |
| D _{J6.6} | Deterministic jitter ^{3,4} | | - | - | 0.15 | UI |
| T _{J5.0} | Total jitter ^{3,4} | 5.0 Gb/s | - | - | 0.30 | UI |
| D _{J5.0} | Deterministic jitter ^{3,4} | | - | - | 0.15 | UI |
| T _{J4.25} | Total jitter ^{3,4} | 4.25 Gb/s | - | - | 0.30 | UI |
| D _{J4.25} | Deterministic jitter ^{3,4} | | - | - | 0.15 | UI |
| T _{J3.20} | Total jitter ^{3,4} | 3.20 Gb/s ⁵ | - | - | 0.20 | UI |
| D _{J3.20} | Deterministic jitter ^{3,4} | | - | - | 0.10 | UI |
| T _{J2.5} | Total jitter ^{3,4} | 2.5 Gb/s ⁶ | - | - | 0.20 | UI |
| D _{J2.5} | Deterministic jitter ^{3,4} | | - | - | 0.10 | UI |
| T _{J1.25} | Total jitter ^{3,4} | 1.25 Gb/s ⁷ | - | - | 0.15 | UI |
| D _{J1.25} | Deterministic jitter ^{3,4} | | - | - | 0.06 | UI |

Table 117: GTY Transceiver Transmitter Switching Characteristics (cont'd)

| Symbol | Description | Condition | Min | Typ | Max | Units |
|-------------------|--------------------------------------|-----------------------|-----|-----|------|-------|
| T _{J500} | Total jitter ^{3, 4} | 500 Mb/s ⁸ | - | - | 0.10 | UI |
| D _{J500} | Deterministic jitter ^{3, 4} | | - | - | 0.03 | UI |

Notes:

- Using same REFCLK input with TX phase alignment enabled for up to four consecutive transmitters (one fully populated GTY Quad) at maximum line rate.
- Using QPLL_FBDIV = 40, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
- Using CPLL_FBDIV = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
- All jitter values are based on a bit-error ratio of 10⁻¹².
- CPLL frequency at 3.2 GHz and TXOUT_DIV = 2.
- CPLL frequency at 2.5 GHz and TXOUT_DIV = 2.
- CPLL frequency at 2.5 GHz and TXOUT_DIV = 4.
- CPLL frequency at 2.0 GHz and TXOUT_DIV = 8.

Table 118: GTY Transceiver Receiver Switching Characteristics

| Symbol | Description | Condition | Min | Typ | Max | Units |
|--|--|-------------------------------------|-------|-----|---------------------|-------|
| F _{GTYRX} | Serial data rate | | 0.500 | - | F _{GTYMAX} | Gb/s |
| R _{XSSST} | Receiver spread-spectrum tracking ¹ | Modulated at 33 kHz | -5000 | - | 0 | ppm |
| R _{XRLL} | Run length (CID) | | - | - | 256 | UI |
| R _{XPMTOL} | Data/REFCLK PPM offset tolerance | Bit rates ≤ 6.6 Gb/s | -1250 | - | 1250 | ppm |
| | | Bit rates > 6.6 Gb/s and ≤ 8.0 Gb/s | -700 | - | 700 | ppm |
| | | Bit rates > 8.0 Gb/s | -200 | - | 200 | ppm |
| SJ Jitter Tolerance² | | | | | | |
| J _{T_SJ32.75} | Sinusoidal jitter (QPLL) ³ | 32.75 Gb/s | 0.25 | - | - | UI |
| J _{T_SJ28.21} | Sinusoidal jitter (QPLL) ³ | 28.21 Gb/s | 0.30 | - | - | UI |
| J _{T_SJ16.375} | Sinusoidal jitter (QPLL) ³ | 16.375 Gb/s | 0.30 | - | - | UI |
| J _{T_SJ15.0} | Sinusoidal jitter (QPLL) ³ | 15.0 Gb/s | 0.30 | - | - | UI |
| J _{T_SJ14.1} | Sinusoidal jitter (QPLL) ³ | 14.1 Gb/s | 0.30 | - | - | UI |
| J _{T_SJ13.1} | Sinusoidal jitter (QPLL) ³ | 13.1 Gb/s | 0.30 | - | - | UI |
| J _{T_SJ12.5} | Sinusoidal jitter (QPLL) ³ | 12.5 Gb/s | 0.30 | - | - | UI |
| J _{T_SJ11.3} | Sinusoidal jitter (QPLL) ³ | 11.3 Gb/s | 0.30 | - | - | UI |
| J _{T_SJ10.32_QPLL} | Sinusoidal jitter (QPLL) ³ | 10.32 Gb/s | 0.30 | - | - | UI |
| J _{T_SJ10.32_CPLL} | Sinusoidal jitter (CPLL) ³ | 10.32 Gb/s | 0.30 | - | - | UI |
| J _{T_SJ9.953_QPLL} | Sinusoidal jitter (QPLL) ³ | 9.953 Gb/s | 0.30 | - | - | UI |
| J _{T_SJ9.953_CPLL} | Sinusoidal jitter (CPLL) ³ | 9.953 Gb/s | 0.30 | - | - | UI |
| J _{T_SJ8.0} | Sinusoidal jitter (CPLL) ³ | 8.0 Gb/s | 0.42 | - | - | UI |
| J _{T_SJ6.6} | Sinusoidal jitter (CPLL) ³ | 6.6 Gb/s | 0.44 | - | - | UI |
| J _{T_SJ5.0} | Sinusoidal jitter (CPLL) ³ | 5.0 Gb/s | 0.44 | - | - | UI |
| J _{T_SJ4.25} | Sinusoidal jitter (CPLL) ³ | 4.25 Gb/s | 0.44 | - | - | UI |
| J _{T_SJ3.2} | Sinusoidal jitter (CPLL) ³ | 3.2 Gb/s ⁴ | 0.45 | - | - | UI |
| J _{T_SJ2.5} | Sinusoidal jitter (CPLL) ³ | 2.5 Gb/s ⁵ | 0.30 | - | - | UI |
| J _{T_SJ1.25} | Sinusoidal jitter (CPLL) ³ | 1.25 Gb/s ⁶ | 0.30 | - | - | UI |
| J _{T_SJ500} | Sinusoidal jitter (CPLL) ³ | 500 Mb/s ⁷ | 0.30 | - | - | UI |

Table 118: GTY Transceiver Receiver Switching Characteristics (cont'd)

| Symbol | Description | Condition | Min | Typ | Max | Units |
|--|--|-----------|------|-----|-----|-------|
| SJ Jitter Tolerance with Stressed Eye² | | | | | | |
| J _{T_TJSE3.2} | Total jitter with stressed eye ⁸ | 3.2 Gb/s | 0.70 | - | - | UI |
| J _{T_TJSE6.6} | | 6.6 Gb/s | 0.70 | - | - | UI |
| J _{T_SJSE3.2} | Sinusoidal jitter with stressed eye ⁸ | 3.2 Gb/s | 0.10 | - | - | UI |
| J _{T_SJSE6.6} | | 6.6 Gb/s | 0.10 | - | - | UI |

Notes:

- Using RXOUT_DIV = 1, 2, and 4.
- All jitter values are based on a bit error ratio of 10⁻¹².
- The frequency of the injected sinusoidal jitter is 80 MHz.
- CPLL frequency at 3.2 GHz and RXOUT_DIV = 2.
- CPLL frequency at 2.5 GHz and RXOUT_DIV = 2.
- CPLL frequency at 2.5 GHz and RXOUT_DIV = 4.
- CPLL frequency at 2.0 GHz and RXOUT_DIV = 8.
- Composite jitter with RX equalizer enabled. DFE disabled.

GTY Transceiver Electrical Compliance

The *UltraScale Architecture GTY Transceivers User Guide (UG578)* contains recommended use modes that ensure compliance for the protocols listed in the following table. The transceiver wizard provides the recommended settings for those use cases and for protocol specific characteristics.

Table 119: GTY Transceiver Protocol List

| Protocol | Specification | Serial Rate (Gb/s) | Electrical Compliance |
|-------------------------|---|--------------------|------------------------|
| CAUI-4 | IEEE 802.3-2012 | 25.78125 | Compliant |
| 28 Gb/s backplane | CEI-25G-LR | 25-28.05 | Compliant |
| Interlaken | OIF-CEI-6G, OIF-CEI-11GSR, OIF-CEI-28G-MR | 4.25-25.78125 | Compliant |
| 100GBASE-KR4 | IEEE 802.3bj-2014, CEI-25G-LR | 25.78125 | Compliant ¹ |
| 100GBASE-CR4 | IEEE 802.3bj-2014, CEI-25G-LR | 25.78125 | Compliant ¹ |
| 50GBASE-KR4 | IEEE 802.3by-2014, CEI-25G-LR | 25.78125 | Compliant ¹ |
| 50GBASE-CR4 | IEEE 802.3by-2014, CEI-25G-LR | 25.78125 | Compliant ¹ |
| 25GBASE-KR4 | IEEE 802.3by-2014, CEI-25G-LR | 25.78125 | Compliant ¹ |
| 25GBASE-CR4 | IEEE 802.3by-2014, CEI-25G-LR | 25.78125 | Compliant ¹ |
| OTU4 (OTL4.4) CFP2 | OIF-CEI-28G-VSR | 27.952493-32.75 | Compliant |
| OTU4 (OTL4.4) CFP | OIF-CEI-11G-MR | 11.18-13.1 | Compliant |
| CAUI-10 | IEEE 802.3-2012 | 10.3125 | Compliant |
| nPPI | IEEE 802.3-2012 | 10.3125 | Compliant |
| 10GBASE-KR ² | IEEE 802.3-2012 | 10.3125 | Compliant |
| SFP+ | SFF-8431 (SR and LR) | 9.95328-11.10 | Compliant |
| XFP | INF-8077i, revision 4.5 | 10.3125 | Compliant |
| RXAUI | CEI-6G-SR | 6.25 | Compliant |
| XAUI | IEEE 802.3-2012 | 3.125 | Compliant |
| 1000BASE-X | IEEE 802.3-2012 | 1.25 | Compliant |

Table 119: GTY Transceiver Protocol List (cont'd)

| Protocol | Specification | Serial Rate (Gb/s) | Electrical Compliance |
|-------------------------------|--|--------------------|------------------------|
| 5.0G Ethernet | IEEE 802.3bx (PAR) | 5 | Compliant |
| 2.5G Ethernet | IEEE 802.3bx (PAR) | 2.5 | Compliant |
| HiGig, HiGig+, HiGig2 | IEEE 802.3-2012 | 3.74, 6.6 | Compliant |
| QSGMII | QSGMII v1.2 (Cisco System, ENG-46158) | 5 | Compliant |
| OTU2 | ITU G.8251 | 10.709225 | Compliant |
| OTU4 (OTL4.10) | OIF-CEI-11G-SR | 11.180997 | Compliant |
| OC-3/12/48/192 | GR-253-CORE | 0.1555–9.956 | Compliant |
| PCIe Gen1, 2, 3 | PCI Express base 3.0 | 2.5, 5.0, and 8.0 | Compliant |
| SDI ³ | SMPTE 424M-2006 | 0.27–2.97 | Compliant |
| UHD-SDI ³ | SMPTE ST-2081 6G, SMPTE ST-2082 12G | 6 and 12 | Compliant |
| Hybrid memory cube (HMC) | HMC-15G-SR | 10, 12.5, and 15.0 | Compliant |
| MoSys bandwidth engine | CEI-11-SR and CEI-11-SR (overclocked) | 10.3125, 15.5 | Compliant |
| CPRI | CPRI_v_6_1_2014-07-01 | 0.6144–12.165 | Compliant |
| Passive optical network (PON) | 10G-EPON, 1G-EPON, NG-PON2, XG-PON, and 2.5G-PON | 0.155–10.3125 | Compliant |
| JESD204a/b | OIF-CEI-6G, OIF-CEI-11G | 3.125–12.5 | Compliant |
| Serial RapidIO | RapidIO specification 3.1 | 1.25–10.3125 | Compliant |
| DisplayPort | DP 1.2B CTS | 1.62–5.4 | Compliant ³ |
| Fibre channel | FC-PI-4 | 1.0625–14.025 | Compliant |
| SATA Gen1, 2, 3 | Serial ATA revision 3.0 specification | 1.5, 3.0, and 6.0 | Compliant |
| SAS Gen1, 2, 3 | T10/BSR INCITS 519 | 3.0, 6.0, and 12.0 | Compliant |
| SFI-5 | OIF-SFI5-01.0 | 0.625 - 12.5 | Compliant |
| Aurora | CEI-6G, CEI-11G-LR | All rates | Compliant |

Notes:

1. 25 dB loss at Nyquist without FEC.
2. The transition time of the transmitter is faster than the IEEE Std 802.3-2012 specification.
3. This protocol requires external circuitry to achieve compliance.

Integrated Interface Block for Interlaken

More information and documentation on solutions using the integrated interface block for Interlaken can be found at [UltraScale+ Interlaken](#). The *UltraScale Architecture and Product Data Sheet: Overview (DS890)* lists how many blocks are in each Zynq UltraScale+ MPSoC. This section describes the following Interlaken configurations.

- 12 x 12.5 Gb/s protocol and lane logic mode ([Table 120](#)).
- 6 x 25.78125 Gb/s and 6 x 28.21 Gb/s protocol and lane logic mode ([Table 121](#)).
- 12 x 25.78125 Gb/s lane logic only mode ([Table 122](#)).

Table 120: Maximum Performance for Interlaken 12 x 12.5 Gb/s Protocol and Lane Logic Mode Designs

| Symbol | Description | Speed Grade and V _{CCINT} Operating Voltages | | | | | | | | | | Units |
|----------------------------|--|---|--------|------------------|--------|------------------|--------|------------------|--------|------------------|--------|-------|
| | | 0.90V | | 0.85V | | | | 0.72V | | | | |
| | | -3 | -2 | -1 | -2 | -1 | -2 | -1 | -2 | -1 | | |
| F _{RX_SERDES_CLK} | Receive serializer/deserializer clock | 195.32 | 195.32 | 195.32 | 195.32 | 195.32 | 195.32 | 195.32 | 195.32 | 195.32 | 195.32 | MHz |
| F _{TX_SERDES_CLK} | Transmit serializer/deserializer clock | 195.32 | 195.32 | 195.32 | 195.32 | 195.32 | 195.32 | 195.32 | 195.32 | 195.32 | 195.32 | MHz |
| F _{DRP_CLK} | Dynamic reconfiguration port clock | 250.00 | 250.00 | 250.00 | 250.00 | 250.00 | 250.00 | 250.00 | 250.00 | 250.00 | 250.00 | MHz |
| | | Min ¹ | Max | Min ¹ | Max | Min ¹ | Max | Min ¹ | Max | Min ¹ | Max | |
| F _{CORE_CLK} | Interlaken core clock | 300.00 | 322.27 | 300.00 | 322.27 | 300.00 | 322.27 | 300.00 | 322.27 | 300.00 | 322.27 | MHz |
| F _{LBUS_CLK} | Interlaken local bus clock | 300.00 | 322.27 | 300.00 | 322.27 | 300.00 | 322.27 | 300.00 | 322.27 | 300.00 | 322.27 | MHz |

Notes:

1. These are the minimum clock frequencies at the maximum lane performance.

Table 121: Maximum Performance for Interlaken 6 x 25.78125 Gb/s and 6 x 28.21 Gb/s Protocol and Lane Logic Mode Designs

| Symbol | Description | Speed Grade and V _{CCINT} Operating Voltages | | | | | | | | | | Units |
|----------------------------|--|---|-----------------|---------------------|--------|-----|--------|------------------|--------|-----|--------|-------|
| | | 0.90V | | 0.85V | | | | 0.72V | | | | |
| | | -3 ¹ | -2 ¹ | -1 | -2 | -1 | -2 | -1 | -2 | -1 | | |
| F _{RX_SERDES_CLK} | Receive serializer/deserializer clock | 440.79 | 440.79 | N/A | 402.84 | N/A | 402.84 | N/A | 402.84 | N/A | 402.84 | MHz |
| F _{TX_SERDES_CLK} | Transmit serializer/deserializer clock | 440.79 | 440.79 | N/A | 402.84 | N/A | 402.84 | N/A | 402.84 | N/A | 402.84 | MHz |
| F _{DRP_CLK} | Dynamic reconfiguration port clock | 250.00 | 250.00 | N/A | 250.00 | N/A | 250.00 | N/A | 250.00 | N/A | 250.00 | MHz |
| | | Min ² | Max | Min ² | Max | Min | Max | Min ² | Max | Min | Max | |
| F _{CORE_CLK} | Interlaken core clock | 412.50 ³ | 479.20 | 412.50 ³ | 479.20 | N/A | N/A | 412.50 | 429.69 | N/A | N/A | MHz |
| F _{LBUS_CLK} | Interlaken local bus clock | 300.00 ⁴ | 349.52 | 300.00 ⁴ | 349.52 | N/A | N/A | 300.00 | 349.52 | N/A | N/A | MHz |

Notes:

1. 6 x 28.21 mode is only supported in the -2 (V_{CCINT} = 0.85V) and -3 (V_{CCINT} = 0.90V) speed grades.
2. These are the minimum clock frequencies at the maximum lane performance.
3. The minimum value for CORE_CLK is 451.36 MHz for the 6 x 28.21 Gb/s protocol.
4. The minimum value for LBUS_CLK is 330.00 MHz for the 6 x 28.21 Gb/s protocol.

Table 122: Maximum Performance for Interlaken 12 x 25.78125 Gb/s Lane Logic Only Mode Designs

| Symbol | Description | Speed Grade and V _{CCINT} Operating Voltages | | | | | Units |
|----------------------------|--|---|--------|-----|-------|-----|-------|
| | | 0.90V | 0.85V | | 0.72V | | |
| | | -3 | -2 | -1 | -2 | -1 | |
| F _{RX_SERDES_CLK} | Receive serializer/deserializer clock | 402.84 | 402.84 | N/A | N/A | N/A | MHz |
| F _{TX_SERDES_CLK} | Transmit serializer/deserializer clock | 402.84 | 402.84 | N/A | N/A | N/A | MHz |
| F _{DRP_CLK} | Dynamic reconfiguration port clock | 250.00 | 250.00 | N/A | N/A | N/A | MHz |
| F _{CORE_CLK} | Interlaken core clock | 412.50 | 412.50 | N/A | N/A | N/A | MHz |
| F _{LBUS_CLK} | Interlaken local bus clock | 349.52 | 349.52 | N/A | N/A | N/A | MHz |

Integrated Interface Block for 100G Ethernet MAC and PCS

More information and documentation on solutions using the integrated 100 Gb/s Ethernet block can be found at [UltraScale+ Integrated 100G Ethernet MAC/PCS](#). The *UltraScale Architecture and Product Data Sheet: Overview (DS890)* lists how many blocks are in each Zynq UltraScale+ MPSoC.

Table 123: Maximum Performance for 100G Ethernet Designs

| Symbol | Description | Speed Grade and V _{CCINT} Operating Voltages | | | | | Units |
|---|---------------------------------------|---|---------|---------|---------|---------|-------|
| | | 0.90V | 0.85V | | 0.72V | | |
| | | -3 | -2 | -1 | -2 | -1 | |
| CAUI-10 Mode | | | | | | | |
| F _{TX_CLK} | Transmit clock | 390.625 | 390.625 | 322.266 | 322.266 | 322.266 | MHz |
| F _{RX_CLK} | Receive clock | 390.625 | 390.625 | 322.266 | 322.266 | 322.266 | MHz |
| F _{RX_SERDES_CLK} | Receive serializer/deserializer clock | 390.625 | 390.625 | 322.266 | 322.266 | 322.266 | MHz |
| F _{DRP_CLK} | Dynamic reconfiguration port clock | 250.00 | 250.00 | 250.00 | 250.00 | 250.00 | MHz |
| CAUI-4, CAUI-4 + RS-FEC, and RS-FEC Transcode Bypass Modes | | | | | | | |
| F _{TX_CLK} | Transmit clock | 390.625 | 322.266 | 322.266 | 322.266 | N/A | MHz |
| F _{RX_CLK} | Receive clock | 390.625 | 322.266 | 322.266 | 322.266 | N/A | MHz |
| F _{RX_SERDES_CLK} | Receive serializer/deserializer clock | 390.625 | 322.266 | 322.266 | 322.266 | N/A | MHz |
| F _{DRP_CLK} | Dynamic reconfiguration port clock | 250.00 | 250.00 | 250.00 | 250.00 | N/A | MHz |

Integrated Interface Block for PCI Express Designs

More information and documentation on solutions for PCI Express® designs can be found at [PCI Express](#). The *UltraScale Architecture and Product Data Sheet: Overview (DS890)* lists how many blocks are in each Zynq UltraScale+ MPSoC.

Table 124: Maximum Performance for PCI Express Designs

| Symbol | Description | Speed Grade and V _{CCINT} Operating Voltages | | | | | Units |
|----------------------|------------------------------|---|--------|--------|--------|--------|-------|
| | | 0.90V | 0.85V | | 0.72V | | |
| | | -3 | -2 | -1 | -2 | -1 | |
| F _{PIPECLK} | Pipe clock maximum frequency | 250.00 | 250.00 | 250.00 | 250.00 | 250.00 | MHz |
| F _{CORECLK} | Core clock maximum frequency | 500.00 | 500.00 | 500.00 | 250.00 | 250.00 | MHz |
| F _{DRPCLK} | DRP clock maximum frequency | 250.00 | 250.00 | 250.00 | 250.00 | 250.00 | MHz |
| F _{MCAPCLK} | MCAP clock maximum frequency | 125.00 | 125.00 | 125.00 | 125.00 | 125.00 | MHz |

Video Codec Performance

The *UltraScale Architecture and Product Data Sheet: Overview (DS890)* lists the Zynq UltraScale+ MPSoC EV devices that include the Video Codec unit (VCU).

Table 125: VCU Performance

| Description | Speed Grade and V _{CCINT} Operating Voltages ¹ | | | | | Units |
|--|--|-------|-----|-------|-----|-------|
| | 0.90V | 0.85V | | 0.72V | | |
| | -3 | -2 | -1 | -2 | -1 | |
| Video Codec encoder/decoder block maximum frequency (H.264/5 10-bit 4:2:2, UHD 3840 x 2160) | 667 | 667 | 667 | 667 | 667 | MHz |
| Video Codec encoder/decoder block maximum frequency (H.264/5 10-bit 4:2:2, DCI 4k (4096 x 2160) ² | 712 | 712 | N/A | 712 | N/A | MHz |

Notes:

- The supply voltage for the VCU (V_{CCINT_VCU}) is specified in Table 2.
- DCI 4k is supported for frame rates of 60 Hz using an encoder/decoder block frequency of 712 MHz.

PL System Monitor Specifications

Table 126: PL SYSMON Specifications

| Parameter | Symbol | Comments/Conditions | Min | Typ | Max | Units |
|--|--------|--|-----|-----|------|-------|
| V _{CCADC} = 1.8V ±3%, V _{REFP} = 1.25V, V _{REFN} = 0V, ADCCLK = 5.2 MHz, T _j = -40°C to 100°C, typical values at T _j = 40°C | | | | | | |
| ADC Accuracy¹ | | | | | | |
| Resolution | | | 10 | - | - | Bits |
| Integral nonlinearity ² | INL | | - | - | ±1.5 | LSBs |
| Differential nonlinearity | DNL | No missing codes, guaranteed monotonic | - | - | ±1 | LSBs |
| Offset error | | Offset calibration enabled | - | - | ±2 | LSBs |
| Gain error | | | - | - | ±0.4 | % |
| Sample rate | | | - | - | 0.2 | MS/s |
| RMS code noise | | External 1.25V reference | - | - | 1 | LSBs |
| | | On-chip reference | - | 1 | - | LSBs |
| ADC Accuracy at Extended Temperatures | | | | | | |
| Resolution | | T _j = -55°C to 125°C | 10 | - | - | Bits |

Table 126: PL SYSMON Specifications (cont'd)

| Parameter | Symbol | Comments/Conditions | Min | Typ | Max | Units |
|---|--|--|------|------|-------------|------------------|
| Integral nonlinearity ² | INL | $T_j = -55^\circ\text{C}$ to 125°C | - | - | ± 1.5 | LSBs |
| Differential nonlinearity | DNL | No missing codes, guaranteed monotonic $T_j = -55^\circ\text{C}$ to 125°C | - | - | ± 1 | |
| Analog Inputs² | | | | | | |
| ADC input ranges | Unipolar operation | | 0 | - | 1 | V |
| | Bipolar operation | | -0.5 | - | +0.5 | V |
| | Unipolar common mode range (FS input) | | 0 | - | +0.5 | V |
| | Bipolar common mode range (FS input) | | +0.5 | - | +0.6 | V |
| Maximum external channel input ranges | Adjacent channels set within these ranges should not corrupt measurements on adjacent channels | | -0.1 | - | V_{CCADC} | V |
| On-Chip Sensor Accuracy | | | | | | |
| Temperature sensor error ^{1,3} | $T_j = -55^\circ\text{C}$ to 125°C (with external REF) | | - | - | ± 3 | $^\circ\text{C}$ |
| | $T_j = -55^\circ\text{C}$ to 110°C (with internal REF) | | - | - | ± 3.5 | $^\circ\text{C}$ |
| | $T_j = 110^\circ\text{C}$ to 125°C (with internal REF) | | - | - | ± 5 | $^\circ\text{C}$ |
| Supply sensor error ⁴ | Supply voltages 0.72V to 1.2V, $T_j = -40^\circ\text{C}$ to 100°C (with external REF) | | - | - | ± 0.5 | % |
| | Supply voltages 0.72V to 1.2V, $T_j = -55^\circ\text{C}$ to 125°C (with external REF) | | - | - | ± 1.0 | % |
| | All other supply voltages, $T_j = -40^\circ\text{C}$ to 100°C (with external REF) | | - | - | ± 1.0 | % |
| | All other supply voltages, $T_j = -55^\circ\text{C}$ to 125°C (with external REF) | | - | - | ± 2.0 | % |
| | Supply voltages 0.72V to 1.2V, $T_j = -40^\circ\text{C}$ to 100°C (with internal REF) | | - | - | ± 1.0 | % |
| | Supply voltages 0.72V to 1.2V, $T_j = -55^\circ\text{C}$ to 125°C (with internal REF) | | - | - | ± 2.0 | % |
| | All other supply voltages, $T_j = -40^\circ\text{C}$ to 100°C (with internal REF) | | - | - | ± 1.5 | % |
| | All other supply voltages, $T_j = -55^\circ\text{C}$ to 125°C (with internal REF) | | - | - | ± 2.5 | % |
| Conversion Rate⁵ | | | | | | |
| Conversion time—continuous | t_{CONV} | Number of ADCCLK cycles | 26 | - | 32 | Cycles |
| Conversion time—event | t_{CONV} | Number of ADCCLK cycles | - | - | 21 | Cycles |
| DRP clock frequency | DCLK | DRP clock frequency | 8 | - | 250 | MHz |
| ADC clock frequency | ADCCLK | Derived from DCLK | 1 | - | 5.2 | MHz |
| DCLK duty cycle | | | 40 | - | 60 | % |
| SYSMON Reference⁶ | | | | | | |
| External reference | V_{REFP} | Externally supplied reference voltage | 1.20 | 1.25 | 1.30 | V |

Table 126: PL SYSMON Specifications (cont'd)

| Parameter | Symbol | Comments/Conditions | Min | Typ | Max | Units |
|-------------------|--------|---|--------|------|--------|-------|
| On-chip reference | | Ground V_{REFP} pin to AGND, $T_j = -40^\circ\text{C}$ to 100°C | 1.2375 | 1.25 | 1.2625 | V |
| | | Ground V_{REFP} pin to AGND, $T_j = -55^\circ\text{C}$ to 125°C | 1.225 | 1.25 | 1.275 | V |

Notes:

- ADC offset errors are removed by enabling the ADC automatic offset calibration feature. The values are specified for when this feature is enabled.
- See the Analog Input section in the *UltraScale Architecture System Monitor User Guide* (UG580).
- When reading temperature values directly from the PMBus interface, the SYSMON has a $+4^\circ\text{C}$ offset due to the transfer function used by the PMBus application. For example, the external REF temperature sensor error's range of $\pm 3^\circ\text{C}$ becomes $+1^\circ\text{C}$ to $+7^\circ\text{C}$ when the temperature is read through the PMBus interface.
- Supply sensor offset and gain errors are removed by enabling the automatic offset and gain calibration feature. The values are specified for when this feature is enabled.
- See the Adjusting the Acquisition Settling Time section in the *UltraScale Architecture System Monitor User Guide* (UG580).
- Any variation in the reference voltage from the nominal $V_{REFP} = 1.25\text{V}$ and $V_{REFN} = 0\text{V}$ will result in a deviation from the ideal transfer function. This also impacts the accuracy of the internal sensor measurements (i.e., temperature and power supply). However, for external ratiometric type applications allowing reference to vary by $\pm 4\%$ is permitted.

PL SYSMON I2C/PMBus Interfaces

Table 127: PL SYSMON I2C Fast Mode Interface Switching Characteristics

| Symbol | Description ¹ | Min | Max | Units |
|--------------|--------------------------|-----|-----|---------------|
| T_{SMFCKL} | SCL Low time | 1.3 | - | μs |
| T_{SMFCKH} | SCL High time | 0.6 | - | μs |
| T_{SMFCKO} | SDAO clock-to-out delay | - | 900 | ns |
| T_{SMFDCK} | SDAI setup time | 100 | - | ns |
| F_{SMFCLK} | SCL clock frequency | - | 400 | kHz |

Notes:

- The test conditions are configured to the LVCMOS 1.8V I/O standard.

Table 128: PL SYSMON I2C Standard Mode Interface Switching Characteristics

| Symbol | Description ¹ | Min | Max | Units |
|--------------|--------------------------|-----|------|---------------|
| T_{SMSCKL} | SCL Low time | 4.7 | - | μs |
| T_{SMSCKH} | SCL High time | 4.0 | - | μs |
| T_{SMSCKO} | SDAO clock-to-out delay | - | 3450 | ns |
| T_{SMSDCK} | SDAI setup time | 250 | - | ns |
| F_{SMSCLK} | SCL clock frequency | - | 100 | kHz |

Notes:

- The test conditions are configured to the LVCMOS 1.8V I/O standard.

Configuration Switching Characteristics

Table 129: Configuration Switching Characteristics

| Symbol | Description | Speed Grade and V _{CCINT} Operating Voltages | | | | | Units |
|---|--|---|-------|-------|-------|-------|----------|
| | | 0.90V | 0.85V | | 0.72V | | |
| | | -3 | -2 | -1 | -2 | -1 | |
| PL Power-up Timing Characteristics | | | | | | | |
| T _{PL} | PS_PROG_B PL latency | 7.5 | 7.5 | 7.5 | 7.5 | 7.5 | ms, Max |
| T _{POR} ^{1,2} | Power-on reset from PL power-on to PL ready to configure (40 ms ramp rate time) | 65 | 65 | 65 | 65 | 65 | ms, Max |
| | | 0 | 0 | 0 | 0 | 0 | ms, Min |
| | Power-on reset from PL power-on to PL ready to configure with POR override (2 ms ramp rate time) | 15 | 15 | 15 | 15 | 15 | ms, Max |
| | | 5 | 5 | 5 | 5 | 5 | ms, Min |
| T _{PS_PROG_B} | PL program pulse width | 250 | 250 | 250 | 250 | 250 | ns, Min |
| Internal Configuration Access Port | | | | | | | |
| F _{ICAPCK} | Internal configuration access port (ICAPE3) | 200 | 200 | 200 | 150 | 150 | MHz, Max |
| DNA Port Switching | | | | | | | |
| F _{DNACK} | DNA port frequency (DNA_PORT) | 200 | 200 | 200 | 175 | 175 | MHz, Max |
| STARTUPE3 Ports | | | | | | | |
| F _{CFGMCLK} | STARTUPE3 CFGMCLK output frequency | 50.00 | 50.00 | 50.00 | 50.00 | 50.00 | MHz, Typ |
| F _{CFGMCLKTOL} | STARTUPE3 CFGMCLK output frequency tolerance | ±15 | ±15 | ±15 | ±15 | ±15 | %, Max |
| T _{DCL_MATCH} | Specifies a stall in the startup cycle until the digitally controlled impedance (DCI) match signals are asserted | 4 | 4 | 4 | 4 | 4 | ms, Max |

Notes:

1. The T_{POR} specification begins when the last of the monitored supplies (V_{CCINT}, V_{CCAUX}, V_{CCBRAM}) reaches 95% of its recommended operating condition voltage.
2. The POR override (POR_OVERRIDE pin tied to V_{CCINT}) is applicable only when the monitored supplies ramp within the specified time.

Revision History

| Date | Version | Description of Revisions |
|-----------|---------|---|
| 3/13/2020 | 1.17 | Removed the XAZU7EV and XAZU11EG in the -1LI (V _{CCINT} = 0.72V) speed/temperature grades because they were incorrectly added in the previous version. The XAZU7EV and XAZU11EG in the -1I speed/temperature grade was moved back to advance in Table 26 and Table 27 . Updated Table 25 to Vivado Design Suite 2019.2.2 v1.27. Added Note 10 to Table 17 . Revised symbol and description of IOPLL_TO_FPD maximum frequency in Table 38 . Increased the maximum line rate of the QPLL0 -1 (V _{CCINT} = 0.85V) output divider 1 in Table 111 and updated Notes 2 and 3. |
| 7/19/2019 | 1.16 | Added the production released XAZU7EV and XAZU11EG devices in the -1I (V _{CCINT} = 0.85V), -1Q (V _{CCINT} = 0.85V), and -1LI (V _{CCINT} = 0.72V) speed/temperature grades to Table 25 , Table 26 , and Table 27 in Vivado Design Suite 2019.1.1 v1.26. Added Note 7 to Vivado Design Suite v2019.1.1 or later to increase the performance of the MIPI PHY transmitter/receiver in . Added the capability for XC and XA devices designed using Table 72 . |

| Date | Version | Description of Revisions |
|------------|---------|---|
| 6/11/2019 | 1.15 | <p>Added the production released XQZU3, XQZU9, XQZU11, and XQZU19 devices throughout data sheet (including adding SFRA484, FFRB1517, and FFRC1760 packages).</p> <p>Updated the devices listed in Table 25 to Vivado Design Suite 2019.1 v1.25</p> <p>Revised minimum PS DDR data rates for all I-grade devices in Table 30: PS DDR Performance.</p> <p>Updated Note 1 in Table 35: PS RTC Crystal Requirements.</p> <p>. Added the capability for XC and XAAdded -1Q and -1M to Note 4 in Table 104: GTH Transceiver User Clock Switching Characteristics.</p> <p>Removed PCI Express Gen4 support in Table 124: Maximum Performance for PCI Express Designs.</p> <p>Updated Notes 5 and 7 in Table 30.</p> <p>Updated the Video Codec Performance table.</p> |
| 11/15/2018 | 1.14 | <p>Added the production released XQZU5EV, XQZU7EV, and XQZU15EG devices in the -2I, -1I, -1M, and -1LI speed/temperature grades to Table 25, Table 26, and Table 27 in Vivado Design Suite 2018.2.2 v1.22.</p> <p>Updated Note 3 in Table 6, Table 7, Table 8. Updated the V_{IDIFF} description in Table 24. In Table 69, revised the Supply Sensor Error T_j conditions to -55°C.</p> <p>Added the SFRC784, FFRB900, FFRB1156, and FFRC1156 packages to Table 1, Table 2, Table 30, Table 74, and Table 99, and the Integrated Interface Block for Interlaken section.</p> <p>Updated the speed grade notes in Table 116.</p> <p>Add the XQZU5EV, XQZU7EV, and XQZU15EG devices to Table 3, Table 9, Table 10, Table 87, Table 88, Table 89, Table 91, Table 92, and Table 95.</p> |
| 8/01/2018 | 1.13 | <p>Updated Table 25, Table 26, and Table 27 to production release the XCZU4EG, XCZU4EV, XCZU5EG, XCZU5EV, XCZU6EG, XCZU7EG, XCZU7EV, and XCZU9EG devices in the -3E speed/temperature grade and in Vivado Design Suite 2018.2.1 v1.21.</p> <p>In Table 71, added Note 5 to the LVDS RX DDR maximum data.</p> <p>In Table 123, revised the calculated values from 322.223 to 322.266.</p> <p>In Table 129, added Notes 1 and 2.</p> |
| 6/18/2018 | 1.12 | <p>Updated Table 25, Table 26, and Table 27 to production release the XAZU4EV and XAZU5EV devices in the -1Q speed/temperature grade in Vivado Design Suite 2018.2 v1.20.</p> <p>In DC Characteristics Over Recommended Operating Conditions, clarified the descriptions. Revised the speed grade -1 ($V_{CCINT} = 0.85$) F_{GTYMAX} in Table 111, which also revised values in Table 116 and added Note 6.</p> |
| 4/09/2018 | 1.11 | <p>Updated Table 25, Table 26, and Table 27 to production release the XCZU11EG, XCZU15EG, XCZU17EG, and XCZU19EG devices in the -3E speed/temperature grade in Vivado Design Suite 2018.1 v1.19.</p> <p>Added the Conversion Rate section to Table 69. Added Table 90 and Table 94. Added Note 2 and 3 to Table 93. Revised Table 123 to add specific mode specifications and remove Notes 1 and 2.</p> |
| 2/07/2018 | 1.10 | <p>Added the XAZU4EV and XAZU5EV devices to many tables.</p> <p>In Table 2, revised the V_{CCINT_VCU} specifications, added automotive (Q) temperature to T_j, and updated Note 5.</p> <p>Added the -1Q note to Table 6, Table 7, and Table 8.</p> <p>Updated Table 25, Table 26, and Table 27 to production for the following devices/speed/temperature grades in Vivado Design Suite 2017.4.1 v1.18.</p> <p>XCZU4CG/XCZU4EG/XCZU4EV: -2LE and -1LI</p> <p>XCZU5CG/XCZU5EG/XCZU5EV: -2LE and -1LI</p> <p>XCZU7CG/XCZU7EG/XCZU7EV: -2LE and -1LI</p> <p>XCZU11EG: -2LE and -1LI</p> <p>XCZU4EV and XAZU5EV: -1LI</p> <p>In Vivado Design Suite 2017.4 v1.17, the XAZU4EV and XAZU5EV devices in the -1I speed/temperature grade were production released.</p> <p>Revised some of the -3E speed files in Table 75, Table 87, Table 88, Table 89, Table 91, and Table 92.</p> |
| 11/28/2017 | 1.9 | <p>Updated Table 25, Table 26, and Table 27 to production for the following devices/speed/temperature grades in Vivado Design Suite 2017.4 v1.17.</p> <p>XCZU4CG/XCZU4EG/XCZU4EV: -2E, -2I, -1E, -1I</p> <p>XCZU5CG/XCZU5EG/XCZU5EV: -2E, -2I, -1E, -1I</p> <p>XCZU7CG/XCZU7EG/XCZU7EV: -2E, -2I, -1E, -1I</p> <p>XCZU17EG: -2LE and -1LI</p> <p>XCZU19EG: -2LE and -1LI</p> <p>Revised the F_{REFCLK} descriptions in Table 82. Added values to Table 95. Revised the $F_{GTYQRANGE2}$ -1 speed grade minimum in Table 111.</p> |

| Date | Version | Description of Revisions |
|------------|---------|--|
| 10/26/2017 | 1.8 | <p>In Table 1, corrected the minimum voltage for the PL System Monitor section. Added Note 4 to Table 2. Added Note 1 to Table 5.</p> <p>Updated Table 25, Table 26, and Table 27 to production for the following devices/speed/temperature grades in Vivado Design Suite 2017.3.1 v1.16.</p> <p>XCZU2CG/XCZU2EG: -2LE and -1LI XCZU3CG/XCZU3EG: -2LE and -1LI XCZU6CG/XCZU6EG: -2LE and -1LI XCZU9CG/XCZU9EG: -2LE and -1LI XCZU15EG: -2LE and -1LI XAZU2EG/XAZU3EG: -1LI</p> <p>Also updated speed file data for this release in Table 87, Table 88, Table 89, Table 91, and Table 92.</p> <p>Added specifications for Quad-SPI device clock frequency operating at 40 MHz with loopback disabled to Table 41 and Table 42.</p> |
| 10/05/2017 | 1.7 | <p>Corrected the speed file version in Table 25 and Table 27 for production release of XAZU2EG and XAZU3EG with -1I and -1Q speed/temperature ranges and the XCZU11EG: -2E, -2I, -1E, -1I to Vivado Design Suite 2017.3 v1.15.</p> |
| 10/03/2017 | 1.6 | <p>In Table 1, because the voltages are covered in Table 6, removed the note on V_{IN} for I/O input voltage for HD I/O banks. Updated T_{SOL} by package in Table 1. In Table 2, updated V_{CCINT_VCU}. Added Note 2 to Table 6 and Table 8.</p> <p>Added the XAZU2EG and XAZU3EG production devices in -1I and -1Q speed/temperature ranges using Vivado Design Suite 2017.3 v1.14.</p> <p>In Table 25, Table 26, and Table 27, updated the XCZU11EG: -2E, -2I, -1E, -1I to production in Vivado Design Suite 2017.3 v1.14. Also updated speed file data for this release in Table 87, Table 88, Table 89, Table 91, and Table 92.</p> |
| 9/01/2017 | 1.5 | <p>Updated Table 25, Table 26, and Table 27 to production release for the following devices/speed/temperature grades in Vivado Design Suite 2017.2.1.</p> <p>XCZU17EG: -2E, -2I, -1E, -1I XCZU19EG: -2E, -2I, -1E, -1I</p> <p>In Table 45, revised the minimum $T_{SDSDRDCk3}$ value. In Table 76, revised the $T_{OUTBUF_DELAY_O_PAD -2}$ ($V_{CCINT} = 0.85V$) values for DIFF_SSTL135_S, DIFF_SSTL15_DCI_S, DIFF_SSTL15_S, DIFF_SSTL18_I_DCI_S, and DIFF_SSTL18_I_S.</p> <p>Revised some of the -3E and -1LI/-2LE ($V_{CCINT} = 0.72V$) speed files in Table 75, Table 76, Table 77, Table 87, Table 88, Table 89, Table 91, and Table 92.</p> <p>Revised the Integrated Interface Block for Interlaken section.</p> |
| 6/28/2017 | 1.4 | <p>Updated Table 25, Table 26, and Table 27 to production release for the following devices/speed/temperature grades in Vivado Design Suite 2017.2.</p> <p>XCZU15EG: -2E, -2I, -1E, -1I</p> <p>Updated Note 15 in Table 2 for clarity. Updated Table 14 to remove Note 3, Note 6, and the MIPI_DPHY_DCI_LP row. These changes are because the DCI and POD standards are not supported in HD I/O banks.</p> <p>Added Note 5 to Table 30. Updated descriptions in Table 38. Revised the -3E and -1LI/-2LE ($V_{CCINT} = 0.72V$) speed files in Table 75, Table 76, Table 77, Table 87, Table 88, Table 89, Table 91, and Table 92. Updated the F_{MAX} symbol names and values in Table 81. Added Note 1 to Table 83. Added Note 3 to Table 124.</p> |

| Date | Version | Description of Revisions |
|-----------|---------|---|
| 4/20/2017 | 1.3 | <p>Updated Table 25, Table 26, and Table 27 to production release for the following devices/speed/temperature grades in Vivado Design Suite 2017.1.</p> <p>XCZU2CG and XCZU2EG: -2E, -2I, -1E, -1I</p> <p>XCZU3CG and XCZU3EG: -2E, -2I, -1E, -1I</p> <p>XCZU6CG and XCZU6EG: -2E, -2I, -1E, -1I</p> <p>XCZU9CG and XCZU9EG: -2E, -2I, -1E, -1I</p> <p>Added -2E ($V_{CCINT} = 0.85V$) speed grade where applicable. Removed -3E speed grade from the XCZU2 and XCZU3 devices in Table 26 and where applicable.</p> <p>In Table 1, updated values and Note 2. In Table 2, added or updated many of the notes. Updated Table 4 including the notes and added Note 6. Moved and updated Table 5. Added Table 8. Updated Table 9 and added Note 4. Updated Table 10 and added Note 1.</p> <p>Revised V_{ICM} in Table 23. Updated Table 30 and removed Note 1. Added Table 31 and Table 32. Updated Table 33 and removed F_{FTMCLK}. Updated $T_{RFPSClk}$ in Table 34. Updated Note 1 in Table 37. Updated Table 39. Removed the PS NAND Memory Controller Interface section. Significant changes to Table 41 and removed Note 3. Significant changes to Table 42 and updated Note 1. Removed $F_{TSU_REF_CLK}$ from Table 44. Revised Table 45 and added Note 2 and Note 3. Revised Table 46 and added Note 2 and Note 3. Updated Table 48. Updated Table 51 and removed Note 2. Revised Table 52. Revised many of the tables in the PS-GTR Transceiver section. Revised Table 70 and Table 71. Removed Note 8 from Table 74.</p> <p>Updated the values in Table 75, Table 76, Table 77, Table 80, Table 87, Table 88, Table 89, Table 91, and Table 92 to the Vivado Design Suite 2017.1 speed specifications.</p> <p>Updated the values in Table 81 and Table 82. Added values to Table 93. Updated Table 95. Revised D_{VPP_OUT} in Table 96. Update the values in Table 98. Added Note 6 to Table 104. Updated Table 105 and Table 106. Revised D_{VPP_OUT} in Table 108. Updated the values in Table 110. In Table 111 updated the -1 (0.85V) specifications and removed Note 1. In Table 116 updated the -1 (0.85V) specifications and added Note 6. In Table 117 and Table 118, added the 28.21 jitter tolerance values and revised the notes. Revised the Integrated Interface Block for Interlaken and Integrated Interface Block for 100G Ethernet MAC and PCS sections. Revised the Configuration Switching Characteristics section. Removed the eFUSE Programming Conditions table and added the specifications to Table 2 and Table 3.</p> |
| 2/10/2017 | 1.2 | <p>Updated some of the maximum voltages in the Processor System (PS) section and other specifications in the Programmable Logic (PL) and GTH or GTY Transceiver sections of Table 1. Updated Table 2, Table 4, Table 6, Table 8, and Table 9. Revised the Power Supply Sequencing section including Table 10. Added PS and VCU ramp times to Table 11. Revised V_{ODIFF} in Table 24. Updated Table 25. Added Note 1 to Table 26. Table 27 replaces the previous three PS memory performance tables. Added values to Table 34, Table 37, and Table 38. Deleted the waveforms in the PS Switching Characteristics section (Figures 1-16 and Figures 25-26). Revised values in the PS NAND Memory Controller Interface section. Added and updated data in Table 40. Added Note 3 to Table 41. Added Note 3 to Table 42. Added Note 1 to Table 45. Updated Table 48 and removed Note 3. Added data to Table 56. Updated Table 60. Added Table 61. Updated Table 63. Revised Table 69. Added data to Table 70. Added Note 2 to Table 71. Updated Table 74 and added Note 4. Updated V_L and V_H values in Table 78. Added T_{MINPER_CLK}, revised F_{REFCLK}, and Note 1 to Table 82. Added $MCM_FDPRCLK_MAX$ to Table 85 and $PLL_FDPRCLK_MAX$ to Table 86. Added data to Table 96, Table 98, Table 100, Table 103, and updated the note references in Table 104. Updated Table 105 and added Note 8. Updated Table 106 and added Note 7. Added more protocols, Note 1 and Note 2 to Table 107. Removed the GTH Transceiver Protocol Jitter Characteristics section because it is covered in Table 107. Added Note 1 to Table 111. Added data to Table 108, Table 110, Table 112, Table 115. Added Note 2 to Table 114. Added note references in Table 116. Updated Table 117 and added Note 8. Updated Table 118 and added Note 7. Added more protocols and Note 3 to Table 119. Removed the GTY Transceiver Protocol Jitter Characteristics section because it is covered in Table 119. Revised Table 126. Added T_{POR} and updated F_{ICAPCK} in Table 129. Updated the Automotive Applications Disclaimer.</p> |

| Date | Version | Description of Revisions |
|------------|---------|---|
| 6/20/2016 | 1.1 | <p>Updated the Summary description. In Table 1, revised V_{IN} for HP I/O banks and added clarifications to some descriptions and symbols. Added I_{RPUI}, I_{RPD}, and Note 4 to Table 2 and updated $V_{PS_MGTRAVCC}$, the PL System Monitor section, and Note 3 and Note 5. Updated Note 5 in Table 4. Updated the PS Power-On/Off Power Supply Sequencing section including all the voltage supply names. Added MIPI_DPHY_DCI to Table 14, Table 15, and Table 17. Updated Table 23, including removing the V_{CCO} specification and adding Note 1. Added Note 1 to Table 24. Updated Table 25 speed specifications for Vivado Design Suite 2016.1. Added values to Table 28. Updated the -2 value in Table 29. Added $F_{DPLIVEVIDEO}$ and updated $F_{FCIDMACLK}$ in Table 33. Added VCO frequencies to Table 36. Added the T_{PSPOR} minimum to Table 37 and updated Note 1. Added Table 38. Added value delineation over V_{CCINT} operating voltages in Table 39. Revised values for F_{TCK} and T_{TAPTCK}/T_{TCKTAP} in Table 40 and added value delineation over V_{CCINT} operating voltages. Updated the PS NAND Memory Controller Interface section. Revised some units and Note 1 in Table 41 and Table 42. Removed Figure 6: Quad-SPI Interface (Feedback Clock Disabled) Timing. Updated Note 1 of Table 43. Added $F_{TSL_REF_CLK}$ to Table 44 and updated Note 1. In Table 45, revised $T_{DCSDHSCLK1}$, $T_{DCSDHSCLK2}$, and $T_{DCSDHSCLK3}$ and Note 1. In Table 46, revised Note 1. In Table 47, revised Note 1. Revised Table 48, including Note 1, and added Note 2 and Note 3. In Table 50, Table 49, Table 51, and Table 53, revised Note 1. Updated Table 71. Replaced Table 74. Updated Table 75 and Table 76. Updated Table 78 and Table 79. In Table 80, added the Block RAM and FIFO Clock-to-Out Delays section. Updated the R_{IN} and C_{EXT} values in Table 57 and Table 97. Updated the -2 (0.72V) and -1 (0.72V) values and added Note 1 to Table 99. Added Table 102 and Table 114. Added Note 2 to Table 108. Revised data in Table 111. Revised Table 116. Revised data and added notes in the Integrated Interface Block for Interlaken section and Table 123. Moved Table 125. Revised INL in Table 126. Added notes to Table 127 and Table 128. In the eFUSE and Programming Conditions table, updated the I_{P5F5} description.</p> |
| 11/24/2015 | 1.0 | Initial Xilinx release. |

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OUR CERTIFICATE

A long-term cooperative relationship can be built between global customers and us by providing excellent products



| | |
|----------------------|---|
| Business Type | Trading Company, Distributor/Wholesaler |
| Main Products | Electronic Integrated Circuit |
| Certifications | ISO9001 |
| Total Annual Revenue | US\$2.5 Million - US\$5 Million |
| Country / Region | Hongkong, China |
| Total Employees | 100 - 200 People |
| Year Established | 2018 |
| Main Markets | North America South Asia Western Europe |